

Design and System Drivers

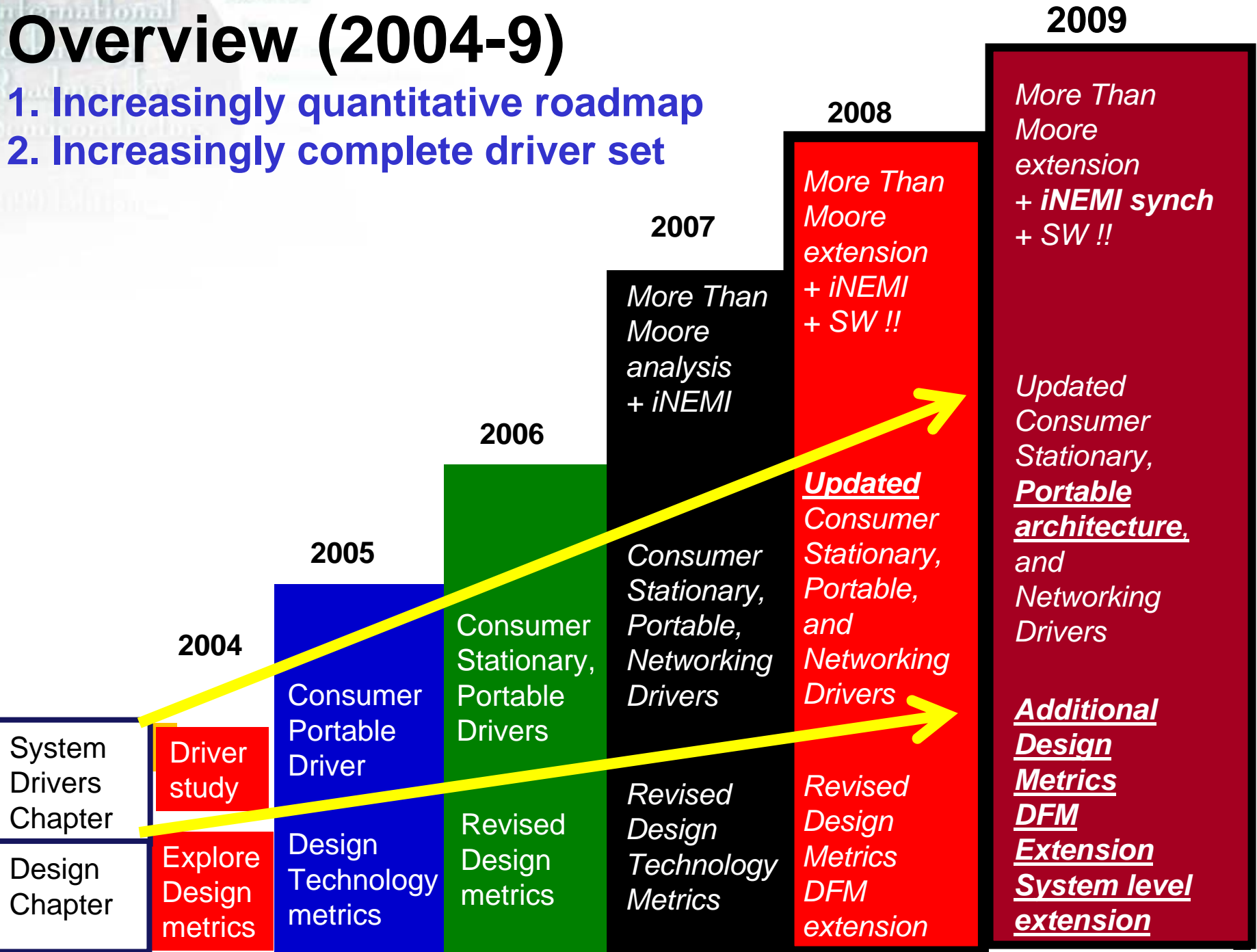
Worldwide Design ITWG: T. Hiwatashi (Japan), W. Rosenstiel (Europe), V. Kathail (USA), J.-A. Carballo (USA), A. B. Kahng (USA)

Key messages:

- 1. Software, system level design productivity critical to roadmap**
- 2. Design technology is key to variability / “sigma” control**
- 3. System-level design technology is key to power efficiency**
- 4. Design cost will be contained through innovation**
- 5. MtM brings new set of Design requirements/solutions**
- 6. Initiating reliability roadmap for 2010-2011**

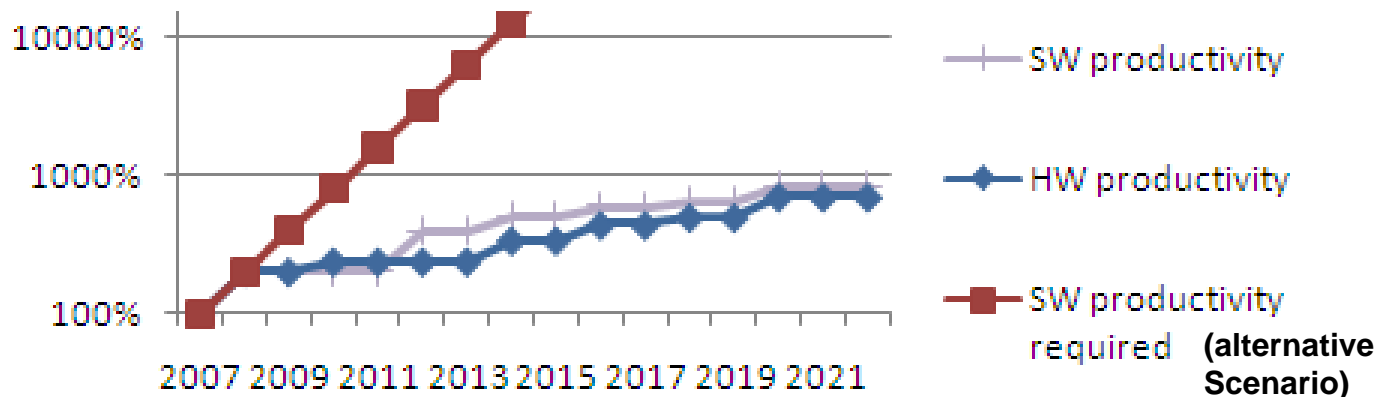
Overview (2004-9)

- 1. Increasingly quantitative roadmap
- 2. Increasingly complete driver set



System Level Design & SOFTWARE

- **Hardware design productivity is growing appropriately**
 - Requirements correspond roughly with solutions
 - Innovations pacing properly (transistors / designer / year)
- **Large gap in software productivity possibly opening up**
 - If hardware accelerators are heavily leveraged, problem mitigated
 - Otherwise, possibly 100X gap can affect memory size, other
- **Adding new parameters to requirements/solutions tables**
 - Hardware design productivity - **requirement**
 - Software design productivity - **requirement**
 - Software design productivity (assuming only software implementation)
 - System design productivity innovations – **solutions** (Fig. 1 in chapter)



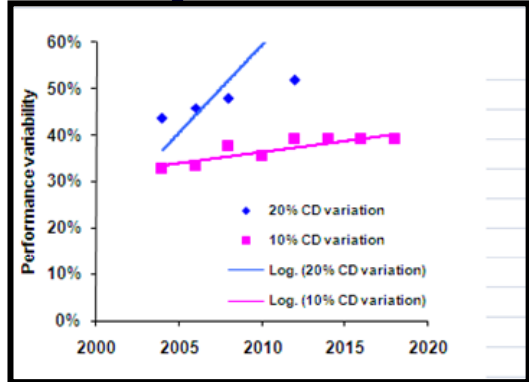
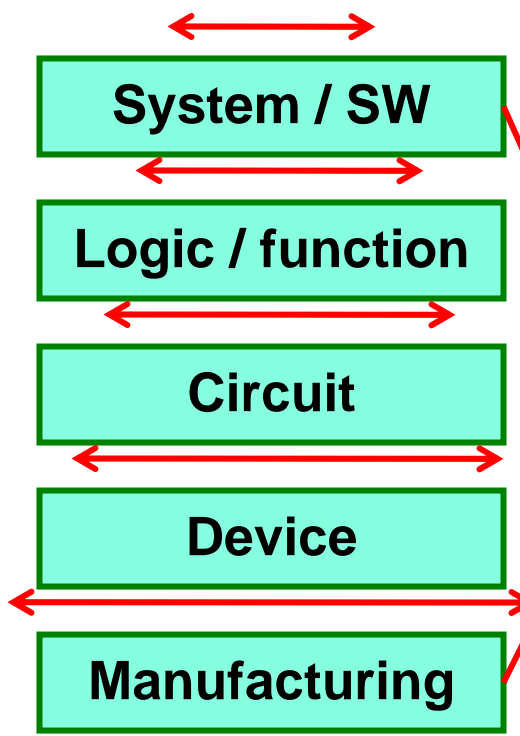
Impact of Design on "Sigma" (Variability)

Goal

Quantify "how many sigmas" can design "reduce"

Approach

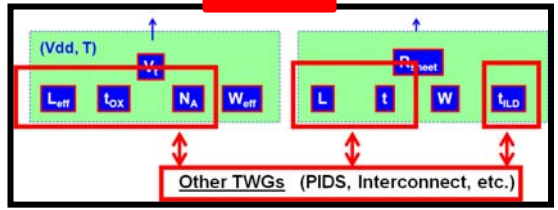
- Inventory of design techniques / tools
- Match inventory to parameters or correlations in model
- Use variability model to capture "delta" in sigmas



Check overall variation

| | CD variation | CD % variation | delay variation | Power variation | Leakage power variation |
|------|--------------|----------------|-----------------|-----------------|-------------------------|
| 2004 | 0.012 | 12% | 44% | 45% | 123% |
| 2006 | 0.0084 | 12% | 46% | 50% | 201% |
| 2008 | 0.00684 | 12% | 48% | 62% | 240% |
| 2010 | 0.00552 | 12% | 61% | 68% | 289% |
| 2012 | 0.0042 | 12% | 52% | 60% | 306% |
| 2014 | 0.00336 | 12% | 77% | 89% | 397% |
| 2016 | 0.00276 | 12% | 89% | 107% | 335% |
| 2018 | 0.00216 | 12% | 93% | 112% | 551% |
| 2020 | 0.00156 | 12% | 115% | 113% | 545% |
| 2022 | 0.00096 | 12% | 126% | 103% | 548% |

Use variability model

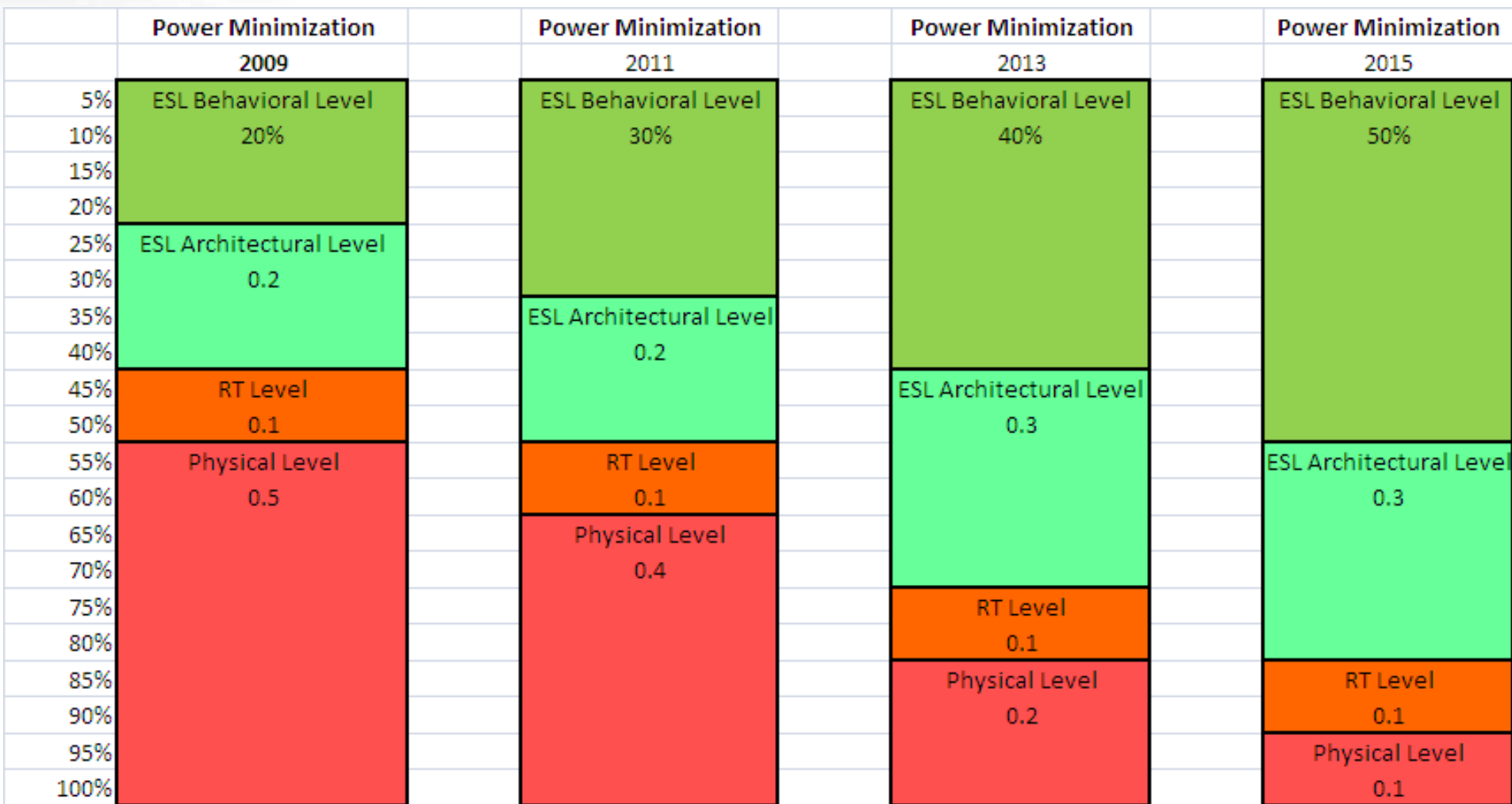


Inputs (manufacturing) 4



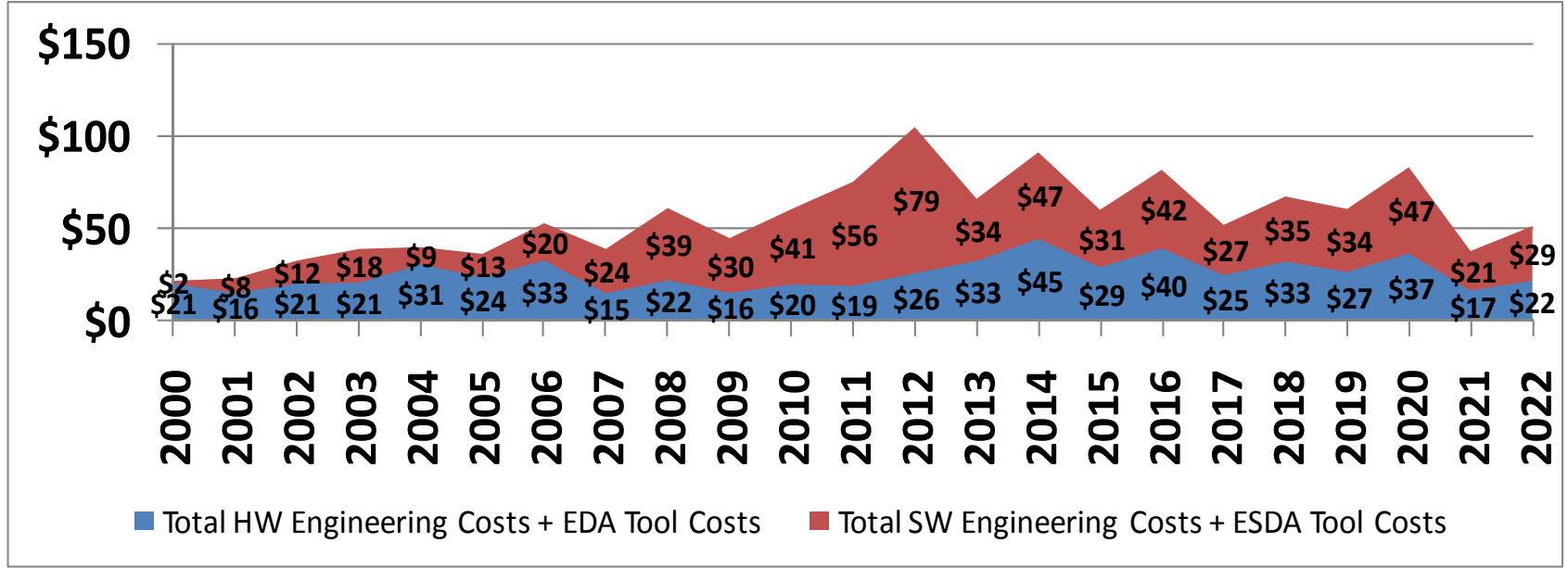
Impact of Design on Power

Emphasis on System Level [SW/HW]



ITRS Cost Chart 2009 (Millions of Dollars)

IC Implementation Tool Set
 RTL Functional Verif. Tool Set
 Transaction Level Modeling
 Very Large Block Reuse
 AMP Parallel Processing
 Intelligent Testbench
 Many Core Devel. Tools
 SMP Parallel Processing
 Transactional Memory
 System Design Automation
 Executable Specification



More Than Moore (Design)

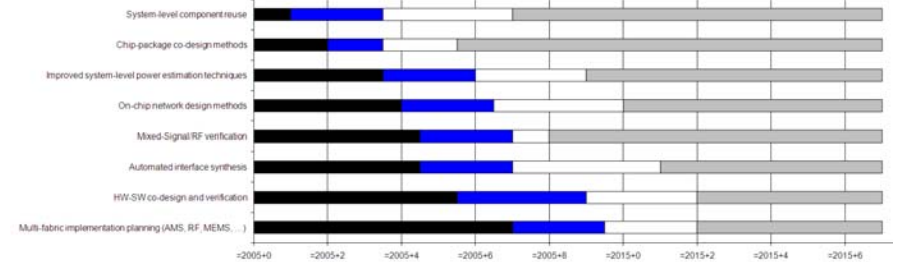
- More than Moore brings new set of requirements/solutions
 - Will create additional inventory of parameters

Existing

Existing requirements

| Table 14 | Year of Production | | 2005 | 2006 | 2007 | 2008 | 2009 | 2010 | 2011 | 2012 | 2013 | 2014 | 2015 | 2016 | 2017 | 2018 | 2019 | 2020 |
|------------------------------|--|---|------|------|------|------|------|------|------|------|------|------|------|------|------|------|-------|------|
| Technology Node | | | 90nm | 65nm | 45nm | 32nm | 28nm | 20nm | 16nm | 14nm | 12nm | 10nm | 7nm | 5nm | 3nm | 2nm | 1.5nm | 1nm |
| Design Reuse | | | | | | | | | | | | | | | | | | |
| 2 | Design block reuse | % to all logic size | 32% | 33% | 35% | 36% | 38% | 40% | 41% | 42% | 44% | 45% | 46% | 48% | 51% | 52% | 54% | 55% |
| Platform Based Design | | | | | | | | | | | | | | | | | | |
| 3 | Available platforms | Normalized to 100% sub-architecture | 52% | 51% | 67% | 63% | 75% | 70% | 80% | 85% | 88% | 89% | 91% | 93% | 94% | 97% | 98% | 99% |
| 4 | Platforms supported | % of platforms fully integrated/usable | 3% | 6% | 10% | 22% | 35% | 50% | 57% | 64% | 70% | 80% | 85% | 90% | 92% | 94% | 95% | 97% |
| High Level Synthesis | | | | | | | | | | | | | | | | | | |
| 5 | Factorial of high-level schemata (performance, area, power, cost) | % vs. measurements | 53% | 56% | 58% | 62% | 66% | 70% | 73% | 76% | 80% | 83% | 86% | 90% | 92% | 94% | 95% | 97% |
| Reconfigurability | | | | | | | | | | | | | | | | | | |
| 6 | FPGA reconfigurability | % of SOC accelerators | 23% | 26% | 28% | 28% | 29% | 28% | 28% | 32% | 42% | 49% | 48% | 50% | 53% | 56% | 60% | 62% |
| Analog Mixed Signal | | | | | | | | | | | | | | | | | | |
| 7 | Analog automation | % vs. digital automation | 12% | 14% | 17% | 17% | 24% | 24% | 27% | 30% | 32% | 35% | 38% | 40% | 43% | 46% | 50% | 52% |
| 8 | Modeling methodology, description languages, and simulation environments | % vs. digital methodology | 53% | 55% | 58% | 60% | 62% | 65% | 67% | 70% | 73% | 75% | 78% | 80% | 83% | 86% | 90% | 92% |

Existing solutions

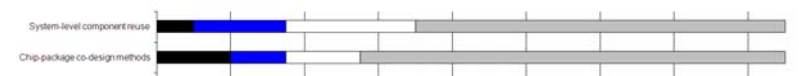


Additional

Additional requirements

| Requirement | 2005 | 2006 | 2007 | 2008 | 2009 | 2010 | 2011 | 2012 | 2013 | 2014 | 2015 | 2016 | 2017 | 2018 | 2019 | 2020 |
|---|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|
| 3.0 IP support for logic and other circuit reuse across multiple nodes for performance, cost, and measurement | 10% | 15% | 20% | 25% | 30% | 35% | 40% | 45% | 50% | 55% | 60% | 65% | 70% | 75% | 80% | 85% |
| 3.0 IP reuse on system performance, design, power, reliability, manufacturability, etc. | 10% | 15% | 20% | 25% | 30% | 35% | 40% | 45% | 50% | 55% | 60% | 65% | 70% | 75% | 80% | 85% |

Additional solutions



E.g.

- System-level (packaging)
- Circuit (inter-chip parasitics modeling/simulation)
- Layout (SiP global layout)
- DFM (package-chip, SiP DFM)

Design and System Drivers

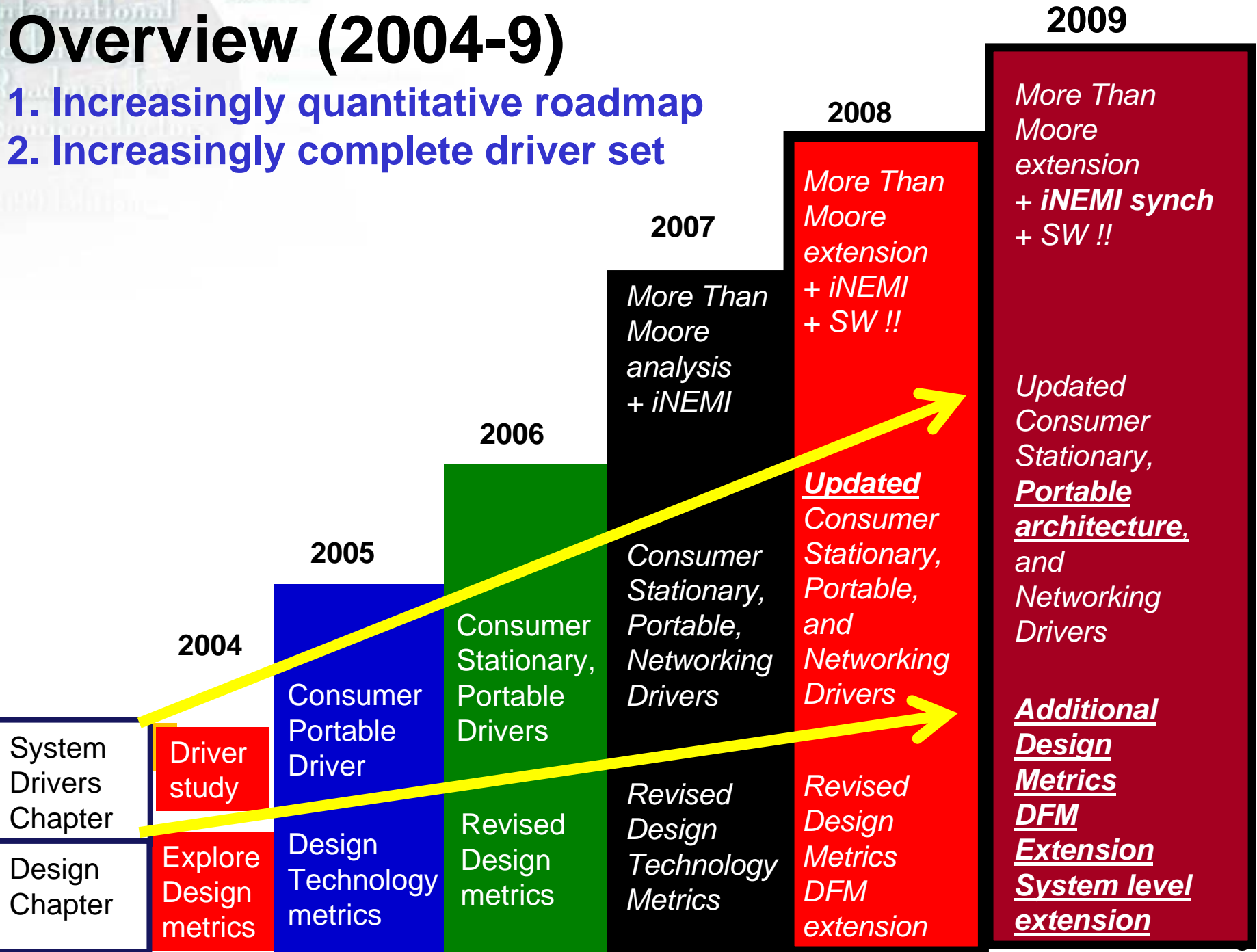
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Key messages:

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- 2. Updated key system drivers: SOC-Consumer Portable, MPU**
- 3. Frequency-power envelope remains critical for industry**
- 4. Continuing to broaden System Drivers, but more cautiously**
- 5. MtM brings new System Driver parameters, 2009 “SIP fabric”**
- 6. Expanded cross-TWG and public activity (DAC '09 workshop)**

Overview (2004-9)

- 1. Increasingly quantitative roadmap
- 2. Increasingly complete driver set

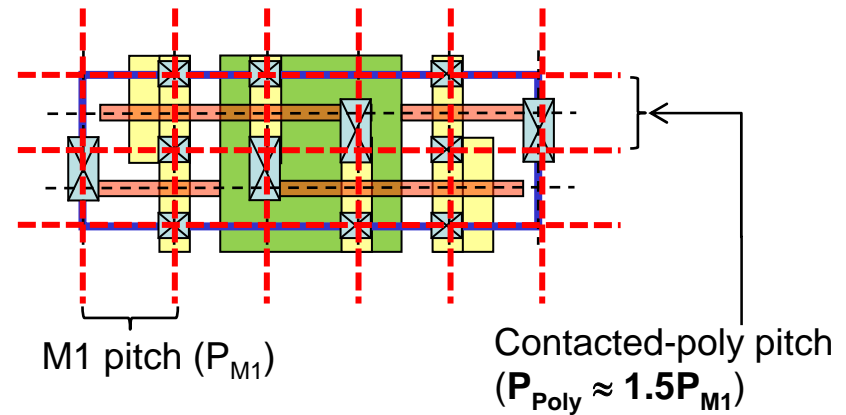
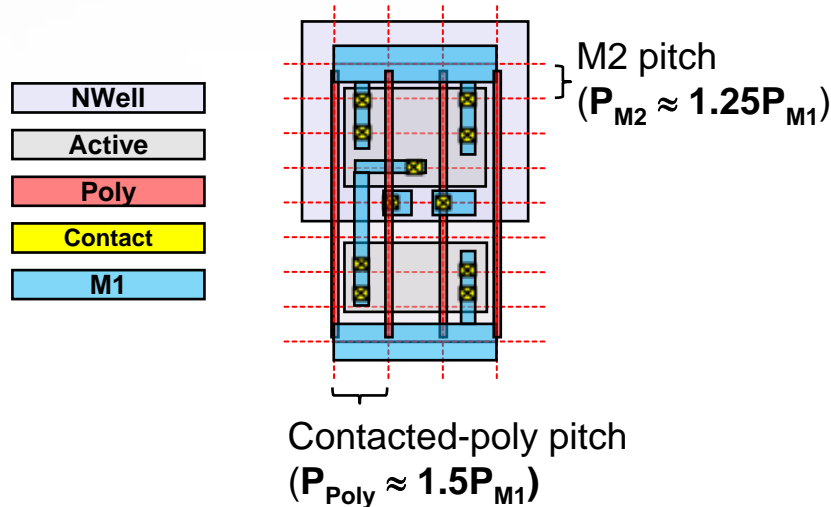


ORTCs: New A-Factor Models

(Area = A-factor $\times F^2$)

▪ Logic: A-factor = 175

▪ SRAM: A-factor = 60



NAND2 Area

$$\begin{aligned}
 &= 3 P_{Poly} \times 8 P_{M2} \\
 &\approx (3 \times 1.5 P_{M1}) \times (8 \times 1.25 P_{M1}) \\
 &= 45 (P_{M1})^2 \\
 &= 180 F^2 \rightarrow \mathbf{175 F^2}
 \end{aligned}$$

SRAM Bitcell Area

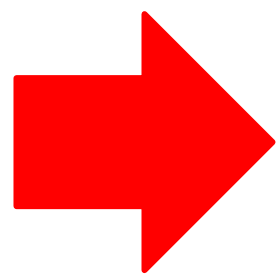
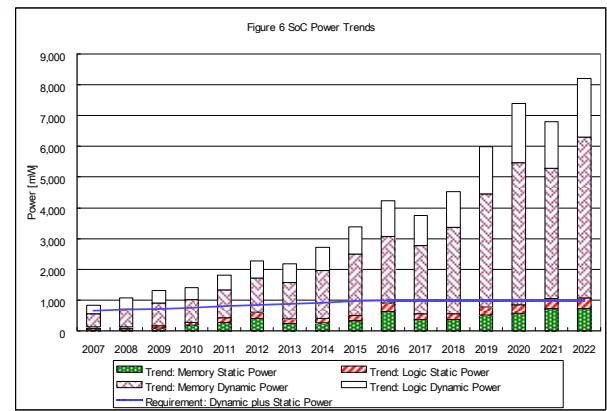
$$\begin{aligned}
 &= 2 P_{Poly} \times 5 P_{M1} \\
 &= 3 P_{M1} \times 5 P_{M1} = 15 (P_{M1})^2 \\
 &= 15 (2 F)^2 = \mathbf{60 F^2}
 \end{aligned}$$

Key System Drivers Constantly Updated

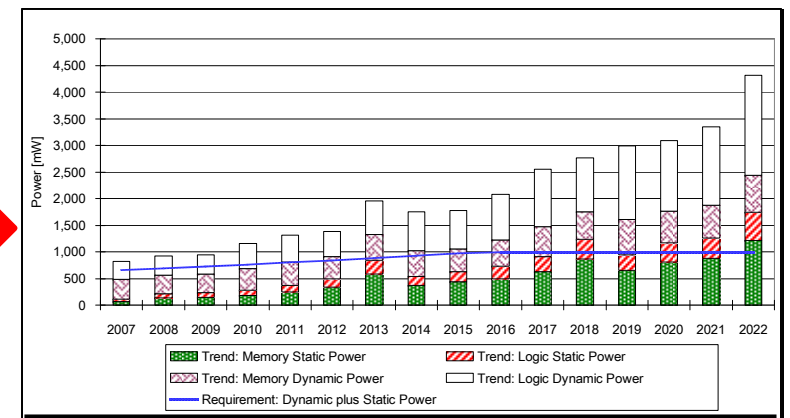
Consumer Driver Model

- **2008: Updated power model with realistic dynamic power**
 - Memory dynamic power 10X less than modeled previously

8 W max total (2022)



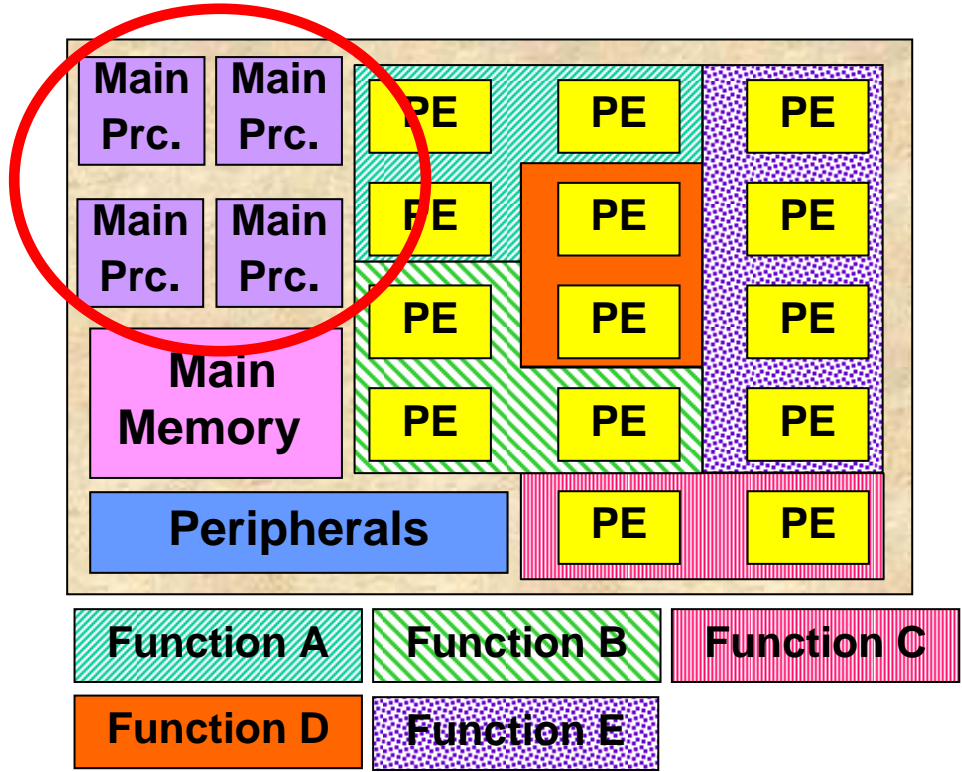
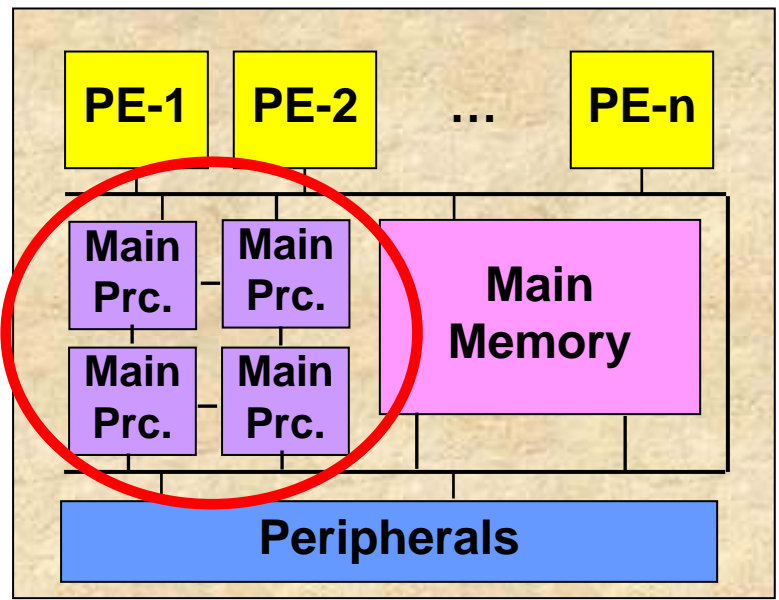
4.3 W max total (2022)



- **Will identify key driver requirements, explore coloring**
 - E.g., excessive power beyond portable limit (1 W)
- **Will explore RF/A/MS for future portable consumer drivers**
 - Extends existing driver (or, future “wireless” driver is possible)
- **Also ongoing: additional parameters per Test requests**
 - Upon provision of rationale/definition: Clocks, I/Os, currents, etc.

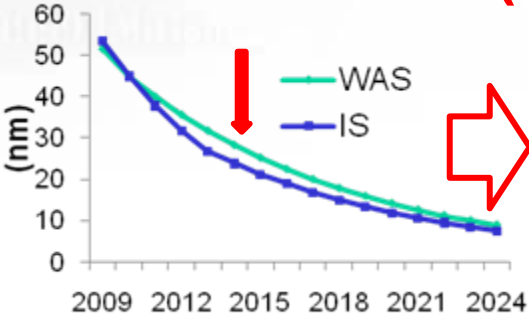
SOC Consumer Portable Architecture Model (updated)

- #Main Processors grows to 2, 4 and beyond
- Power budget reduced to 0.5W
- Die size reduces slowly to 44mm²



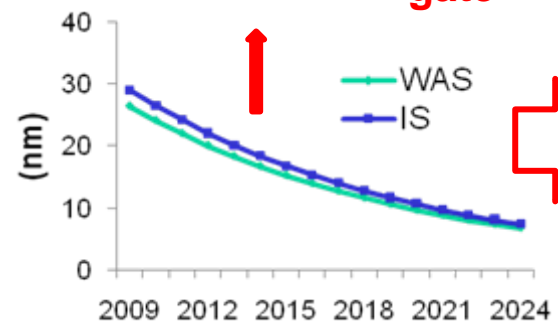
Updated MPU Density/Power/Frequency

M1 Half-Pitch (F)



Decrease P_{dyn} and P_{leak}

Physical L_{gate} (L)

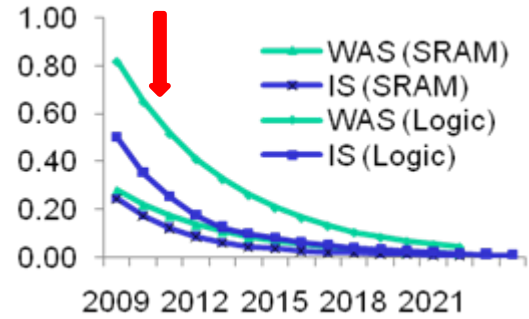


Increase P_{dyn} , decrease P_{leak}

A-Factor (A)

Logic: ~320 (WAS) → 175 (IS)
 SRAM: ~100 (WAS) → 60 (IS)

Unit cell size



Growth of #Tr
 2x / 3 year (WAS)
 → 2x / 2 year (IS)
 up to 2013

Die size reduction
 310mm² (WAS)
 → 260mm² (IS)

#core/die, #tr/core

12.2% / year (WAS)
 → 18.9% / year (~2013, IS),
 → 12.2% / year (2014~, IS)

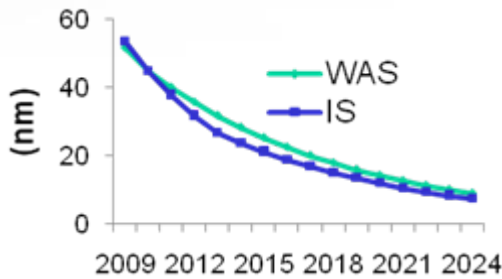
Increased P_{dyn} and P_{leak}



Design Pacing, Challenges Unabated

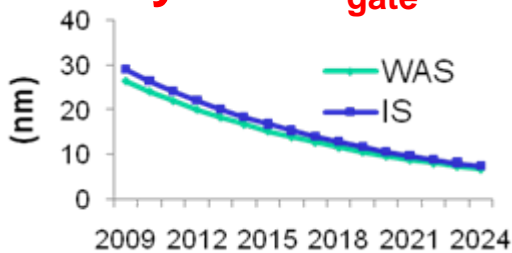
- 2009: Final Lgate and M1 HP scaling impact on Drivers

M1 Half Pitch

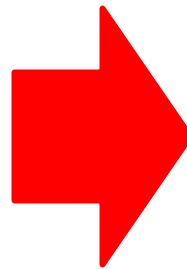


2 year delay, but faster scaling
 0.7x / 3yr → 0.7 / 2yr (~2013), 0.7x / 3yr (2014~)

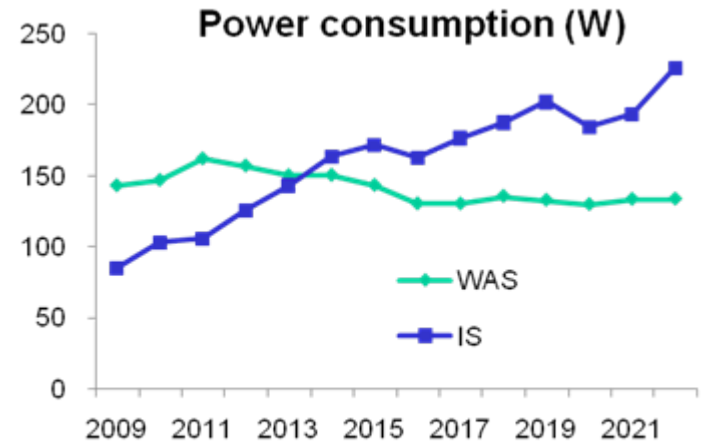
Physical L_{gate}



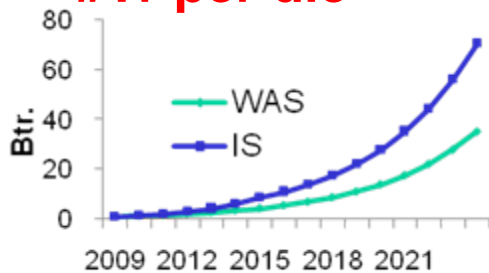
1 year shift



Updated MPU model (power)



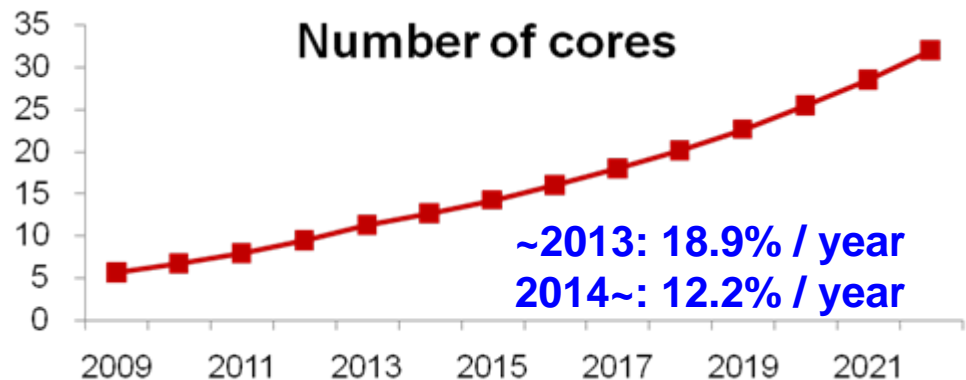
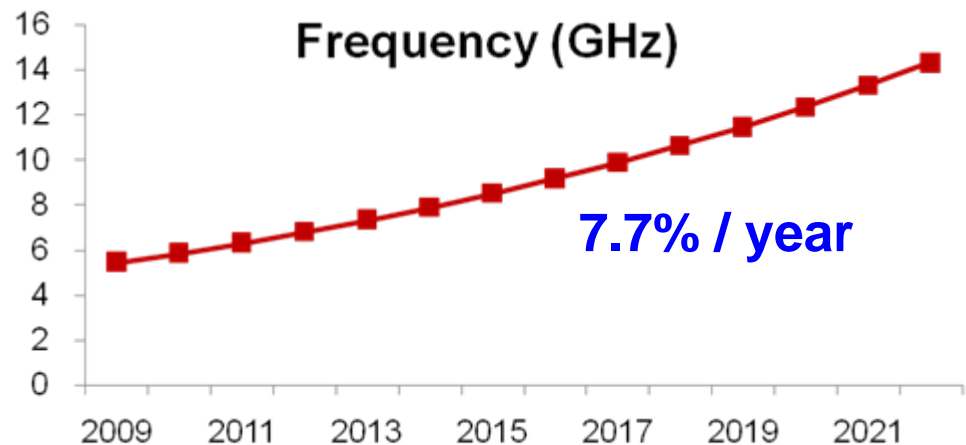
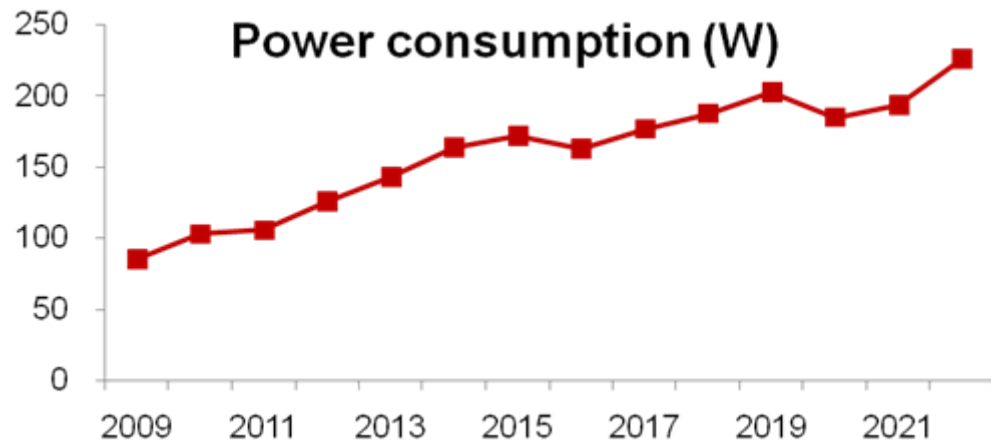
#Tr per die



New A-factors
 Faster M1 half pitch reduction

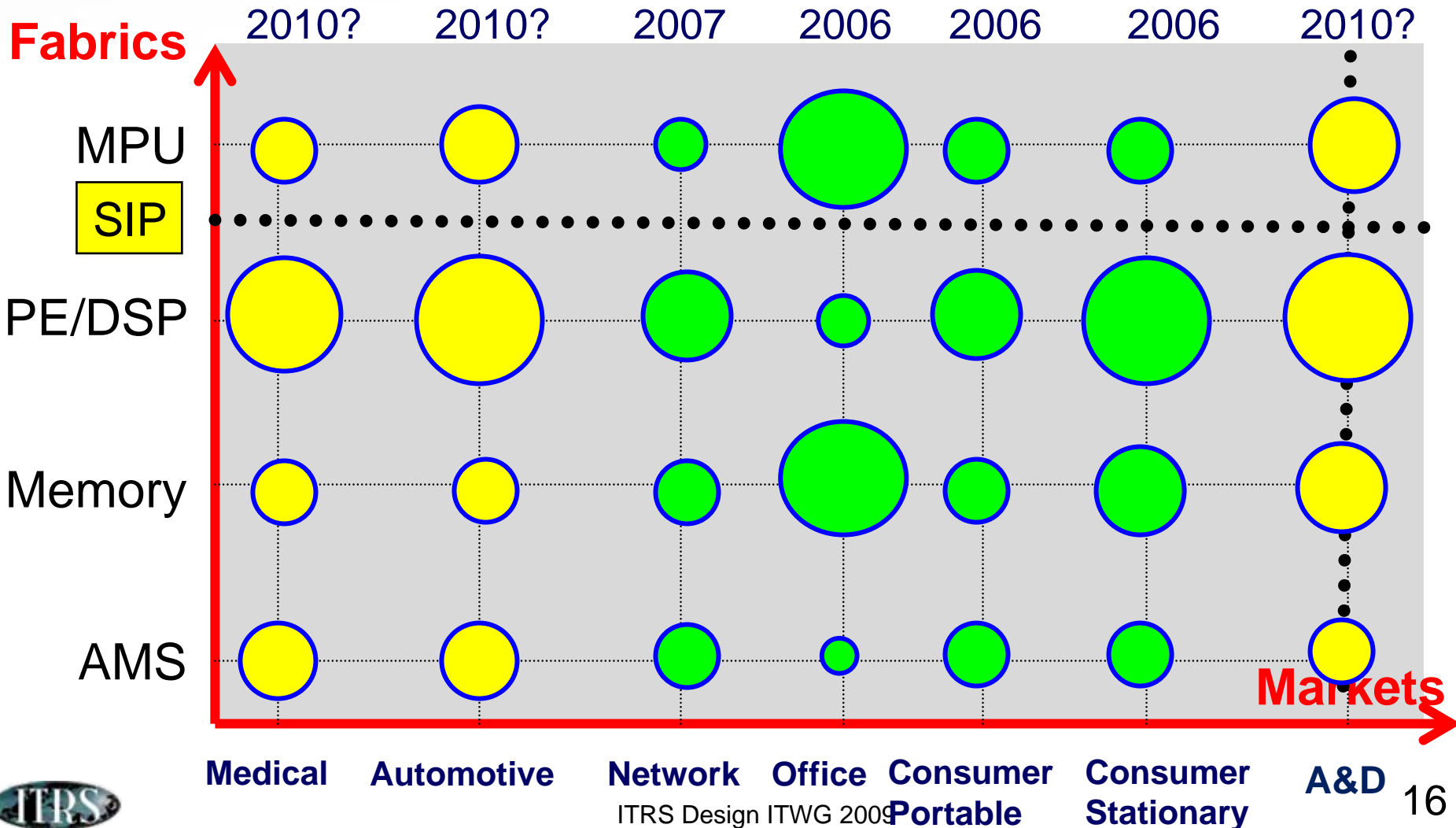
Frequency-Power Envelope Remains Critical System Issue

- Current priorities
 - Power #1 goal
 - Frequency slowdown
 - Multi-core enables tradeoff
- Need to track trade-off
 - Market vigilance
 - Yearly adjustment
 - Possible 2009 survey



New System Drivers? At the right pace...

- New SIP Fabric driver proposed, draft in 2009
- Others (aerospace & defense, medical, auto, FPGA) deferred



More Than Moore

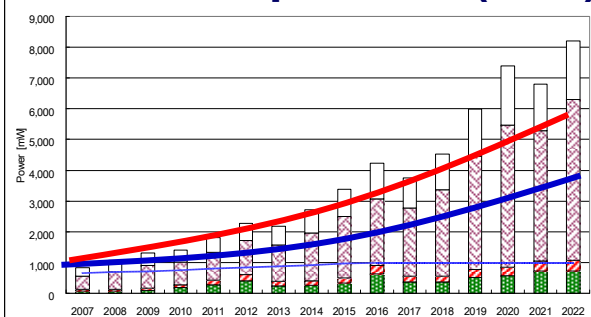
Brings Alternative Set of Parameters (2009-10)

- Will create additional inventory of parameters

CONCEPT: Current SoC scenario vs. Additional SiP scenario

System Drivers

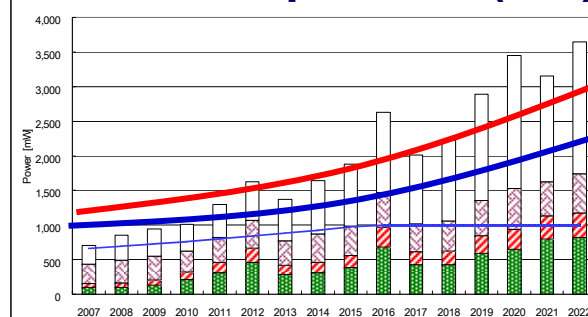
Consumer portable (SoC)



Power

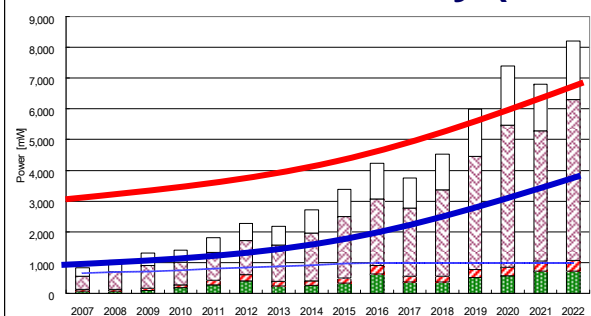
Normalized Cost

Consumer portable (SiP)



System Drivers

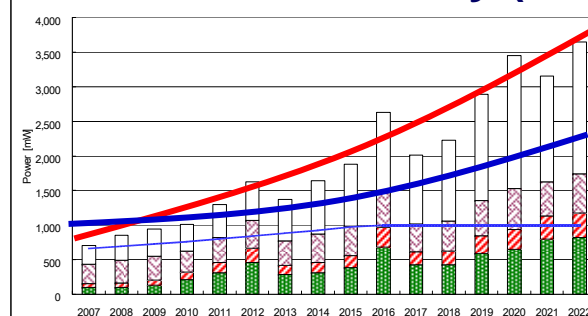
Consumer stationary (SoC)



Performance

Normalized Cost

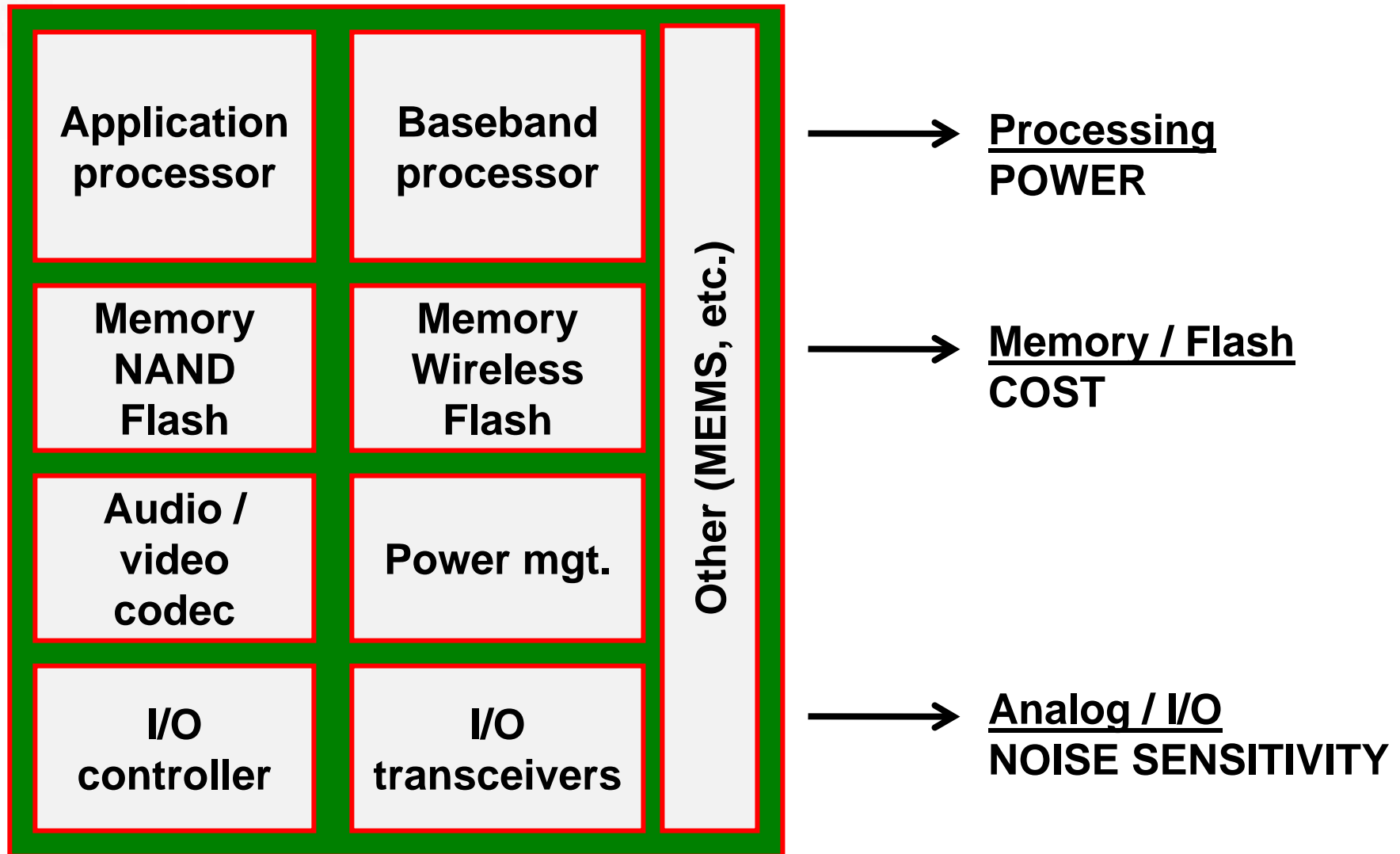
Consumer stationary (SiP)



System Drivers and iNEMI (2009)

Proposal to iNEMI: develop Portable System Architecture Template

New Chair with domain expertise – expect deeper commitment



Design & Key ITRS Cross-TWG Initiatives

- **With Interconnect (A&P):** 3D / TSV roadmapping survey
- **With PIDS, FEP, IRC:** Modeling and requirements support for CV/I → RO-based transistor metric
- **With CSTNSG:** Updated frequency, SRAM area, active area (yield) projects
- **With More Than Moore Study Group:** Definition of SIP-scenario System Driver roadmaps to complement existing SOC-scenario Driver roadmaps

DAC-2009 ROADMAPPING WORKSHOP SAN FRANCISCO MOSCONE CENTER MONDAY, JULY 27, 9AM - 3PM -- FREE!

Agenda Title / Topic

Welcome / Welcome to workshop, agenda

Plenary 1 The ITRS semiconductor industry roadmap

Plenary 2 The iNEMI roadmap

Session 1 How to Roadmap Electronic Design Automation
(panel)

Session 2 Roadmaps and Geographies

Summary

Design

1. Software, system level design productivity critical to roadmap
2. Design technology is key to variability / “sigma” control
3. System-level design technology is key to power efficiency
4. Design cost will be contained through innovation
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System Drivers

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