

International Technology Roadmap for Semiconductors



Assembly and Packaging 2009

San Francisco Conference July 15, 2008

Assembly and Packaging Technical Working Group Participants and Collaborators for 2009

81 Active participants

✓ *Representation from:*

- *Europe*
- *Japan*
- *Korea*
- *Taiwan*
- *United States*
- *Hong Kong*

✓ *Meeting in Beijing for input from China*

✓ *Active Collaboration with iNEMI and JISSO Roadmaps*

✓ *Joint Project with MIT Microphotonics Center*

Major Activities 2009

Revision made to single chip package categories

Previous Categories

Low-cost/hand held
Cost performance
High performance
Harsh



New Categories

Low-end, Low-cost
Mobile/Handheld
Memory
Cost performance
High performance
Harsh

Major Activities 2009

Expanded coverage of :

- Wafer Level Packaging
- Wafer thinning, singulation and bonding for 3D integration
- Optoelectronics
- Through silicon vias

Added coverage of:

- *Photovoltaics*
- *LEDs*
- *Power devices*

Automotive Packaging

<i>Metric</i>	<i>Specification</i>
<i>Automotive Maximum Temperatures (Ambient Temperatures)</i>	
Passenger Compartment Dashboard, panel	+85°C

The rapid growth in hybrid and electric vehicles brings an additional class of electronics and a new subset of environmental conditions that will be addressed in the 2009 Roadmap. This is not reflected in the 2008 table.

Operating Range	-40°C to 150°C
Typical Mission Profile	-40 to -20°C / 300h -20 to +20°C / 600h 20 to +130°C / 4000h 130 to +140°C / 1000h +150°C / 100h
Vibration	40g / 10–1000Hz (depending on customer)
Mechanical Shock	50g / 11ms (depending on customer)

Major Activities 2009

Major revisions to tables for:

- *Optoelectronics*
- *System in Package*
- *Wafer thinning*
- *Wafer level Packaging*
- *Wafer Stacking/3D integration*

Major Activities 2009

New tables for:

- Photovoltaics
- Power devices
- Packaging gaps and needs
- Optical Transceivers
- Packaging Consortia

New Materials will be required

Working with ERM the Needs have been identified

Many are in use today

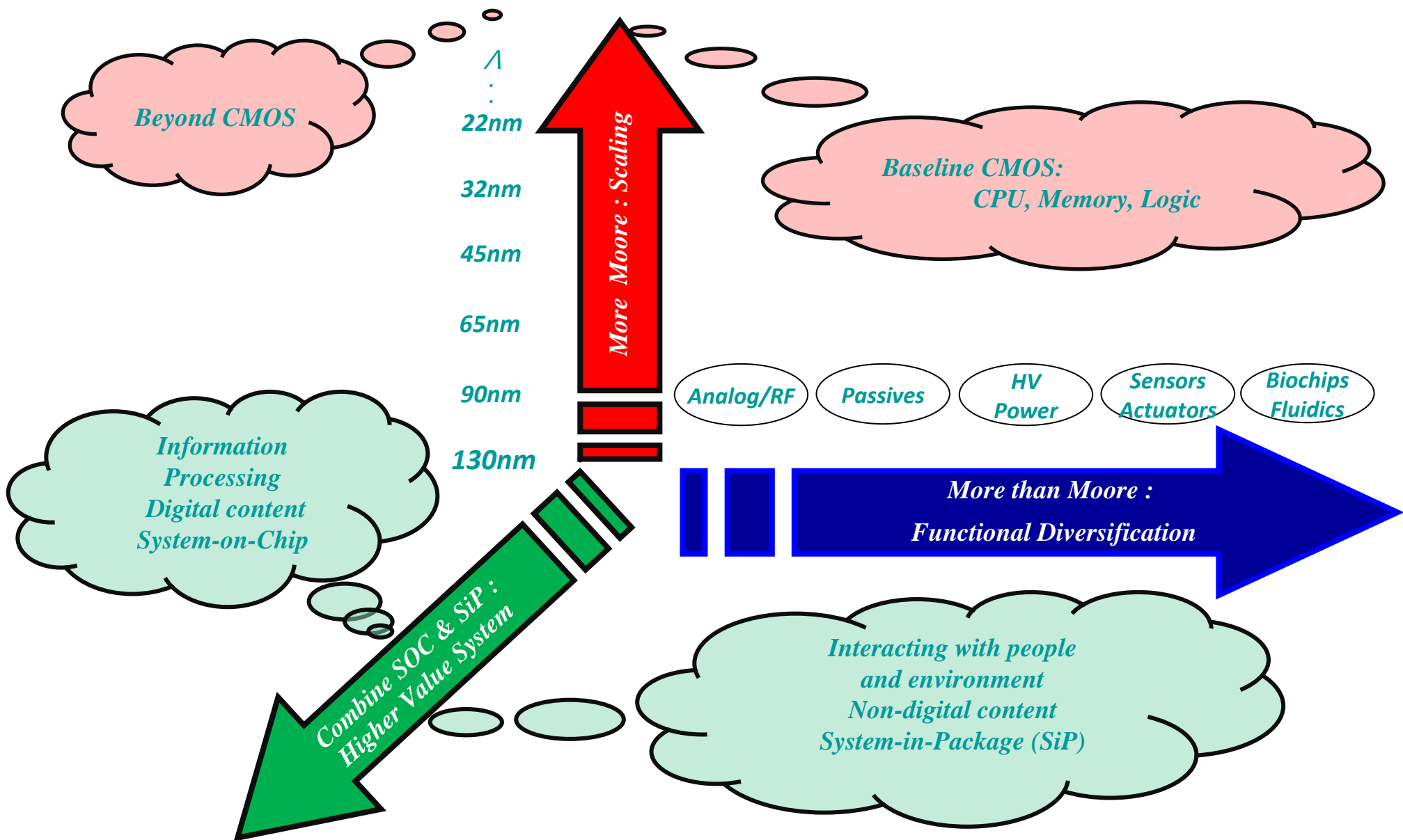
- **Cu interconnect**
- **Ultra Low k dielectrics**
- **High k dielectrics**
- **Organic semiconductors**
- **Green Materials**
 - Pb free
 - Halogen free

Many are in development

- *Nanotubes*
- *Nano Wires*
- *Macromolecules*
- *Nano Particles*
- *Composite materials*

But improvements are needed

Packaging enables More than Moore



Functional Diversification and “More than Moore” are driving rapid change in Packaging Technology

Everything is changing:

- **Architectures**
- **Materials**
- **processes**
- **equipment**

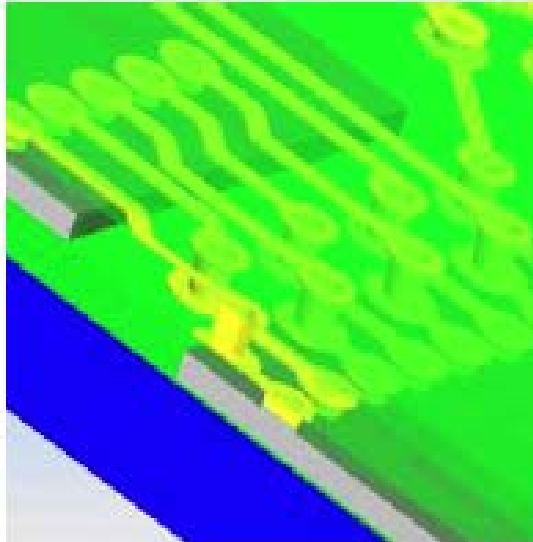
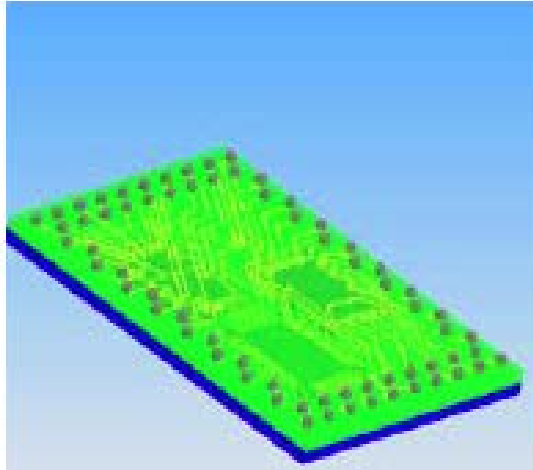
**ITRS Assembly and Packaging TWG
and MIT's Microphotonics Center
are Collaborating on 3D
Implementation of a Computing SiP**

*This project is intended to identify the
difficult challenges and potential solutions
for Complex 3D integration*

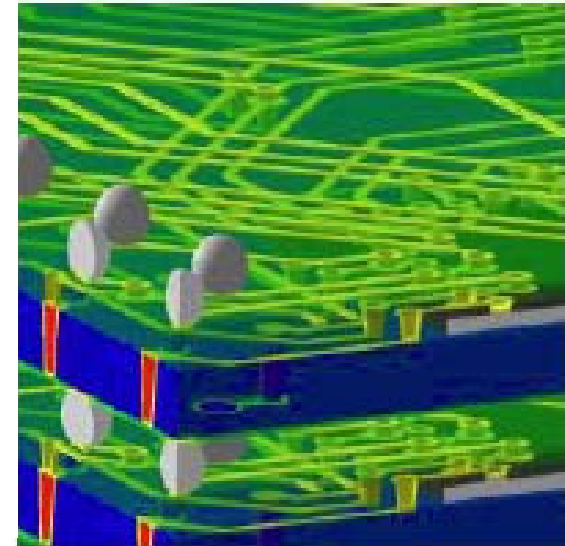
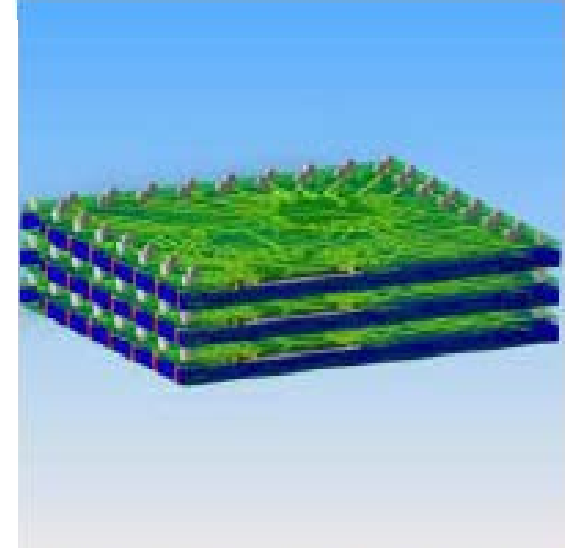
The Target is Tera-scale computing by 2015

- **Implementation of a 3D Integrated Computing SiP targeting Capability in 2015**
 - This Project illustrates the technical challenges for packaging posed by technology nodes below 45nm

The Design Parameters



<i>Target date for production:</i>	2015
<i>Number of Cores:</i>	100-1000
<i>Core transistor speed:</i>	10- 1GHz
<i>Electrical pins off-chip max:</i>	25GHz
<i>Optical connections per Package:</i>	1
<i>Power, ground and clock connections through substrate</i>	#TBD
<i>Total power per package:</i>	TBD
<i>Die size:</i>	
<i>Memory</i>	557mm²
<i>Logic</i>	310mm²
<i>Optical</i>	TBD
<i>Die thickness</i>	
<i>CPU:</i>	25um
<i>Memory:</i>	25um
<i>Total power per package:</i>	TBD
<i>Maximum power density:</i>	TBD
<i>Hot spot distribution:</i>	TBD
<i>Max. Junction temperature:</i>	~85°C
<i>Operating Voltage:</i>	400mV



Tera-scale Computing by 2015

Collaboration underway to identify challenges and define solutions

ITRS Technical working subgroups are addressing:

- TSV technology**
- Thermal management**
- Die to die bonding**
- Power integrity**
- SiP integration**
- Optical signaling**
- Package substrate requirements**

.....and more



Tera-scale Computing by 2015

The Roadmap says we can make the components:

- 3D memory stack with TSV interconnect
- 25GHz electrical signaling
- Microfluidic based thermal management
- 1000 core processor with 1 GHz clock?
- 100 core processor with 10 GHz clock?
- Stacked die multicore processor?
 - (10 die with 100 cores/die)
- 100Gbit memory die
- Optical transceivers at 1TB/S per channel

Assembly and Packaging TWG

