

# **ITRS Public Conference**

## ***Emerging Research Devices***

### ***2009 ERD Chapter***

- ***Emerging Memory Devices***
- ***Emerging Logic Devices***
- ***Emerging Architectures***

**Jim Hutchby – SRC**  
**July 15, 2009**

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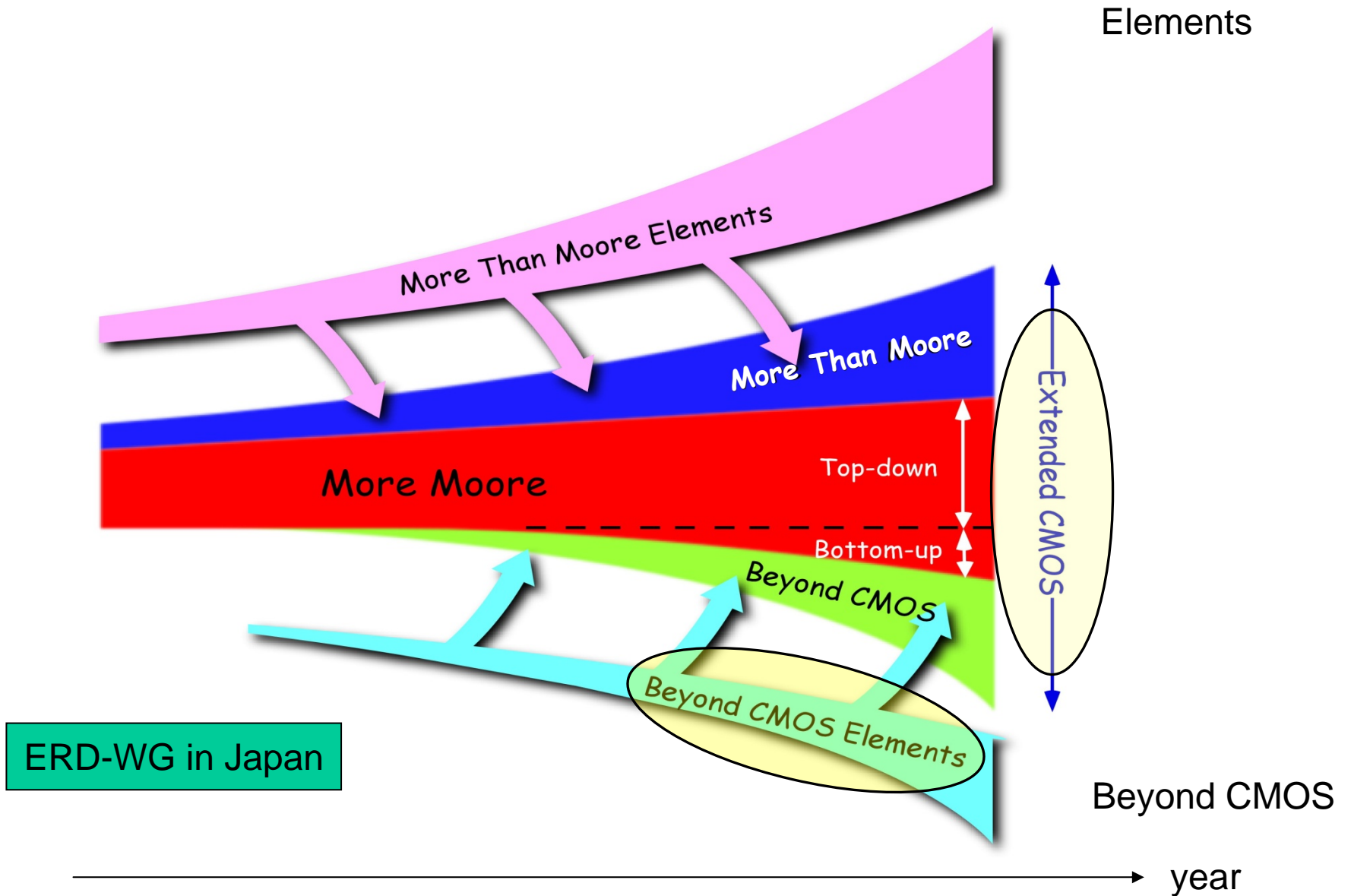
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# Evolution of Extended CMOS



# ***2009 ERD Chapter***

- Emerging Memory Devices***
- Emerging Logic Devices***
- Emerging Architectures***

# Memory Technology Entries

## Resistive Memories

- **Nanoelectromechanical**
- **Spin Transfer Torque MRAM**
- **Macromolecular (Polymer)**
- **Molecular Memory**

- **Electronic Effects Memory**
  - Charge trapping
  - Mott Transition
  - FE barrier effects

- **Nanothermal**
  - Thermochemical FUSE/Anti-FUSE
  - Nanowire PCM
- **Nanoionic Memory (Electrochemical)**
  - Cation migration
  - Anion migration

# Memory Technology Entries

## Resistive Memories

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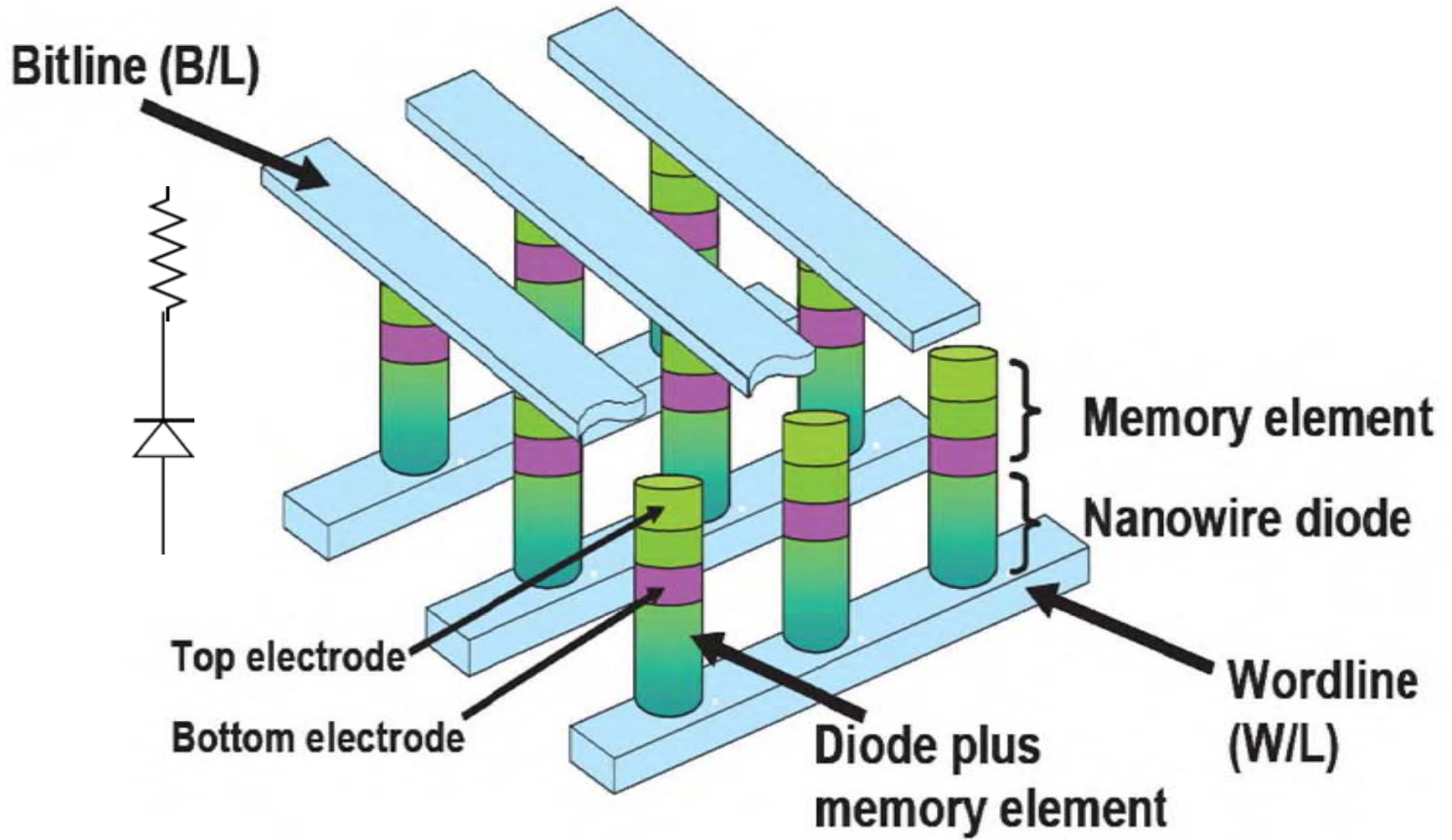
- **Electronic Effects Memory**
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- **Nanothermal**
  - Thermochemical FUSE/Anti-FUSE
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- **Nanoionic Memory (Electrochemical)**
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  - Anion migration

## Capacitive Memory

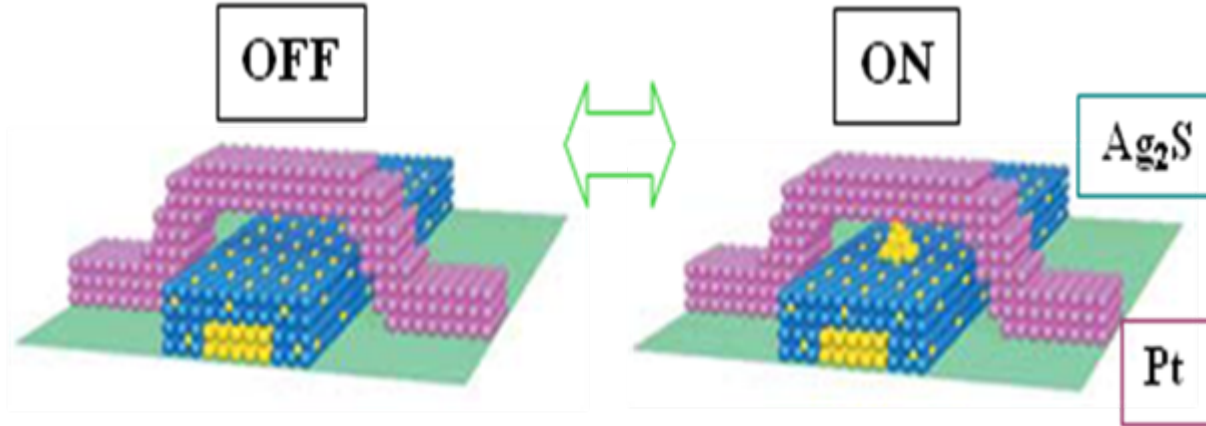
- **FeFET Memory**

# One Diode – One Resistor (1D1R) Memory Cell

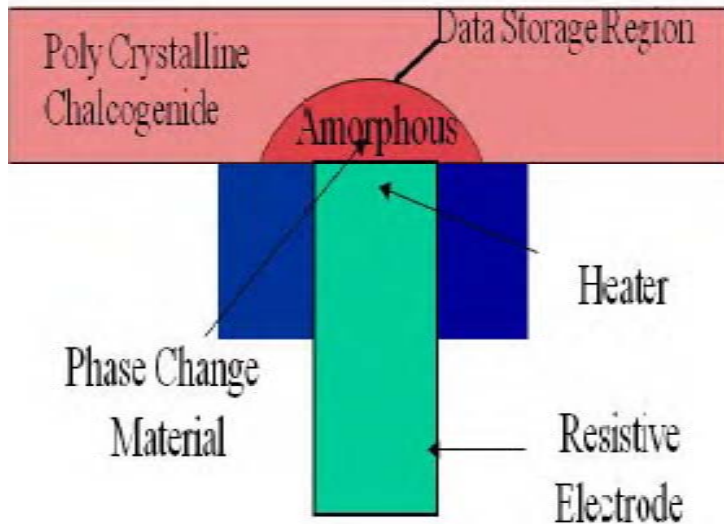


H-S. P. Wong – Stanford U.

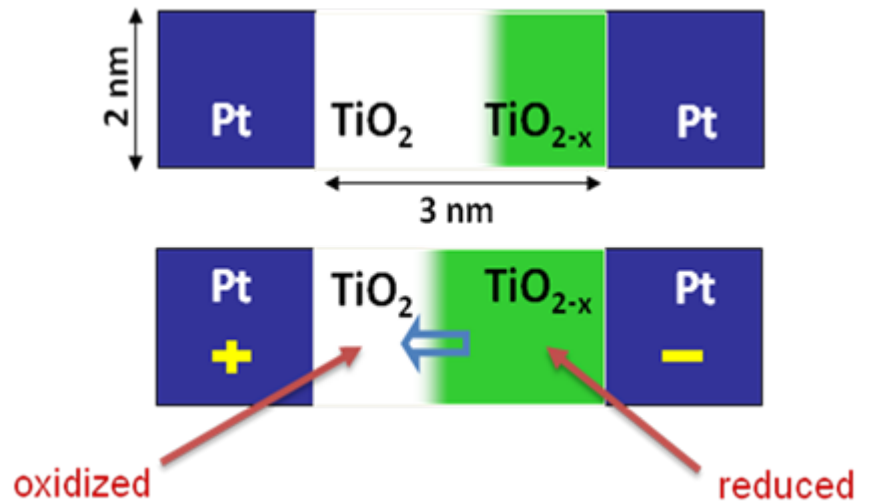
# Resistive Change Memory Cells



Electrochemical metallization or Atomic Switch



Phase Change Memory Cell



Nanoionic Memory Cell

# Content changes for Emerging Research Memory Section

- Recommend transfer of Engineered Tunnel Barrier Memory to PIDS and FEP
- Add Nano Wire Phase-Change Memory
- Add Spin Transfer Torque Magnetic RAM

# ***2009 ERD Chapter***

- ☐ Emerging Memory Devices***
- ☐ Emerging Logic Devices***
- ☐ Emerging Architectures***

# New Logic Technology Tables

Table 1 – MOSFETs  
Extending the Channel  
of MOSFETs to the  
End of the roadmap

---

CNT FETs  
Graphene nanoribbons  
III-V Channel MOSFETs  
Ge Channel MOSFETs  
Nanowire FETs  
Non conventional  
geometry devices

Table 2- Unconventional  
FETS, Charge-based  
Extended CMOS  
Devices

---

Tunnel FET  
I-MOS  
Spin FET  
SET  
NEMS switch  
Negative Cg MOSFET

Table 3 - Non-FET, Non  
Charge-based 'Beyond  
CMOS' devices

---

Collective Magnetic Devices  
Moving domain wall devices  
Atomic Switch  
Molecular Switch  
Pseudo-spintronic Devices  
Nanomagnetic (M:QCA)

# 2009 Logic Transition table

Technology	Status	Reason	Comment
<b>RTD</b>	<b>out</b>	<b>No viable logic functionality</b>	<b>Has been tracked for multiple revisions</b>
<b>Bi-layer tunneling devices</b>	<b>In</b>	<b>Significant theoretical work in NRI</b>	
<b>Band to band tunneling devices</b>	<b>In</b>		
<b>NEMS</b>	<b>In</b>		
<b>RSFQ</b>	<b>Possible future device</b>		

# III-V MOSFETs – Why Develop ?

Increase electron velocity and lower source/drain resistance:

$$I_d / W_g = qn_s v \quad I_d / Q_{transit} = v / L_g$$

InGaAs → lower  $m^*$  → higher velocity  
( mobility > 1000 cm<sup>2</sup>/V-s is sufficient)

Difficulties, hence research thrusts:

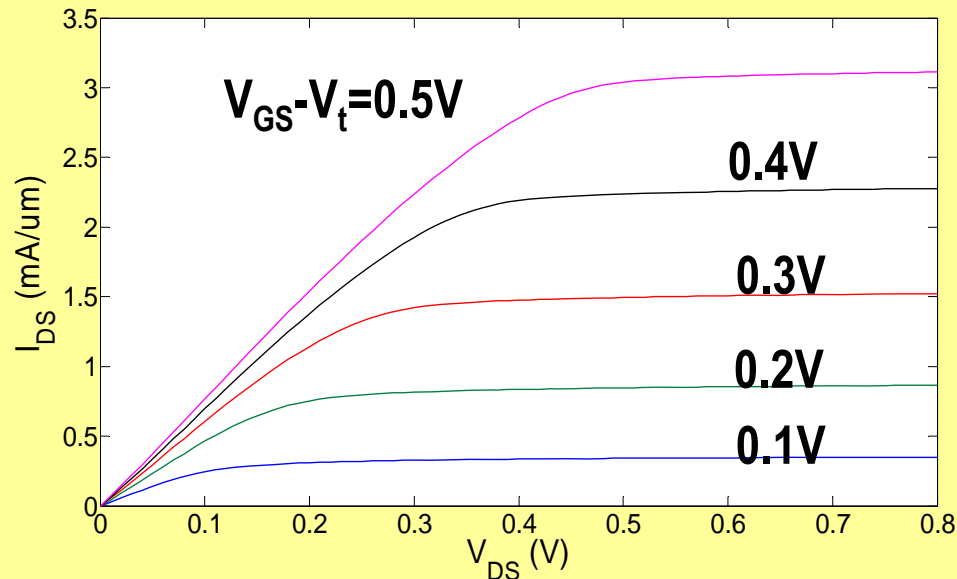
High-K dielectrics and III-V surface passivation

III-V growth on Si

VLSI-compatible MOSFET process flows

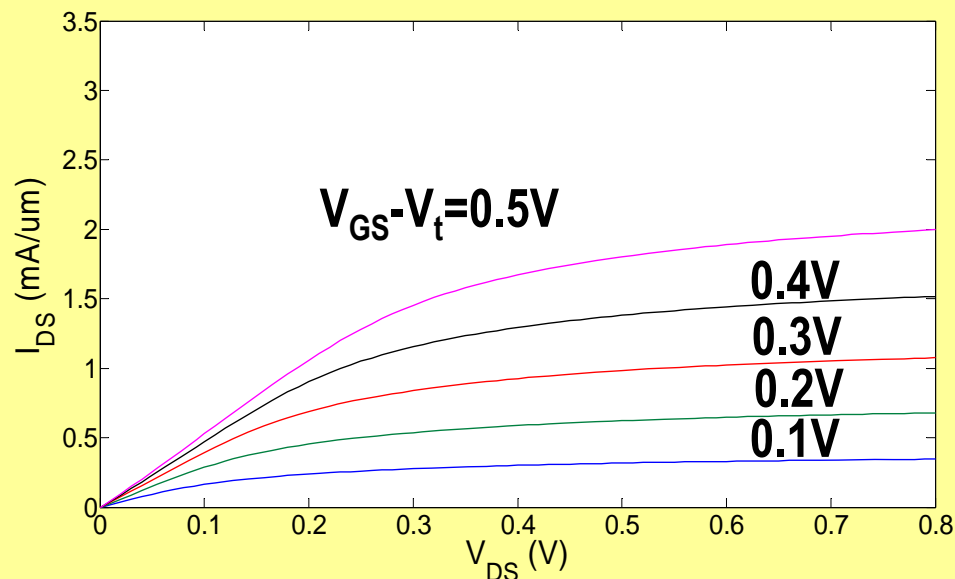
low  $m^*$  constrains vertical scaling, reduces drive current

# High Drive Currents are Feasible for InGaAs MOSFETs



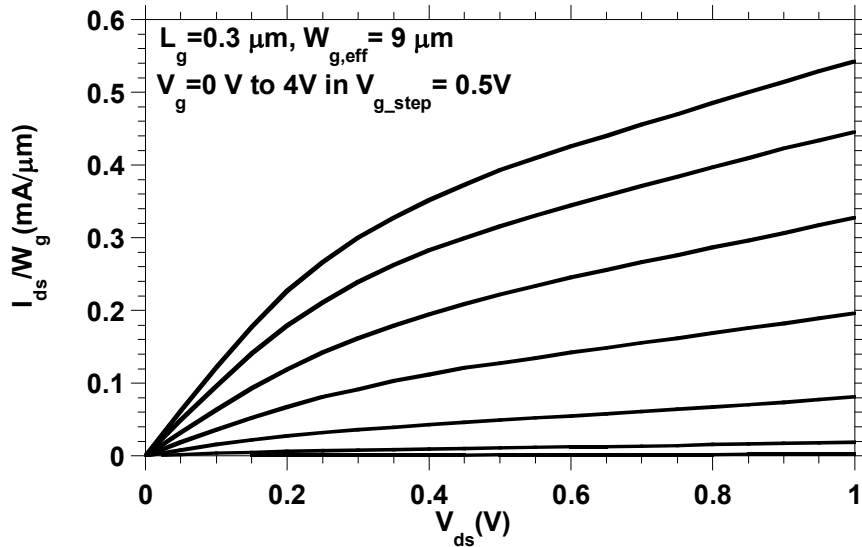
InGaAs  $\mu=1000 \text{ cm}^2/\text{V-sec}$   
 $R_s=R_d=20 \text{ Ohm um}$

- When taking into account finite mobility and series resistance, InGaAs is superior in terms of saturation current level  $I_{DSsat}$  and equivalent turn on resistance  $R_{on}$ .



Silicon  $\mu=200 \text{ cm}^2/\text{V-sec}$   
 $R_s=R_d=50 \text{ Ohm um}$

# III-V MOSFET Transistors – Experimental Results



*E-mode devices.*

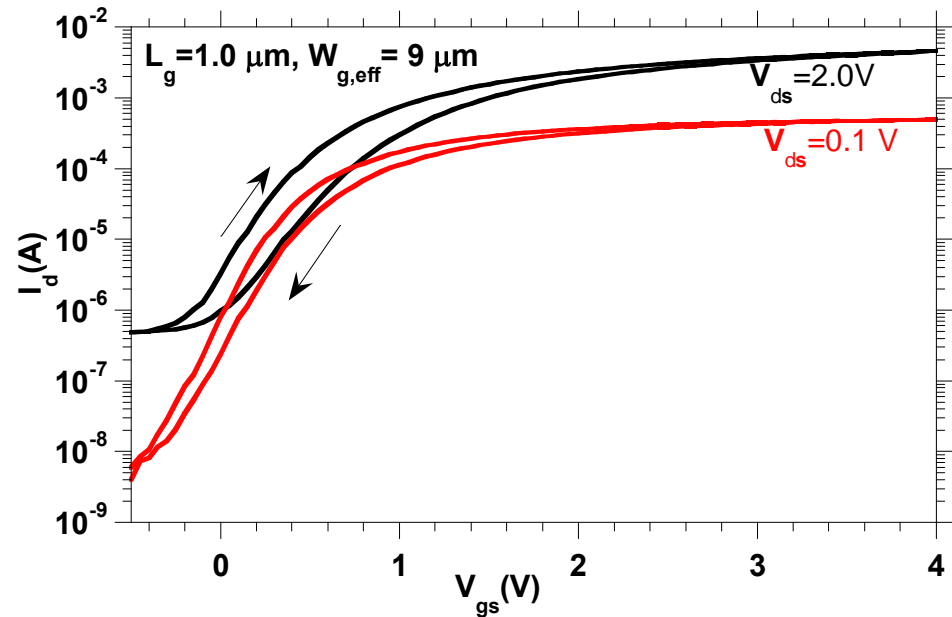
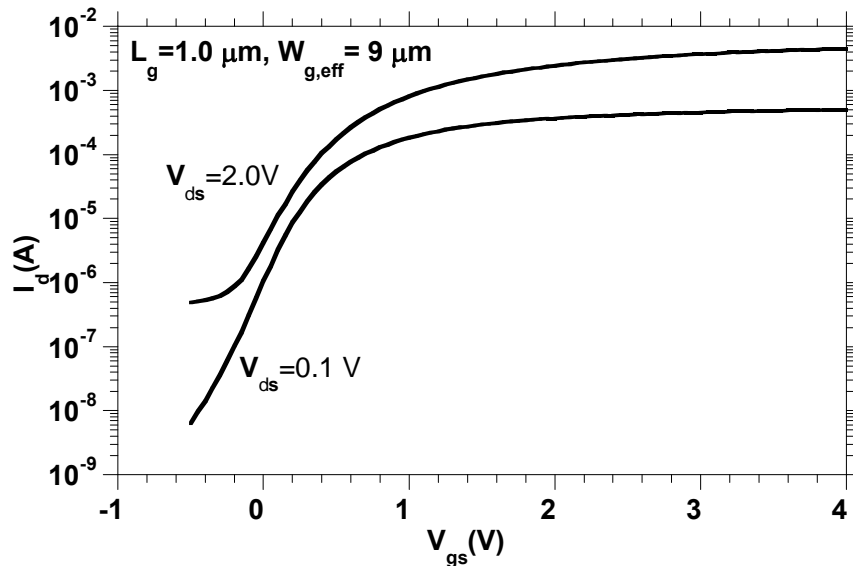
$g_m \sim 0.40 \text{ mS}/\mu\text{m}$ .

$\sim 270 \text{ mV/decade}$

*Low access resistance.*

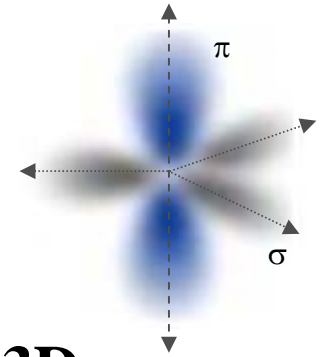
$g_m, I_d$  limited by  $D_{it}$ .

*Decapping problems on this run ?*



M. Rodwell UCSB

# Carbon-based Nanoelectronics



Atomic orbital  $sp_2$

0D

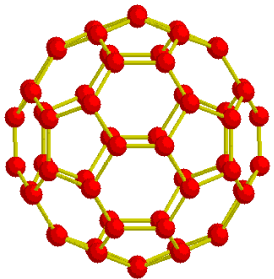
1D

2D

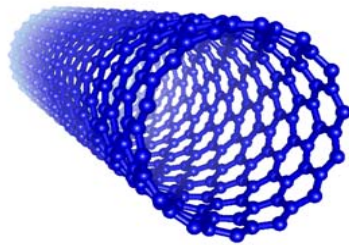
3D



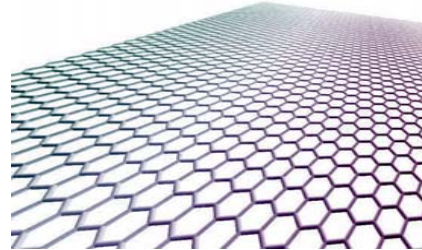
Fullerenes ( $C_{60}$ )



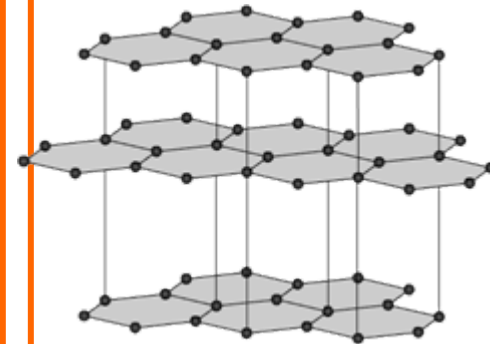
Carbon Nanotubes



Graphene



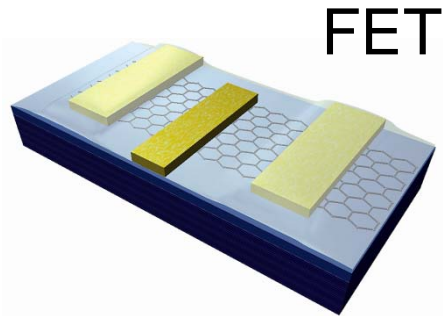
Graphite



P. Kim – Columbia U.

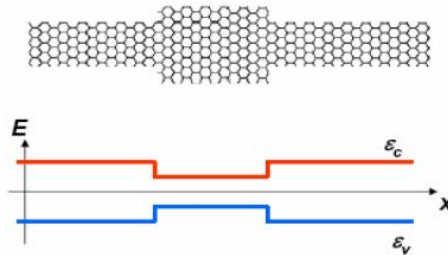
# Graphene Electronics: Conventional & Non-conventional

## Conventional Devices

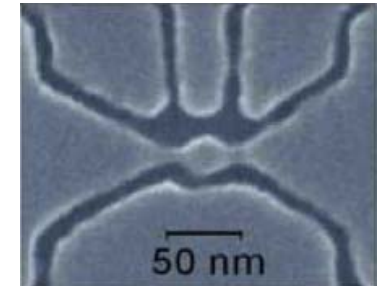


FET

Band gap engineered  
Graphene nanoribbons

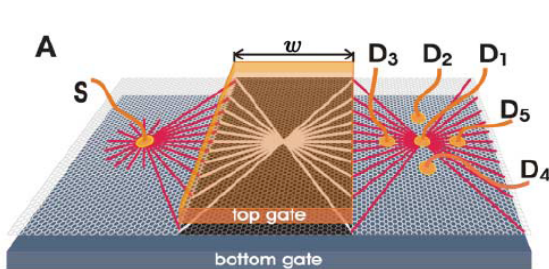


Graphene quantum dot



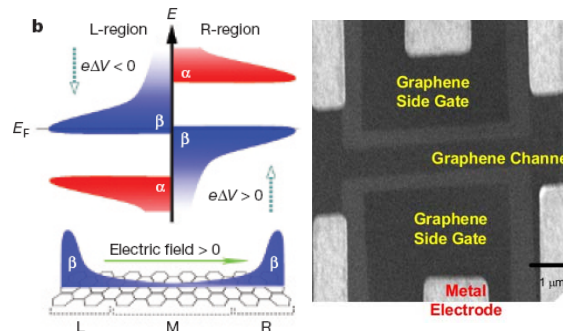
(Manchester group)

## Nonconventional Devices



Graphene Veselago lense

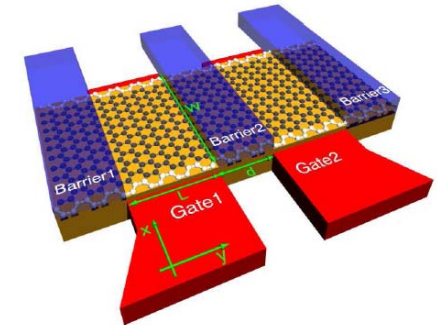
Cheianov *et al. Science* (07)



Graphene Spintronics

Son *et al. Nature* (07)

P. Kim – Columbia U.

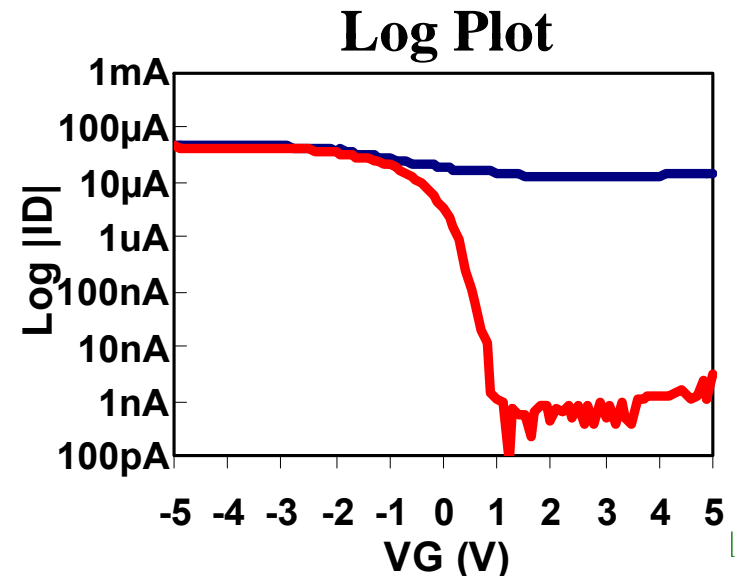
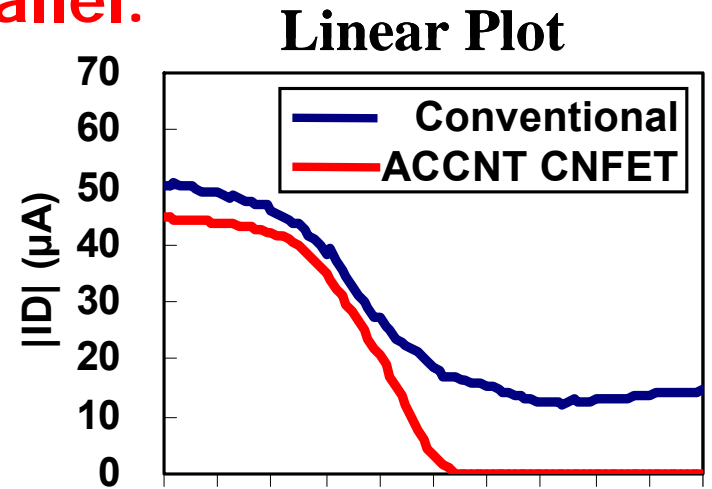
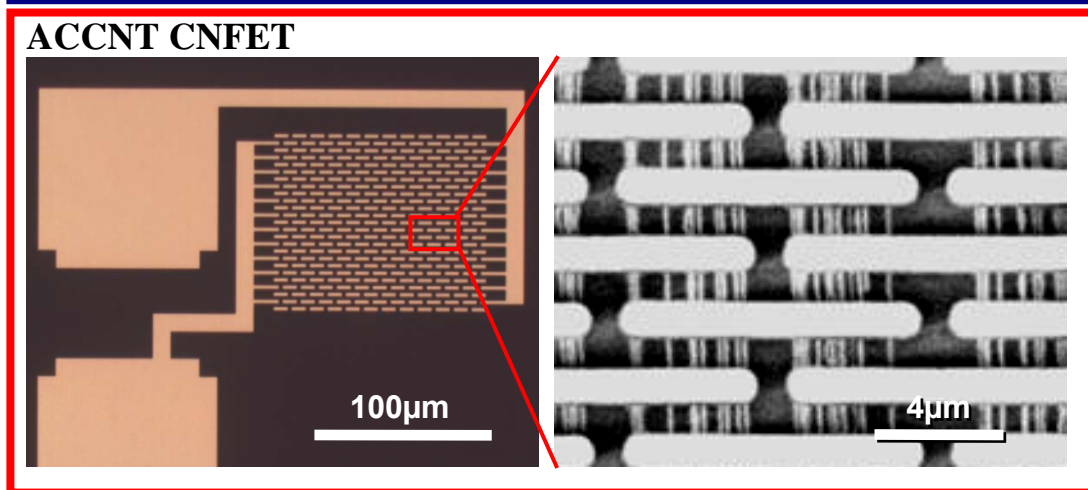
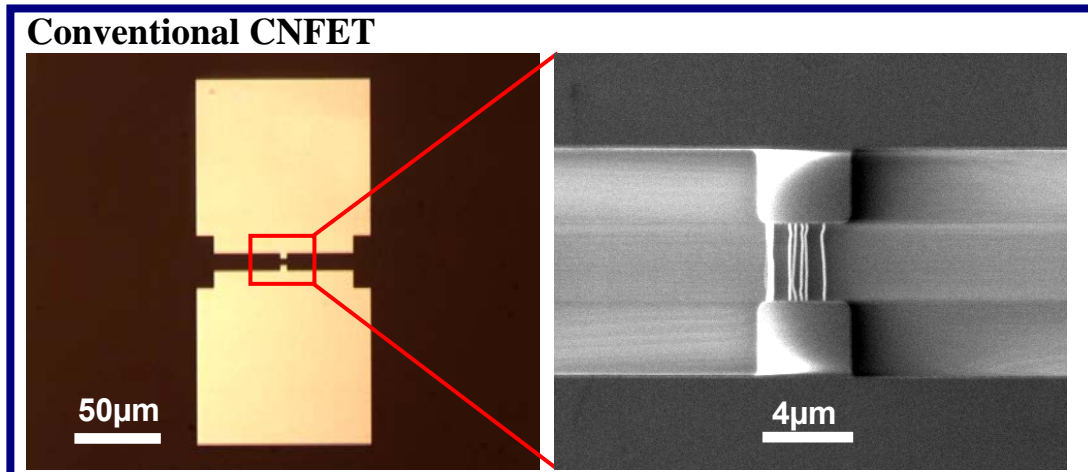


Graphene pseudospintronics

Trauzettel *et al. Nature Phys.* (07)

# ACCNT: A Comparison

- ACCNT:**  
Connect uncorrelated CNFETs in series; connect correlated rows/CNFETs in parallel.



# ***2009 ERD Chapter***

- Emerging Memory Devices***
- Emerging Logic Devices***
- Emerging Architectures***

# ***Emerging Architectures***

***Benchmarking***

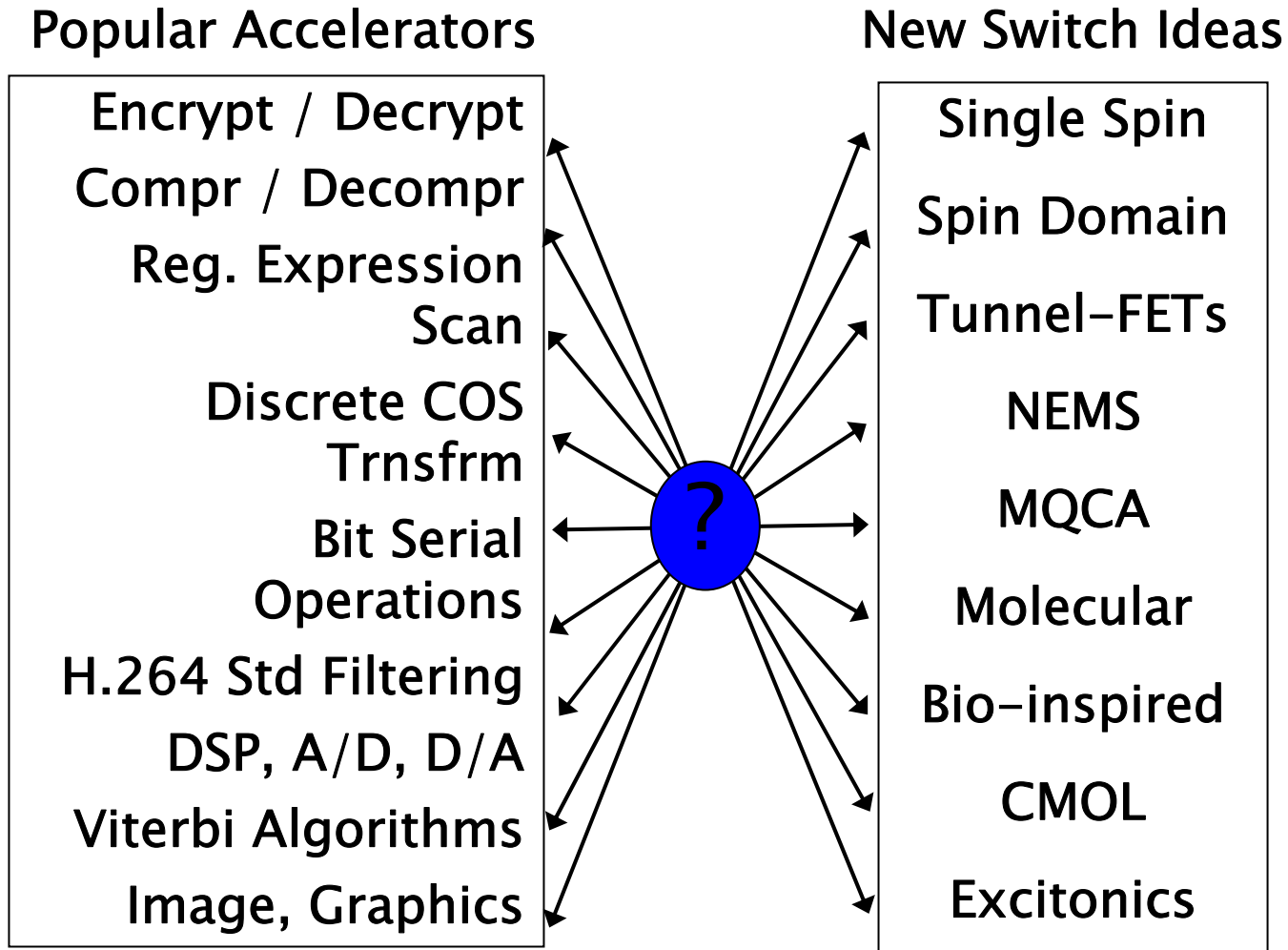
***Memory***

***Morphic (e.g. Architecture  
for Inference)***

# Four Architectural Projections

- 1) Hdwre Accelerators execute selected functions faster than software performing it on the CPU.**
- 2) Alternative switches often exhibit emergent, idiosyncratic behavior. We should exploit them.**
- 3) CMOS is not going away anytime soon.**
- 4) New switches may improve high utilization accelerators**

# Matching Logic Functions & New Switch Behaviors



# ***Emerging Architectures***

***Benchmarking***

***Memory***

***Morphic (e.g. Architecture  
for Inference)***

# Improving Memory Power Efficiency

## Critical Needs --

- **Reduced power SRAM replacements**
  - 45 nm L1 Cache: 3.6 pJ/bit
  - Note: re-architecting in 3D can save ~50%
  - What is the potential for an ERD to reduce to 0.3 J/bit?
- **Reduced power switched interconnect**
  - Esp. packet routed interconnect (NOC)
  - What is the potential for a memory-style ERD to be used for fast switchable interconnect?

# Memory Architecture

## Preliminary Observations

- For both General Purpose and Application Specific, the bottleneck is not in logic operations but in memory, communications, and reliability
- 3DIC creates new opportunity for algorithms and architectures that benefit from locality
- ERD could benefit from a 1R1D cell
  - 1 Resistor 1 Diode (1R1D) potentially as useful as 1 Resistor 1 Transistor (1R1T)
  - Gives better scaling

# ***Emerging Architectures***

***Benchmarking***

***Memory***

***Morphic (e.g. Architecture  
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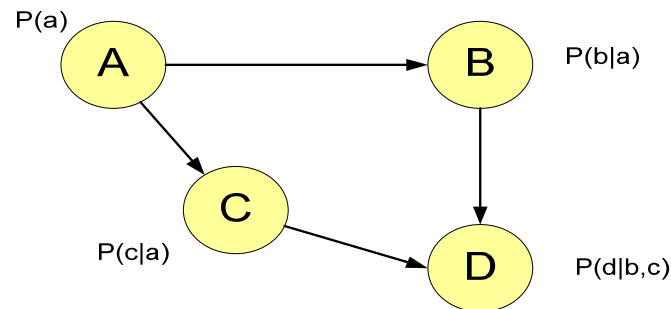
# Architecture by Inference

## Intelligent Computing

- Large class of problems that computers still do not solve well
- These problems involve the transformation of data across the boundary between the real world and the digital world
- They occur wherever a computer is sampling and acting on real world data, which includes almost all embedded computing applications
- These are difficult problems that require computers to find complex structures and relationships through space and time in massive quantities of low precision, ambiguous, noisy data
- Our lack of general solutions to these problems, outside of specialized niches, constitutes a significant barrier to computer usage and huge potential markets
- Traditional Rule Based Knowledge systems are now evolving into probabilistic structures where inference becomes the key computation, generally based on Bayes' rule

7/20/2009

- We now have **Bayesian networks**
- Bayesian nets express the structured, graphical representations of probabilistic relationships between several random variables
- **And the fundamental computation has become probabilistic inference**



$P(d b,c)$	$d_1$	$d_2$
$b_1, c_1$	0.5	0.5
$b_2, c_1$	0.3	0.7
$b_1, c_2$	0.9	0.1
$b_2, c_2$	0.8	0.2

# ERD – Key Messages

- ◆ Process for Technology Transfer to PIDS/FEP made explicit
- ◆ Logic Devices
  - ❖ New Logic Table structure defined to identify three device categories (1 – Extend CMOS; 2 – Charge-based Non-CMOS; 3 – Non-charge-based Beyond-CMOS)
  - ❖ New potential solution table for “Carbon-based Nanoelectronics”
- ◆ Memory Devices
  - ❖ Transfer Engineered Tunnel Barrier Memory to PIDS/FEP
  - ❖ A new taxonomy for categorizing resistive memories introduced.
  - ❖ STT RAM and Nano-wire PCM scaled beyond 15nm
  - ❖ STT RAM included in ERD to complement entry in PIDS/FEP
  - ❖ An assessment of new memory devices is underway.
- ◆ Architecture
  - ❖ New Architectural work for benchmarking “Beyond CMOS” devices
  - ❖ New Architecture section includes 1) memory architecture, 2) a new inference compute proposal, and 3) a conceptual thermodynamic method for evaluating architecture.