PIDS Summary

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Outline

- PIDS Scope and Sub-Categories
- 2009 Update Summary
  - Logic
  - Memory: DRAM
  - Memory: Nonvolatile
  - Reliability

- PIDS = **P**rocess **I**ntegration, **D**evices, and **S**tructures
- Scopes:
  - Provide physical and electrical requirements and solutions for sustaining IC performance scaling (performance = speed, density, power, functionality…)
  - On logic and memory devices:
    - Structures
    - Process-integration issues
    - Reliability

PIDS Sub-Categories

- Logic
  - HP = High Performance (μP…)
  - LOP = Low Operating Power (notebook…)
  - LSTP = Low Standby Power (cellular…)
- Memory
  - DRAM
  - Nonvolatile
- Reliability

2009 Update: Logic (Team Lead = Kwok Ng , Thomas Skotnicki, Hidekazu Oda)

- *CV/I* metric relaxed from 17% increase per year to 13%.
- The transition among bulk, FDSOI, multi-gate still needs to be worked out in the next few weeks (more details from FEP).
- Insertion of non-Si channel being considered. Has to satisfy
  1. Technology is ready.
  2. Si cannot keep pace in *CV/I*, but non-Si can.
- MASTAR updated to include III-V materials.

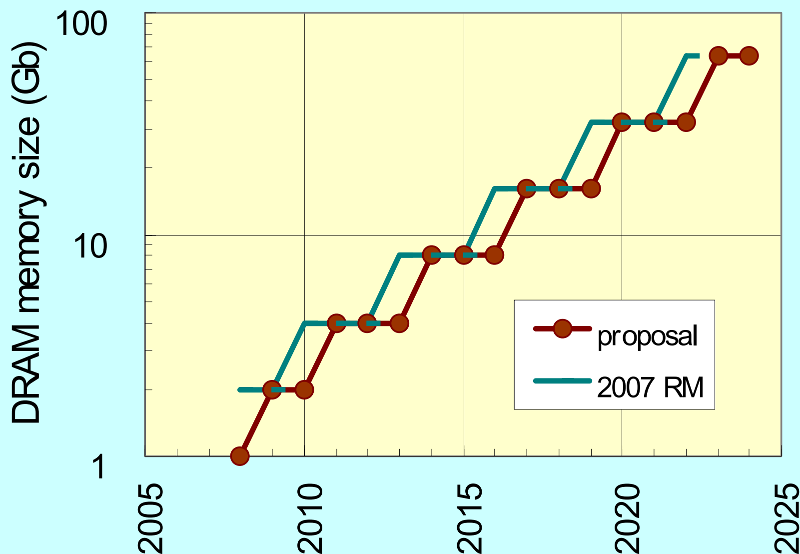
2009 Update: Logic (cont'ed)

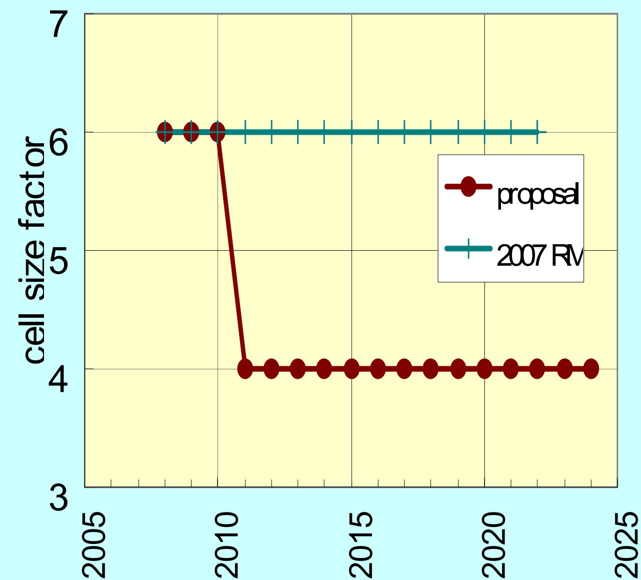
- Add new metrics that are relevant to circuit performance:
  - Add p-MOSFET performance (n-channel/p-channel current and capacitance ratios).
  - Add ring-oscillator delays (FO=1 & FO=4, in addition to CV/I).
  - Access resistance R_{acc} specs tightened (35% I_{sat} degradation as opposed to 40-50%).

- I_{off} = 100 nA/um (as opposed to 200-700 nA/um) for HP.

2009 Update: DRAM (Team Lead = Shizuo Sawada)

- Cell factor – $4F^2$ cell in 2011.
- DRAM product size 1 yr delay from ITRS 2008 (4Gb in 2011)





2009 Update: Nonvolatile Memory (Team Lead = Rich Liu, Hirofumi Inoue)

- NAND flash:
  - NAND half-pitch, pull-in 1 year from ITRS 2008, i.e. 32 nm in 2010.
  - FG-to-CTF transition in 2012, delay 2 years.
  - 3D-CTF in 2014, delay 1 year.
  - 3 bit–4bit/cell transition delays 2 years (2012).
- NOR Flash gate length and node scaling slows down to reflect product reality.
- Update non-charge-based NVM requirements:
  - STT (spin torque transfer) MRAM added
  - PCRAM (phase change RAM) updated to reflect recent product reality
  - FeRAM scaling pace also slows down to reflect product reality.

2009 Update: Reliability (Team Lead = Charles Cheung)

- Update reliability requirements to the extent allowed by time limits in 2009.
- Reliability requirements that need extensive revision of roadmap will be updated in 2010.
- Increase emphasis on circuit impact of device reliability issues.

2009 Update: Reliability (cont'ed)

- Emphasis:
  - The impact of faster pace of new material/structure introduction while shortening technology cycle.
  - The impact of variability on reliability assurance.
  - The need for extreme reliability in many new market driving applications – automobile, medical devices, ….
  - The reliability challenge of integrating sensor/actuator on CMOS platform.
  - The challenge of testing enough samples for reliable lifetime projection.
  - The need for circuit-aware reliability assessment.
  - The need for reliability-aware fault-tolerant design.