ITRS - YE ITWG

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L. Pfitzner, lothar.pfitzner@iisb.fraunhofer.de

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Organization of the Chapter 2009

- **Chair:** Lothar Pfitzner (Fraunhofer IISB)
  Co-Chair: Dilip Patel (SEMATECH)

- Difficult Challenges
    - Table YE 2
- Technology Requirements and Potential Solutions
  - Yield Learning (YL – no tables)
    - Chair: N.N.
  - Yield Model and Defect Budget (YMDB)
    - Chair: Sumio Kuwabara (NEC) - Japan
    - Table YE 3, YE 4, YE 5,
  - Defect Detection and Characterization (DDC)
    - Chair: N.N.
    - Table YE 6, YE 7, YE 8
  - Wafer Environment Contamination Control (WECC)
    - Chair: Kevin Pate (Intel) – USA, Andreas Neuber (AMAT) - Europe
    - Table YE 9

2009 YE ITWG Contributors (to be revised)

Europe

Ines Thurner (DDC; Qimonda)
Lothar Pfitzner (Chair; Fraunhofer IISB)
Andreas Nutsch (DDC; Fraunhofer IISB)
Andreas Neuber (WECC; Applied Materials**)**
Benoit Hirschberger (DDC; ST)
Astrid Gettel (WECC, GLOBALFOUNDRIES)
Jan Cavelaars (DDC; Crolles 2/ NXP)
Dieter Rathei (YMDB; DR Yield)
Francois Finck (DDC/YMDB; ST)
Christoph Hocke (WECC; Infineon)
Francesca Illuzzi (WECC; ST)
Hubert Winzig (WECC; Infineon)
Matthias Pfutterer (WECC, M+W Zander)
Michael Lurie (WECC; Tower)
Michael Otto (WECC; Fraunhofer IISB)
Jean-Marie Collard (WECC, Solvay)
Jochen Ruth (WECC, PALL)
Guillaume Gallet (WECC, Camfil)

Japan

Fumio Mizuno (DDC; Meisei Univ.)
Masakazu Ichikawa (DDC; Tokyo Univ.)
Isao Kojima (DDC; AIST)
Eiichi Kawamura (DDC; Fujitsu)
Yoshinori Nagatsuka (DDC; SEIKO-EPSON)
Koichiro Saga (WECC; Sony)
Koichi Sakurai (DDC/YMDB; Renesas)
Kazuo Nishihagi (WECC; Horiba)
Ken Tsugane (WECC; Hitachi)
Masahiko Ikeno (DB&YM; Hitachi HT)
Sumio Kuwabara (DB&YM; NEC EL)
Takanori Ozawa (YL/YMDB; Rohm)
Yoko Miyazaki (DDC; Accretech)
Yoshimi Shiramizu (WECC; NEC EL)
Yuichiro Yamazaki (DDC; Toshiba)
Ryu Shioda (YL, Agilent)
Katsunobu Kitami (WECC, Kurita)
Takahiko Hashidzume (DDC, Panasonic)
Kazuhiro Honda (DDC; JEOL)
Takashi Futatsugi (WECC; Organo)

Korea

Uri Cho (; Samsung)
Hyun Chul Baek (; Hynix)
Sang KyuPark (; Magna Chip)

Taiwan

Tings Wang (YL; Promos)
CS Yang (Winbond)
CH Chang (; SIS)
ChanYuan Chen (; TSMC)
CS Yang (; Winbond)
Jim Huang (; UMC)
Jimmy Tseng (; PSC)
Len Mei (; Promos Tech)
Steven Ma (; Mxic)

Thank you very much!

United States

Dilip Patel (Co-chair, DDC, Intel)
Kevin Pate (WECC, Intel)
J. Ritchison (DDC; TI)
James Dougan (DDC; Freescale)
Allyson Hartzell (WECC; Exponent)
Barry Gotlinsky (WECC; Pall)
Bart Tillotson (WECC; Fujifilm Electronic Materials)
Bob Latimer (WECC; Hach Ultra)
Chris Muller (WECC; Purafil)
Dan Fuchs (WECC, Air Liquide)
Dan Wilcox (WECC; Spansion)

United States (cont.)

Dave Roberts (WECC; Nantero)
David Blackford (WECC, FMT)
Dimitry Znamensky (WECC;)
Drew Sinha (WECC, SUMCO)
Dwight Beal (WECC, PMS)
James McAndrew (WECC; AirLiquide)
Janice Edler (WECC, IBM)
Jeff Chapman (WECC; IBM)
Wai->ming Choi (WECC; Mykrolis)
Jill Card (, Exponent)
John Degenova (WECC; TI)
John Kurowski (WECC; IBM)
Jonathan M. Myers (WECC, IBM)
Joseph O'Sullivan (WECC; Intel)
Keith Kerwin (WECC; TI)
Kosei Matsumoto (WECC, Kurita)
Luke Lovejoy (WECC; Freescale)
Mark Camenzind (WECC; Air Liquide)
Mark Crockett (WECC; Applied Materials)
Rajat Agrawal (WECC;)
Rick Godec (WECC, GE)
Rick Udischas (WECC; Ais Liquide)
Biswanath Roy (WECC; Pall)
Sarah Schoen (WECC; Air Liquide)
Slava Libman (WECC; M+W Zander)
Scott Anderson (WECC; Air Liquide)
Scott Covington (WECC, Kurita)
Steve Hues (WECC; Micron Technology)
Terry Stange (WECC; Hach Ultra)
Tony Schleisman (WECC; Air Liquide)
Tracey Boswell (WECC; Sematech)
Val Stradzs (WECC; Intel)
William Moore (WECC; IBM)
James S. Clarke (DDC; Intel)

Revision: 2009 Key Challenges

The Yield Enhancement community is challenged by the following topics:

- ***Near Term (>16 nm)***
  - ***Detection of Multiple Killer Defects / Signal to Noise Ratio -*** Detection of multiple killer defects and their simultaneous differentiation at high capture rates, low cost of ownership and high throughput. It is a challenge to find small but yield relevant defects under a vast amount of nuisance and false defects.
  - ***3D Inspection*** – For inspection tools the capability to inspect high aspect ratios but also to detect non-visuals such as voids, embedded defects, and sub-surface defects is crucial. The need for high-speed and cost-effective 3D inspection tools becomes crucial as the importance of 3D defect types increases.
  - ***Process Stability vs. Absolute Contamination Level –*** Including the Correlation to Yield Test structures, methods and data are needed for correlating defects caused by wafer environment and handling with yield. This requires determination of control limits for gases, chemicals, air, precursors, ultrapure water and substrate surface cleanliness.
  - ***Wafer Edge and Bevel Monitoring and Contamination Control –*** Defects and process problems around wafer edge and wafer bevel are identified to cause yield problems.

Revision: 2009 Key Challenges

The Yield Enhancement community is challenged by the following topics:

- ***Long Term (<16 nm)***
  - ***Non-Visual Defects and Process Variations –*** Increasing yield loss due to non-visual defects and process variations requires new approaches in methodologies, diagnostics and control. This includes the correlation of systematic yield loss and layout attributes. The irregularity of features in logic areas makes them very sensitive to systematic yield loss mechanisms such as patterning process variations across the lithographic process window. This issue should be already taken into account in the near term challenges.
  - ***In - line Defect Characterization and Analysis –*** *Based on the need to work on smaller defect sizes and feature characterization, alternatives to optical systems and Energy Dispersive X-ray Spectroscopy systems are required for high throughput in-line characterization and analysis for defects smaller than feature sizes. The data volume to be analyzed is drastically increasing, therefore demanding for new methods for data interpretation and to ensure quality.*
  - ***Development of model-based design-manufacturing interface —*** *Due to Optical Proximity Correction (OPC) and the high complexity of integration, the models must comprehend greater parametric sensitivities, ultra-thin film integrity, impact of circuit design, denser transistor packing, etc.*

Introduction of 450 mm substrates

Impact of 450 mm Wafer Diameter on Equipment and Metrology

Diameter	300 mm	450 mm
Thickness	775 µm	925 µm
Area	706 cm²	1589 cm²

Impacted Areas	Focus Items
Processes	uniformity of processes, contamination, thermal effects/uniformity, (cleaning, polishing, deposition, etch, anneal, ..)
Lithography	increase of area by 2.25 times requires high performance – high speed litho
Handling	**deformation (→stress), transport issues, wafer translation (large distances, acceleration and settling times increase, vertical drift along the wafer)**
Metrology	**stages and handling, mapping capabilities, increase of area by 2.25 times requires high performance – high speed metrology (inspection), dimensional change due to thermal expansion coefficient, …**
Data Management	**amount of data, data quality, …**

Revision: 2009 Key Challenges

- *Possible new Long Term (<16 nm) key challenge, including some near term key challenges:* ***Introduction of 450 mm substrates***
  - The introduction of 450 mm wafers in the future is expected to impact the yield topics in the following way:
  - Defect Detection and Characterization:
    - throughput in combination with tools cost: cost of ownership,
    - development of 450 mm handling for inspection (risk of large substrate flexibility, coordinate transfer for review,
    - huge amount of inspection data
  - Defect Budget and Yield Model
    - Number of chips per wafer
    - Defect densities are unknown (currently still available for 200 mm technology?)
  - The introduction of 450 mm wafers requires a new generation of inspection tools. It will be important to define prior to discussions the targeted technology generation.

Revision 2009

- **Overall**
  - confirmation of key challenges
  - introduction of 450 mm as a new challenge
- **DDC**
  - adjust tables to ORCT input
  - update colours and numbers
- **DB & YL**
  - outline for Defect budget survey presented
  - discuss non – visible defects
  - adjust tables to ORCT input
  - update colors and numbers

Revision 2009

- **WECC:**

  Focus items (Ultrapure Water, Chemicals, Gas, Precursors, Airborne/Surface Molecular Contamination)

  – Particles: Measurement, particle chemistry, critical size, identify yield correlation, deposition model
  – Organics: Measurement, speciation, identify yield correlation, deposition model
  – Ionic contamination: Measurement, identify yield correlation, deposition model
  – Gas, CVD/ALD precursor: Measurement, identify yield correlation
  – Airborne Molecular Contamination: Measurement, integrated control concept, cross contamination via FOUP (Cross-TWG work with FI)

Outlook

Development/ Improvement of the Yield Enhancement chapter

- Reflection of current status and future requirements needs subsequent adjustment of outline and content of the chapter
- Request to IDMs, JEITA, ISMI, academia contributing to ITRS:
  - assure that sufficient contributors and resources are available
  - surveys required for future updates e.g. DB&YM
- Definition of critical particle size with regard to different processes, products requirements