

Emerging Materials Committee Introduction and Focus

In 2003, the ITRS Starting Materials sub-Technology Working Group established the Emerging Materials Committee to examine and track alternative materials technologies that are under consideration for implementation in conjunction with traditional CMOS scaling. This document, which was released in 2007, is the second full revision of the original 2003 document.

Emerging Materials Definition

The definition of an Emerging Material is as follows:

Novel starting materials, structures, and processing methodologies that will enable anticipated roadmap requirements and enhance silicon-based CMOS technology.

In general, emerging materials will augment silicon transistor technology by providing enhanced speed, lower-power consumption, improved heat dissipation, improved memory capacity/data retention, or added RF/analog functionality while maintaining the large scale integration capability of CMOS. The augmentation of the silicon starting material need not be entirely silicon-based as long as CMOS system improvement is the end goal. As an example, the integration of III-V compound optoelectronics on Silicon (Si) for enhanced bandwidth for I/O limited CMOS technologies would be considered a topic for the Emerging Materials Committee, but the fabrication of III-V on Si devices for discrete implementation without any incorporation of a Si microelectronics theme would not be a topic for the Emerging Materials Committee.

Status of Emerging Materials

The Emerging Materials Committee has tracked technologies for close to four (4) years at this point and we believe it is important to provide guidance on the technologies that have demonstrated progress towards mainstream application (*i.e.*, have moved beyond ‘emerging’ status to more mainstream application); those technologies that have continued to stay active, but have not moved into mainstream application; and those technologies that have shown some loss of momentum.

Table 1: Emerging Materials Status Table

Emerging Material	First Year Coverage	Chip Products on Market	Close to Mainstream Acceptance	Change of Importance Since 2005		
				Increased	No Change	Decreased
Global Strained Si	2003	No	No		X	
Global Strained SOI	2003	No	No	X		
Germanium Channel Transistors	2003	No	No	X		
III-V Channel Transistors	2007	No	No		N/A	
Isotopically Pure Si	2003	No	No			X
Silicon on Diamond	2005	No	No		X	
Silicon on SiC	2005	No	No		X	
Silicon on Aluminum Oxide	2005	No	No		X	
Channel Orientation	2005	Yes	Yes	X		
Surface Orientation	2005	No	No		X	
Carbon Nanotubes	2005	No	No		X	
High Resistivity Si	2003	Yes	Yes	X		
Optical Interconnection on Si	2003	No	No		X	
Phase Change Memory	2007	No	No		N/A	

Table 1 lists the technologies that have been covered by the ITRS Emerging Materials committee since its inception in 2003 along with several columns that discuss the status of each technology.

The second column, First Year Coverage, denotes the year the technology was initially introduced as one of those tracked by the committee. The earliest a technology could be tracked was 2003 (the first year of the committee) and the latest would be 2007, which would be technologies we just started to consider this year for the 2007 ITRS. The new technologies under consideration this year are III-V Channel Transistors and Phase Change Memory.

The third column denotes whether actual chip-level products are on the market. Note that for several of the technologies, wafers or starting materials are commercially available (*e.g.*, Ge wafers), but for the scope of our work we consider chip implementation to be the indicator of the technology progression. In a somewhat linked criterion, the fourth column denotes whether the technology is close to mainstream acceptance. Admittedly, this is a somewhat subjective criterion as it is not possible to obtain complete records of how many companies

ship how many products with a given technology. From the committee's discussions, only the use of channel orientation to augment PMOS performance and the use of high resistivity (~1,000 Ω -cm) Si substrates would be considered mainstream technologies at this point. As such, the committee will no longer track channel orientation for mobility improvement as an emerging technology, and the tracking of high resistivity Si substrates will be limited to substrates with resistivity >10,000 Ω -cm.

The last three columns, broadly under the category of Change of Importance Since 2005, denote the committee's opinions on whether a particular technology has gained momentum since our last evaluations in 2005. The progression of Channel Orientation and High Resistivity Si to mainstream status has already been discussed. Strained Si on Insulator and Ge Channel Transistors have increased in momentum from our perspective due to the greater availability of starting materials and some reported advances in the transistor performance. Isotopically Pure Si is the only technology that we considered to have lost significance since 2005. For this reason, we will no longer track it as a viable Emerging Material that could potentially impact future CMOS technology.

All of the assessments in Table 1 are a snapshot of what the committee believes at the present time. In the future, it is anticipated that commercial trends and technological progress will alter our analysis. In the mean time, we welcome information from the semiconductor community that provides more perspective on the technologies we are covering (or perhaps those that we should be covering). Comments/thoughts can be sent to the committee chairman, Dr. Mayank Bulsara, at bulsara@atlastechnology.net.

Sources of Information and Emerging Materials Categories and Topics

The committee is grateful to the following industry experts who presented information on several relevant topics:

1. Steve Hudgens, *Ovonyx*, Phase Change Memory
2. Sajan Saini, *MIT Microphotonics Center*, Microphotonics
3. Don Scansen, *Semiconductor Insights*, Cutting Edge CMOS
4. Vahé Mamikunian, *Lux Research*, Emerging Nanotechnology
5. Ravi Kanjolia, *Epichem*, CVD/ALD Chemistry

After consideration of the information presented by industry experts and independent evaluation of the technologies being considered for implementation by the semiconductor industry, the Emerging Materials Committee identified four distinct categories of alternative materials solutions that are being examined by the semiconductor industry:

1. Thermal Management Solutions
 - a. Silicon on Diamond/Silicon on Silicon Carbide
 - b. Silicon on Aluminum Oxide on Silicon
2. Mobility Enhancement Solutions
 - a. Strained Silicon
 - b. Germanium/Strained Germanium Channels
 - c. III-V Compound Semiconductor Channels
 - d. Carbon Nanotubes
3. System on Chip Solutions
 - a. High Resistivity Silicon
 - b. Optical Interconnection on Silicon
4. Memory Solutions
 - a. Phase Change Memory

The fourth category, Memory Solutions, is new to this year's Emerging Materials analysis.

We note that forward-looking development approaches for any given technology may differ. Where possible, the committee has strived to present general embodiments of the identified Emerging Materials. However, where appropriate, more established approaches are highlighted. In addition, questions are raised if the long-term cost effectiveness or technical merits of an approach are not clear.

Thermal Management Solutions

Due to increased transistor density and enhanced current drive per transistor, the amount of power dissipated in modern circuits can lead directly to thermal management problems that could result in the degradation of circuit performance or reliability. The following subsections address materials solutions that enhance the thermal conductivity of CMOS circuits, thereby mitigating potential hot spots and the overall overheating of circuit components.

Silicon on Diamond/Silicon on Silicon Carbide

Materials with better thermal conductivity than Si in the immediate vicinity of the transistors could potentially keep circuits cooler due to their more efficient heat removal. For example, single crystal diamond and single crystal silicon carbide (SiC) have thermal conductivities, $20 \text{ W cm}^{-1} \text{ K}^{-1}$ and $3\text{-}4 \text{ W cm}^{-1} \text{ K}^{-1}$ respectively, that are much greater than that of Si, $1.5 \text{ W cm}^{-1} \text{ K}^{-1}$. Thus, it would be favorable to have diamond and SiC regions incorporated into chip architectures for thermal management reasons.

To reduce the operating temperatures of the Si transistors, the transistor regions need to be placed on top of either 1) a handle wafer consisting completely of better thermal conducting material or 2) a high thermal conductivity layer that itself resides on top of conventional Si substrate. In the first case, heat can be dissipated more efficiently to a heat sink. In the second case, heat removal from the active circuit is not changed much, but heat can be spread more uniformly across the entire area, thus reducing the potential for hot spots.

Combining CMOS quality Si with either diamond or SiC requires wafer bonding and layer transfer. In the case of diamond, the only reasonable option for the foreseeable future is to utilize a polycrystalline diamond film (note polycrystalline layers can have significantly lower thermal conductivity than equivalent single-crystal layers, but their properties will be dependent upon the grain size) sandwiched between a Si wafer and a thin Si active layer. Such a structure would be similar to SOI, but with a considerably thicker layer of diamond in the place of the traditional SiO_2 insulator in order to facilitate lateral heat flow. Since it is difficult to obtain a smooth surface of polycrystalline diamond, a planarizing layer of polysilicon or SiO_2 may have to be utilized between the Si film and the diamond. The SiO_2 layer would also help in passivating electrical defects at the lower Si interface.

Several different configurations with SiC are potentially possible. An oxidized layer of Si can be transferred to either a single crystal or a polycrystalline SiC wafer. Because of the cost considerations, polycrystalline SiC is a more attractive solution. Since our last review of this topic, wafers with a layer of Si on polycrystalline SiC (SopSiC) have been made commercially available at 75 and 100 mm diameter for use as substrates for GaN based power devices.

Extension of this technology to large wafer diameters suitable for high power/high performance Si devices is proceeding.

Silicon on Aluminum Oxide on Silicon

It is well known that the insulator in SOI structures is normally a thin layer of thermally grown SiO₂. A high quality dielectric layer with better thermal properties than SiO₂ would be of interest for improving heat dissipation in SOI circuits. Amorphous, polycrystalline or possibly single crystalline aluminum oxide, Al₂O₃ (called sapphire when it is single crystalline), has a thermal conductivity 10-30 times higher than SiO₂ and would thus improve heat dissipation during SOI circuit operation¹.

Mobility Enhancement Solutions

Modern transistor technology has essentially reached the limit of the fundamental electronic capabilities of Si. High mobility materials for enhanced transistor speed and reduced power consumption are considered paramount for modern CMOS applications. The following subsections address several solutions for enhancing the mobility characteristics of CMOS transistors.

Strained Silicon (On Insulator)

Strained Si technology, the introduction of elastic strain in Si transistor channels, is the most widely accepted method for enhancing the carrier mobility of Si. There are two variants to Strained Si technology that have been researched and demonstrated: 1) local strain introduction via transistor module engineering and 2) global (wafer-scale) strain introduction via silicon-germanium (SiGe) epitaxial processes (and layer transfer processes for global strain with SOI). For the purposes of this document local strain introduction techniques are not considered emerging materials since they are already in production, but they are discussed to provide a reference point for the status and performance potential of global strain engineering techniques.

Global strained Si technology is based upon the deposition of Si_{1-x}Ge_x alloys, which form a template for subsequent channel layer deposition (and layer transfer process in the case of strained Si on insulator [SSOI]). Typically the alloys contain a Ge content in the range of x=0.15 to 0.30. The deposition of pure Si on such a template results in biaxial (*i.e.*, in the two in-plane directions) strains on the order of 1%. Due to strain introduction at the starting materials stage, global or wafer-scale strained Si is more universal in nature and some of its attributes or specifications can be addressed more generally.

¹C. de Beaumont, *et al.*, *Silicon-on-Insulator Technology and Devices XII*, ECS Proc Vol. 2005-03, edited by G. K. Celler, *et al.*, p 231 (2005)

Table 2: Reported enhancements with local and global strain engineering techniques

Manufacturer	Strain Type	L_g (nm)	NMOS I_{dsat} Enhancement	PMOS I_{dsat} Enhancement	Reference
AMD	Local (on SOI)	40	13%	20%	M. Horstmann, et al., Mat. Sci. and Eng. B, 114-115, p. 3, 2004
AMD	Global	25	25%	N/A	J.S. Goo, et al., IEEE Elec. Dev. Lett., 24, p. 351, 2003
Freescale/TSMC/SOITEC	Global (on SOI)	150	28%	12%	A.V.Y. Thean, Symp. on VLSI Tech., p. 134, 2005
Freescale/SOITEC	Global/Local (on SOI)	40	27%	36%	A.V.Y. Thean, Symp. On VLSI Tech., 2006
IBM/Sony/Toshiba AMD/Chartered	Local (on SOI)	45	11%	20%	H.S. Yang, et al., IEDM Tech. Dig., p. 1075, 2004
IBM	Global	67	35%	N/A	K. Rim, et al., Symp. on VLSI Tech., p. 59, 2001
Intel	Local	45	10%	25%	T. Ghani, et al., IEDM Tech. Dig., p. 978, 2003
Intel	Global	140	24%	N/A	S. Datta, et al., IEDM Tech. Dig., p. 653, 2003
Toshiba	Global	40	N/A	19%	T. Sanuki, et al., IEDM Tech. Dig., p. 65, 2003
TSMC	Global	60	15%	N/A	H.C.H. Wang, et al., IEDM Tech. Dig., p. 61, 2003

Table 2 summarizes several transistor performance results based upon global and local strain engineering techniques. It should be noted that the only new data point in Table 2 since the last survey is highlighted point reported by Freescale/SOITEC. The data reported by Freescale/SOITEC is based upon the concurrent optimization of NMOS and PMOS with globally strained silicon on insulator (SSOI) substrates and local strain techniques. This data point addressed one of the outstanding questions since our last update, which was the demonstration of an integration scheme that addressed both NMOS and PMOS drive current enhancements. In addition, since our last report on Emerging Materials, SSOI substrates have been made commercially available, thereby enhancing its outlook for potential commercial chip applications.

Germanium/Strained Germanium Channels

Transistors with pure Ge channels are being investigated for implementation in next-generation microelectronics. The ultimate advantage of working with Ge is the carrier mobility enhancement, making it attractive for high-speed circuit applications. Low field electron mobility in Ge is more than double that of Si (3900 vs. 1500 cm²/V-sec) and the increase is four-fold for holes (1900 vs. 450 cm²/V-sec). Despite the intrinsic speed advantages of implementing Ge transistor technology, Ge has not established a strong presence as an electronic material for ubiquitous microelectronic application because it does not form a stable oxide that would be suitable for gate stack formation. However, as the industry is beginning a transition to high κ dielectric films, necessitated by electron tunneling through very thin SiO₂, new opportunities are being explored to implement pure Ge transistor technology.

There are two aspects of development that need to be considered in parallel for implementation of Ge transistor technology: 1) The embodiment of the Ge substrate technology and 2) The multiple aspects of Ge transistor integration and performance optimization.

The three embodiments of Ge substrate technology are generally: 1) Bulk Ge substrates, 2) Ge layers transferred to oxidized Si handle wafers, thereby forming Ge-on-Insulator (GeOI) and 3) Epitaxial deposition of Ge thin films on Si substrates in various configurations. Bulk Ge substrates (grown via the Czochralski method) are more difficult to make than bulk Si substrates due to the lower critical resolved shear stress and lower mechanical strength of Ge. Although 300 mm dislocation-free Ge substrates can be fabricated, the economics of high volume manufacture are still unsure. Development is still required to obtain site flatness and crystal originated pit (COP) specifications that are equivalent to state of the art Si substrates. Ultimately, even if the technical and economical issues were resolved, it is unlikely that the world's Ge reserves could support the complete replacement of bulk Si substrates via Ge, therefore it is expected that Ge substrate technology developments will be aimed at making Ge substrates that are suitable as donor wafers for repeated Ge exfoliation processes in the formation of GeOI. GeOI addresses substrate manufacturability concerns and reduces the likelihood of excessive Ge junction leakage during device implementation. Epitaxial Ge technology is especially promising, and necessary, for the implementation of biaxially strained Ge channels, which have been shown to have the highest hole mobility.

Since Ge inversion layer mobility is the key metric in comparison to traditional Si transistor technology, the integration of a reliable gate stack is paramount to exploiting the benefits of Ge transistor technology. Germanium oxynitride^{2,3}, aluminum oxide⁴, hafnium oxide⁴, and zirconium oxide⁵ high κ dielectrics have

² Chui, *et al.*, IEEE Electron Device Lett., **25**, p. 613 (2004)

³ Shang, *et al.*, IEDM Tech. Dig., p. 441 (2002)

⁴ Chen, *et al.*, IEEE Trans. Electron Devices, **51**, p. 1441 (2004)

been implemented with Ge channel transistors with varying degrees of success. However, no completely satisfactory solution has been demonstrated with Ge channels. This in part has led to less than anticipated mobility enhancements for holes and typically electron mobilities that are inferior to that of Si. For methods that use epitaxial Ge layers, thin layers of Si, which preserve the gate oxide integrity, have been used to cap the Ge channel layers. Relaxed and biaxially strained embodiments of Ge transistors using Si capping layers have markedly better mobility characteristics (2X-10X) than Si control transistors⁶. Some questions about properties of Ge in such applications require further analysis. Ge has a smaller bandgap than Si, which can cause junction leakage problems. However, it has been reported that in the presence of significant strain, Si may experience more leakage than Ge⁷. Lastly, the saturated high field drift velocity of charge carriers in Ge is somewhat lower than that of Si.

Recent experiments and simulations are helping to fully define the benefits and trade-offs of modern Ge electronics⁸. As the benefits are established, the optimum substrate and transistor embodiments will become clearer. In general, we believe that Ge substrate/transistor architectures will continue to gain momentum and play prominent role in future Si-based microelectronics.

Surface Orientation

Another approach to improve on the mobility and current drive capabilities of Si involves the exploitation of the mobility anisotropy of Si. Figure 1 shows the mobility of electrons and holes for different surface orientations and in the case of the (110) surface, two different in-plane channel directions. It is well known that electron mobility is highest for the traditional Si substrate/transistor configuration, which includes a (100) surface with a $\langle 110 \rangle$ channel direction, while hole mobility is highest for a (110) surface with a $\langle 110 \rangle$ channel direction. A hybrid substrate configuration¹¹ has been proposed to allow for the ultimate mobility configuration for each carrier. As with conventional Si surface and channel geometries, the introduction of strain in tandem with different substrate orientations has been under investigation^{9,10}.

⁵ Chui, *et al.*, IEDM Tech. Dig., p. 437 (2002)

⁶ Lee, *et al.*, IEDM Tech. Dig., p. 429 (2003)

⁷ Krishnamohan, *et al.*, IEDM Tech. Dig., p. 937 (2006)

⁸ Saraswat, *et al.*, IEDM Tech. Dig., p. 659 (2006)

⁹ T. Mizuno, *et al.*, IEEE Electron Device Letters, 24, p. 266 (2003)

¹⁰ T. Mizuno, *et al.*, IEDM Tech. Dig., p. 809 (2003)

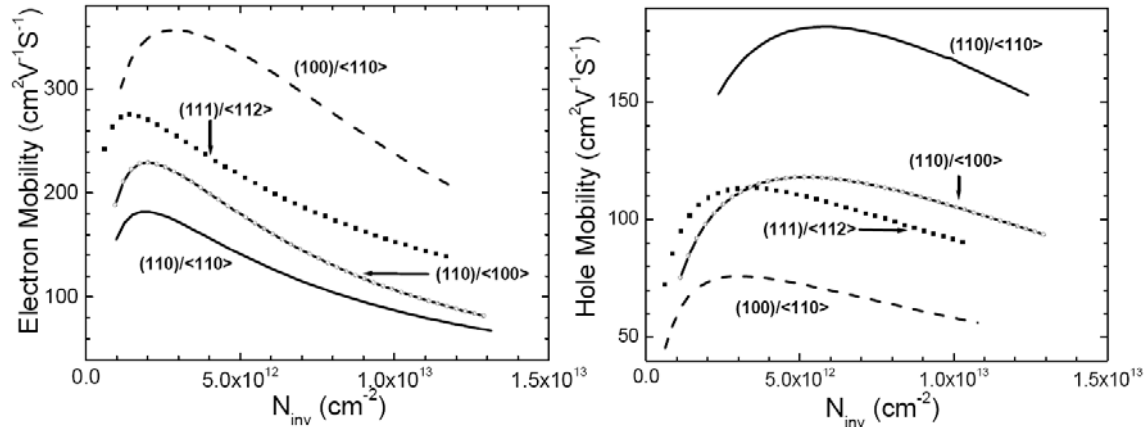


Figure 1: Electron and Hole Mobility Anisotropy for Silicon¹¹

Carbon Nanotubes

Carbon Nanotubes (CNTs) have remarkable physical and chemical properties. CNTs, only 1-2 nm in diameter, have a tensile strength that is 375 times greater than that of steel. In addition, the Young's modulus and thermal conductivity of CNTs are nearly those of diamond. The density of a hexagonal array of CNTs is about 1.4 g/cm³. This remarkable combination of properties lead to a wide variety of potential applications for CNTs such as composite materials, hydrogen storage, fabrics, lithium intercalation for batteries, and electrochemical super capacitors. We are concerned here with only their electrical properties for microelectronic application.

Single-walled carbon nanotubes (SWCNTs) are attractive for extreme scaling of integrated circuits due to their small diameters (~ 1 nm), long lengths (~ 100s μm), and thermal stabilities. SWCNTs can be either semiconducting or metallic, and their electrical properties depend on the tube's longitudinal axis relative to principal axes of a graphene sheet (helicity)¹² and its diameter. SWCNTs are being considered for application as transistors, diodes, and interconnects in future integrated circuits.

CNT Transistors

CNT field effect transistors (CNTFETs) can be modified and controlled in many of the same ways that Si MOSFETs can be tailored. They can be p-type or n-type and their threshold voltages can be set by doping. CNTFETs can exhibit bulk-switched behavior like MOSFETs with characteristics equal to or superior to conventional Si devices. The advantages of CNTFETs include high mobility, no mobility degradation when integrated with high κ dielectrics, ballistic transport, adjustable band gap, and low contact resistance. Integration of CNTFETs has also been shown viable through demonstration of several kinds of small circuits with CNTFETs including NOT and NOR logic gates, flip-flops, ring oscillators and voltage inverters.

¹¹ M. Yang, *et al.*, IEDM Tech Dig., p. 453 (2003)

¹² J. Wilder, *et al.*, Nature, 91, p. 59 (1998)

FETs utilizing CNTs as channel materials are one-dimensional (1D) devices due to the small diameters of CNTs. The 1-D nature of CNTFETs draws performance comparisons to Si nanowire FETs, which have been shown to have superior scalability over even double-gate FETs in simulations¹³. CNTs offer several advantages over Si nanowires. SWCNTs are about five times thinner than the thinnest Si nanowires, leading to improved scalability. Si carrier mobility degrades, especially for holes, as the Si becomes thin¹⁴, whereas this is not the case for CNTFETs, which have hole mobilities up to 80 times higher and lower self-heating than that in Si nanowires with comparable dimensions^{15,16}. CNTs also have atomically smooth surfaces for hundreds of micrometers and all the carbon bonds are within the CNT, reducing electronic states at the interface with the gate dielectric. These features allow for ballistic transport and higher on-currents than Si nanowires^{15,16,17}.

Transistors using CNTs as channels do not offer any advantages over other materials at the quantum mechanical tunneling limit between the source and the drain. This limit is predicted to be at a gate length of about 5nm, but up to this limit CNTFETs can offer improved performance over Si MOSFETs.

Metallic CNTs

Metallic SWCNTs have better conducting properties than copper and can carry very high current densities (1000 times higher than copper), making them attractive for highly scaled interconnects. Calculations for the 45 nm technology node show no performance enhancement for CNTs over similarly sized copper lines. However, the performance enhancement is expected to be 30-80% for the 22 nm node, depending on the mean free path of electrons in the CNTs^{18,19}. Multi-walled CNTs in a 20 nm diameter, 150 nm long via have demonstrated a resistance of 8 k Ω and a current density of 500 MA/cm²²⁰. While these values are about an order of magnitude lower than ideal, the work demonstrates feasibility of the use of CNTs as interconnects.

Process Control of CNTs

While CNTs are very attractive for use in integrated circuits, several difficult problems remain to be solved before wide-spread use is realized. Methods must be developed to precisely and consistently control CNT structures (*e.g.*, desired positions, helicity, diameters, directions, and lengths), and hence the electrical properties of CNTs during synthesis. As a first step, methods for large-scale separation of electrical and semiconducting CNTs are required. Some progress

¹³ J. Wang, *et al.*, IEDM Tech. Dig., p. 695 (2003)

¹⁴ K. Uchida, *et al.*, IEDM Tech. Dig., p. 47 (2002)

¹⁵ T. Durkop, *et al.*, Nano Lett., 4, p. 35 (2004)

¹⁶ S. J. Wind, *et al.*, Phys. Rev. Lett., p. 0583011-4 (2004)

¹⁷ J. Guo, *et al.*, IEDM Tech. Dig., p. 703 (2004)

¹⁸ A. Naeemi, *et al.*, Electr. Dev. Lett., 26, p. 84 (2005)

¹⁹ A. Naeemi, *et al.*, IEDM Tech. Dig., p. 699 (2005)

²⁰ F. Kreupl, *et al.*, IEDM Tech. Dig., p. 683 (2004)

is being made in this area and it is likely that some sort of self-assembly technique will be required. However, it remains to be seen if any technique will satisfy mainstream CMOS requirements and allow for useful CNT integrated circuit components.

III-V Channel Transistors

High mobility channel materials that are compatible with Si are being sought as one way to extend the performance of integrated circuits beyond physical limitations of Si based electronics. High mobilities can offer comparable or improved performance at lower voltages than standard Si, providing increased power saving. In addition to strained Si, and CNTs described above, III-V materials offer interesting possibilities and significant challenges as channel materials. Many III-V materials offer very high electron mobilities, as high as 3-50 times that of Si. Examples include materials such as GaAs, GaSb, and InSb. There is a relatively short list of materials that offer high hole mobilities. While GaSb and InSb offer modest improvements in hole mobility over Si, Group IV elements such as C and Ge may also need to be integrated as channel materials for PFETs to maximize performance scaling. Much of the processing to make devices with the III-V materials is known. High electron mobility transistors (HEMT) made with III-V compound materials have been implemented commercially for very high frequency applications for a very long time. However, scaling of such devices was limited to gate lengths above 100 nm. Recently, HEMTs with gate lengths as short as 50 nm with high I_{on}/I_{off} ratios have been produced²¹. The band gap of materials generally decreases as their mobility increases. Thus, voltage scaling will have to continue in order to take advantage of high mobility materials.

While these materials show significant promise, there are also significant challenges associated with their implementation. Any new material destined to replace or enhance CMOS integrated circuits must ultimately integrate well with Si. The most promising materials have lattice constants significantly different from that of Si. Hence epitaxial films must be engineered well to enable new, high-mobility channel materials. Another challenge is that the density of states for many high mobility materials is low, limiting the amount of current they can support. Improving the ability to dope the source-drain regions of such materials will be key to reducing parasitic resistances external to the channel. High κ gate dielectrics, just now about to being introduced with high volume Si integrated circuits, will be needed to minimize gate leakage and further gate length scaling for III-V compound channel materials. Recently, researchers built and demonstrated enhancement-mode, high-mobility, NMOS devices incorporating a high κ gate dielectric on a GaAs channel without Fermi pinning²².

²¹ J. del Alamo and D.-H. Kim, IPRM, p. 51 (2007).

²² K. Rajagopalan, et al., Elec. Dev. Lett., **28**, p. 100 (2007)

System on Chip Solutions

As core digital logic continues to advance in terms of performance, there is an increasing need to further the state-of-the-art chip capabilities in other areas, such as input/output functions and integration of more functionality. The following subsections describe two technologies/concepts that under consideration to improve overall chip/system performance.

High Resistivity Silicon

Material and device developments over the past few years have enabled the production of CMOS and BiCMOS transistors capable of operating at very high RF frequencies. The fabrication sequence of such devices is compatible with standard digital CMOS processing, allowing the monolithic integration of RF circuitry with high-speed logic and memory. This has led to the emergence of whole new classes of mixed digital/analog devices with wireless communication capabilities.

Most CMOS logic and memory circuits today are fabricated on bulk wafers with resistivity in the range of about 1-20 ohm-cm, or epi wafers with a similar epi resistivity on a heavily doped substrate. SOI wafers are also used for both CMOS and BiCMOS devices. The integration of RF circuits into CMOS devices favors a shift to a very high substrate resistivity. This is because unlike digital CMOS, RF circuitry requires linear, analog devices with low noise and precision passive components (*e.g.*, resistors, capacitors and inductors). Very high substrate resistivity decreases capacitively-coupled cross-talk between digital, analog and RF components, improving noise isolation. It also improves the quality factor of spiral inductors by decreasing eddy current losses, and improves the quality factor of metal-insulator-metal (MIM) capacitors by decreasing parasitic substrate capacitance.

The intrinsic resistivity of Si, ~725,000 ohm-cm at room temperature, is the maximum resistivity theoretically attainable. In practice, resistivity greater than 50 ohm-cm offers tangible benefits to device performance. "High resistivity" is typically defined as resistivity $\geq \sim 1000$ ohm-cm, but as we noted in the introduction, we can consider ~1000 ohm-cm resistivity substrates to be mainstream. However, much higher resistivity (~10,000 ohm-cm) Si substrates are still being sought and fall into the category of emerging materials.

Production of high resistivity Si places three stringent demands on the crystal growth process. First, the intentional dopant addition to the crystal must be very tightly controlled, and the crystal growth process must produce extremely good axial and radial resistivity uniformity. Second, the sources of unintentional doping must be minimized by the careful application of high purity materials. Finally, the formation of interstitial oxygen (O_i)-related thermal donors during heat treatment in the temperature range of 400-550 °C must be suppressed. Since this temperature range is common in back-end fab processes, the control of

thermal donor formation is vital to obtaining stable, predictable resistivity behavior during device processing.

Float zone (FZ) Si has traditionally been used to produce very high resistivity Si. The FZ process is crucible-less, so that unintentional doping problems are greatly reduced. Because it is crucible-less, FZ Si is also essentially free of oxygen, eliminating thermal donors. The FZ process also acts as a zone refining process, sweeping out impurities ahead of the melt interface. Although FZ 200 mm is commercially available in volumes, there is no development activity for 300 mm at this time. Unless introduced by intentional oxygen doping, FZ crystals by default have much lower oxygen concentrations than CZ. This avoids the unwelcome thermal donors, but also reduces or prohibits internal gettering and decreases the mechanical strength of the wafers.

Czochralski (CZ) growth is preferable to FZ for large-scale production of large diameter wafers; however, the use of a silica crucible in CZ growth leads to two problems. First, boron is a low-level contaminant in SiO₂ that is very difficult to remove. Consequently, unintentional boron contamination of CZ Si from even the highest purity crucibles makes it very difficult to produce substrates with resistivity greater than ~ 5000 ohm-cm. Secondly, the crucible introduces interstitial oxygen into the CZ Si, leading to potential thermal donor formation problems. CZ growth methods exist that can reduce O_i to a level where thermal donor generation is insignificant, but as in the FZ case, these low-O_i wafers do not develop the oxygen precipitation necessary to produce internal gettering nor strengthen the wafer.

Currently, the most promising approach to suppression of thermal donor formation at the higher O_i levels found in standard CZ Si is to deliberately grow oxygen precipitates in the wafer to consume interstitial oxygen^{23, 24} while still maintaining control of the requisite wafer warpage. Growth of a high density of large precipitates can consume enough of the interstitial oxygen to minimize subsequent thermal donor formation. As an added benefit, the oxygen precipitates provide internal gettering in the wafer. The oxygen precipitation heat treatment can be lengthy however, adding to the wafer manufacturing cost. The growth of large precipitates and concomitant decrease of O_i also lower the yield stress of the wafer. Very high temperature heat treatments (T > 1100-1200 °C) in the fab can also redissolve some of the precipitated oxygen, increasing O_i and leading to thermal donor formation again, during subsequent thermal processing. Efforts continue to develop a robust and cost-effective manufacturing process that can control thermal donor formation while providing acceptable internal gettering in high resistivity, CZ Si.

The effects of co-doping CZ material with suitable deep level traps have also been investigated. The decreased resistivity due to background Boron

²³ T. Abe and W. Qu, ECS PV **2000-17**, 491-500 (2000)

²⁴ Ohguro, *et al.*, Symposium on VLSI Technology, 2002, 158-159 (2002)

concentration on CZ wafers could be counteracted by using suitable doping species^{25 26}. It is not clear at this time if co-doped material is compatible with device processing requirements.

Integrated Optoelectronics on Silicon

Si has become the mainstay of the digital computing industry due to its unique integration capabilities and highly efficient cost structure. Despite Si's prowess in most mainstream semiconductor applications, a need is developing to introduce technologies compatible with Si that enable high speed, optical communications for application within chip, chip to chip, and beyond. Techniques akin to packaging (e.g., hybrid chip mounting) administer to some of this need, but monolithic integration of light emission, light detection, and light routing capabilities with Si CMOS computing provides the greatest potential for Si microsystem enhancement. In general, light emission and light detection offer the greatest challenges when considering optoelectronic integration with Si CMOS because of Si's limited utility in such applications due to its indirect band gap. Recent advances in utilization of the Raman Effect in Si have enabled the demonstration of continuous-wave Raman Si laser²⁷. Although there are many variants in the literature, there are two other broad approaches for the integration of light emission and light detection communications capability with Si: (1) alter the Si microstructure in a way to induce a corresponding change in its energy band diagram, to enable efficient light coupling and conversion, (2) work with interlayer approaches to introduce high quality photonic materials (e.g., III-V compounds, Ge photodetector layers, or carbon nanotubes) on the Si substrate.

²⁵Mallik, *et al.*, *Semiconductor Science and Technology*, vol. 18, no. 6, pp. 517-524, 2003

²⁶Mallik, *et al.*, *Proceedings of the 36th European Solid States Device Research Conference*, pp. 435-438, 2006

²⁷H. Rong, *et al.*, *Nature*, **433**, p. 725, 2005

Memory Solutions

Up till this year the Emerging Materials Committee had focused primarily on the introduction of new materials in computing technology and has not considered the application of new materials for memory technology. The use of new materials for memory chips is certainly not a new concept, as a large suite of materials have been examined for use with dynamic random access memory (DRAM) fabrication processes, and there is no way we can provide an complete treatment on the topic at this time. However, we believe it is appropriate for the committee to at least start considering and providing some information on emerging materials making progress for memory application. Please note that an exhaustive treatment of alternative memory technologies is considered in the Emerging Research Devices section of the ITRS and we will not try to duplicate those excellent efforts, but we will more try to provide some supplemental information and perhaps in time branch into alternative approaches and analyses.

Phase Change Memory

Phase change memory (PCM) is a nonvolatile memory architecture that relies upon materials that can undergo electrically induced, reversible phase changes (amorphous-to-crystalline and vice versa). In the amorphous state the material can be greater than 1000X more resistive than in the crystalline state, and thus its phase is an indication of its programming state. Chalcogenide thin films were reported to show these characteristics as early as 1968²⁸. Soon after this discovery, chalcogenide thin films started to be considered for optical memory application²⁹ and now they are used ubiquitously in commercial optical storage products. For the past several years, PCM has been under serious investigation for displacement of NOR flash memory and DRAM products.

Ge₂Te₂Sb₅ is the material of choice for PCM applications and it is typically deposited via sputtering, although there have been reports using atomic layer deposition and metal-organic vapor deposition methods. In terms of chip integration, there have been several reports of successful test chip demonstration by multiple commercial entities^{30,31}.

Sampling of the technology appears to be underway and given the extensive research and background work in the development of these materials, we believe that PCM will find suitable placement in commercial products going forward.

²⁸ S.R. Ovshinsky, Phys. Rev. Lett., 21, p. 1450 (1968)

²⁹ J. Feinleib, *et al.*, J. of Noncrystalline Solids, 8-10, p. 909 (1971)

³⁰ K.J. Lee, *et al.*, Proc. of ISSCC, p. 472 (2007)

³¹ J. Maimon, *et al.*, Proc. of NVMTS (2002)