2008 Test and Test Equipment

July 2008
San Francisco, USA

Roger Barth - Chair

ITRS Test TWG

2008 Test TWG Members

44 members – 30 Affiliations

Name	Affiliation	Name	Affiliation
Dave Armstrong	Advantest	Yi Cai	LSI
Paul Roddy	Advantest	Jerry McBride	Micron
Mike Peng Li	Altera	Peter Maxwell	Micron
Mike Bienek	AMD	Roger Barth	Numonyx - Chair
Amit Majumdar	AMD	Bill Price	NXP Semiconductors
Calvin Cheung	ASE	Rene Segers	NXP Semiconductors
Rob Aitken	ARM	Wataru Uchida	Renesas (STRJ)
Mouli Chandramouli	ARM	Sejang Oh	Samsung
Atul Goel	Avago Technologies	Davide Appello	STMicroelectronics
Tetsuo Tada	Bunri University, Japan	Sridhar Kannan	Stream Processors
Steve Payne	Credence	Prasad Mantri	Sun Microsystems
Jack Courtney	IBM	Tom Williams	Synopsys
Shawn Fetterolf	IBM	Brad Robbins	Teradyne
Anne Gattiker	IBM	Lee Song	Teradyne
Phil Nigh	IBM	Steve Comen	TI
Jody Van Horn	IBM	Shichi Ito	Toshiba (STRJ)
Dennis Conti	IBM	Ulrich Schoettmer	Verigy
Peter Muhmenthaler	Infineon	Erik Volkerink	Verigy
Phil Burlison	Inovys	Yervant Zorian	Virage Logic
Wendy Chen	KYEC		
David Wu	Intel	Mike Rodgers	Consultant
Koorosh Zaerpoor	Intel	John Lukez	Consultant

2008 Test Updates

- Mixed Signal
  - mid & max ranges vs. high only
    - Waveform generators – 40-80 MHz mid vs 120-320 MHz max
    - Noise floor at -145dB for mid vs. -165dB for max
  - Non-numerical changes to reflect current state of the art
- RF
  - Faster Radio adoption rate and RF ports per device
  - Non-Numerical changes to table to reflect current state of the art
- Logic
  - Likely minor revision in logic data volumes
  - SoC DFT wrapper alignment with between design and test
- Memory
  - 200 MHz NAND updated to reflect ONFI-2 performance pull-in
  - LPDDR2 performance will be added in the 2009 roadmap

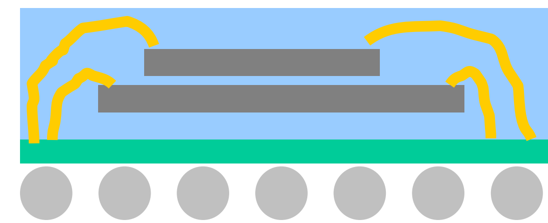
Challenges

Challenge - DFT

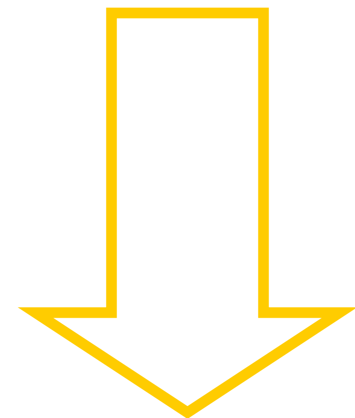
- Encompassing “More than Moore”
  - Multi-heterogeneous core devices
- Rewrite with partitioning between design and test chapters
  - Test – requirements for low cost
  - Design – implementation methodology
- Test power vs. operational power management
- Test wrappers for future cores
  - Method to handle legacy cores
- Scalable DFT architecture – die to system operation
- Compression, compression ratio and fault isolation

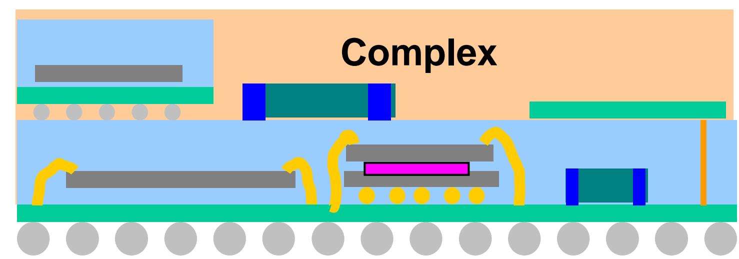
Challenge – SiP Test

- Now highly complex systems
  - Any Silicon (digital, analog) & passives
  - Packaged ICs, other SiP
- Targets consumer & low power
- Challenges
  - High yield with low test cost
  - Standardized test strategy
- Potential solutions
  - Design for die, debug and system test
  - Per die BIST and accessibility at all levels
  - KGD use with minimal post test
  - On-SiP test engine



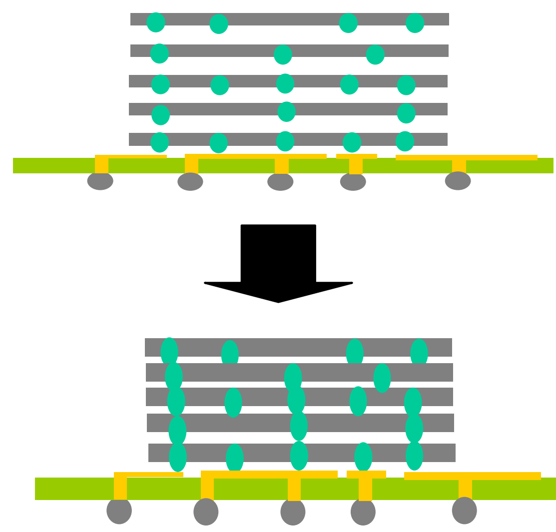
Simple





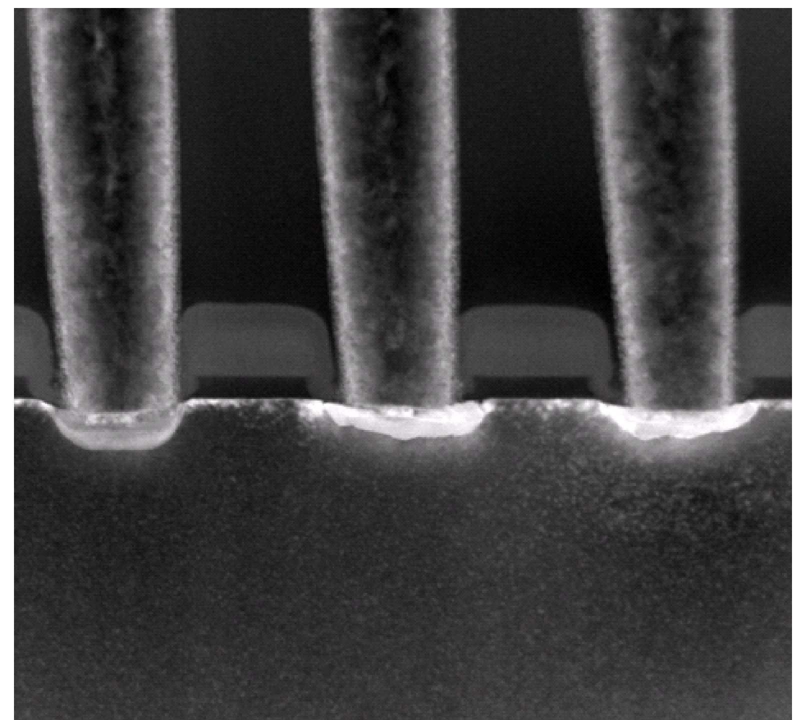
Challenge - 3D Devices

- Multiple die system
  - Sub-systems designed to be assembled together
  - Connection is by potentially 1000’s of TSVs (Thru Silicon Via’s)
- Design, Test and Assembly joint problem
- Requirements
  - Testability of each die
  - Via continuity checks - for signal and non-signal vias
  - Cross die test methodology
  - System (die stack) test post assembly
  - Multi-die domain EDA tools required



Challenge: Test for Yield Learning

- "Visualize" Non-visible defects…yield learning is statistical!
  - Predominant in roadmap
  - "Feature" of approaching the wall
- Smart Data Mining tools
  - Find common signatures in fail data
  - Adaptive data collection
- Localization of defects



Challenge – Cost of Test

- Maintain Moore's Law learning per technology
- Effective use of DFT die size budget per litho
- Make the device appear "smaller"
  - Concurrent test of similar structures or cores
  - Memory folding and compression
- Higher parallelism on reduced pin interfaces
- Self Test
- Reuse of older tools
- Guaranteed "performance" by proving "functionality"

Challenge - Mechanical Handling

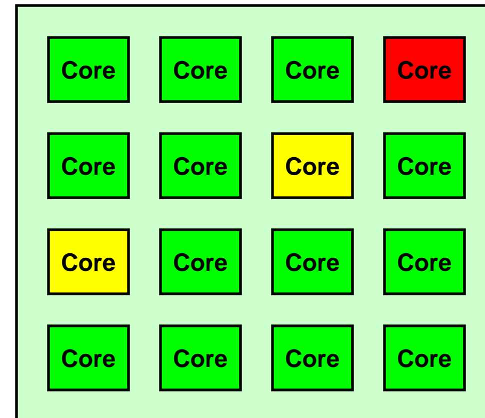
- Small ball pitches on high parallelism memory (>0.4mm)
- Very small packages (2mm x 3mm)
- Testing and handling of < 20um "thin" die
- High test parallelism
- 450mm wafers

Challenge - Fault Tolerant Devices “Bad but Good”

- Multiple identical core MPUs…not all cores need be good
- Memory with allowable bad bits / blocks
- Image sensors without the “perfect” image

Challenge: Fault Tolerant Device "Bad but Good"

- Multi identical core MPU
- Core issues
  - 1 bad
  - 2 marginal
- Is MPU good or bad?
  - Disable cores?
  - Fix or "Ignore" with smart OS kernel?



2008 Key Drivers

- Device trends
  - Increasing device interface **bandwidth** (# of signals and data rates)
  - Increasing **device integration** (SoC, SiP, MCP, 3D packaging)
  - Integration of emerging and **non-digital CMOS** technologies
  - **Complex package** electrical and mechanical characteristics
  - Device **characteristics beyond** one sided **stimulus/response** model
  - **Multiple I/O types and power supplies on same device**
- Increasing test process complexity
  - Device **customization** during the test process
  - "**Distributed test**" to maintain cost scaling
  - **Feedback** data for tuning manufacturing
  - **Dynamic test flows via "Adaptive Test"**
  - Higher order dimensionality of test conditions
- Continued economic scaling of test
  - **Physical limits** of test parallelism
  - Managing (logic) test data and feedback **data volume**
  - Effective limit for speed difference of **HVM ATE versus DUT**
  - Managing **interface hardware** and (test) socket costs
  - Trade-off between the **cost of test** and the **cost of quality**
  - **System test and BIST** driving multiple test socketings

Cost of Test

$ NRE Costs

$ DFT design and validation
$ Test development

$ Device Costs

$ Die area increase
$ Yield loss

$ Work-Cell Cost

$ Building Capital
$ People
$ Consumables
$ Loadboards, DUT interface

$ Capital Equipment

Depreciation of:
$ Test Equipment
$ Handler/Prober

Untested Units → **Work-Cell** → **Good Units Shipped**

Work-Cell → **Rejected Units**

UPH/$M

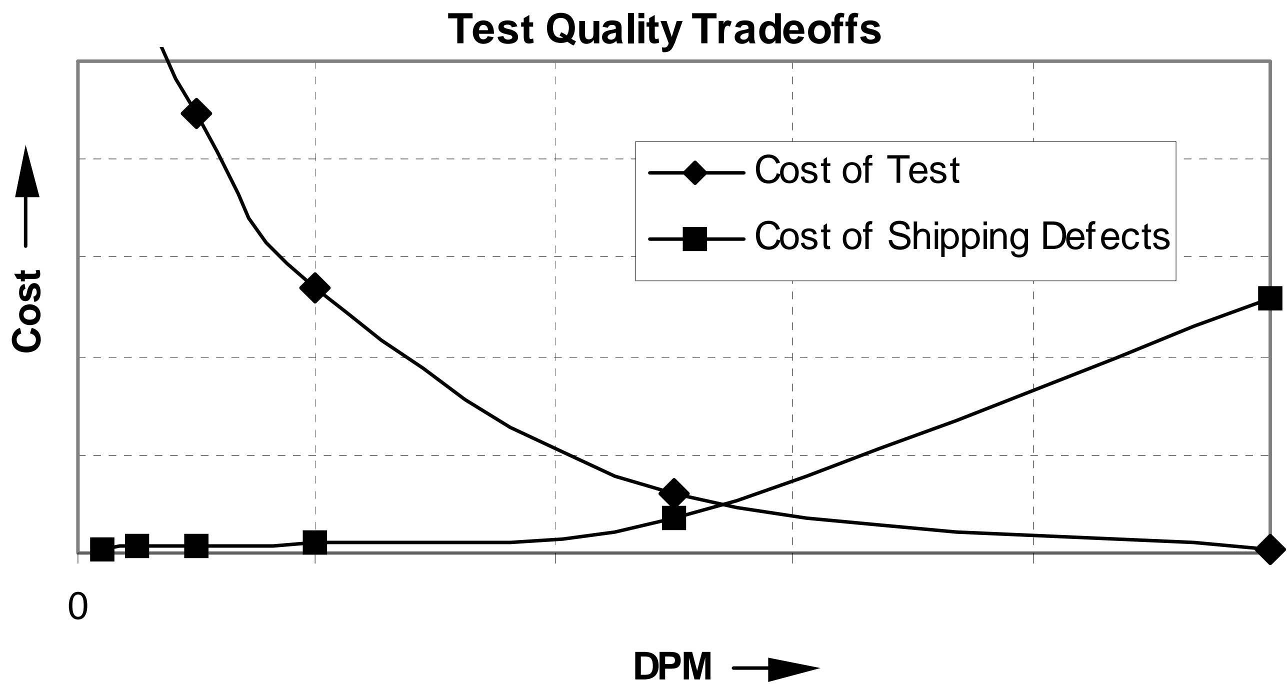
Effectiveness Measure

Goal is to optimize product cost

- Must strike a balance between cost/value of design, manufacture, yield learning, and test

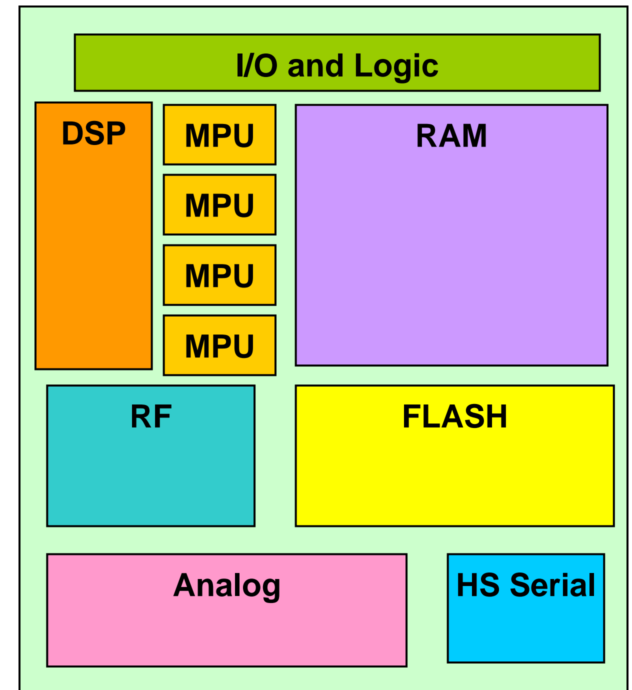
Cost of Quality

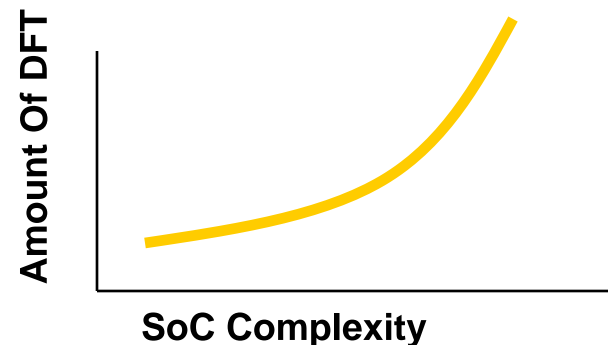
- Test is a balance of DPM and cost
- Shipped defect cost is more than bad components
  - Customer relationships, goodwill, penalties



SoC – Consumer Logic

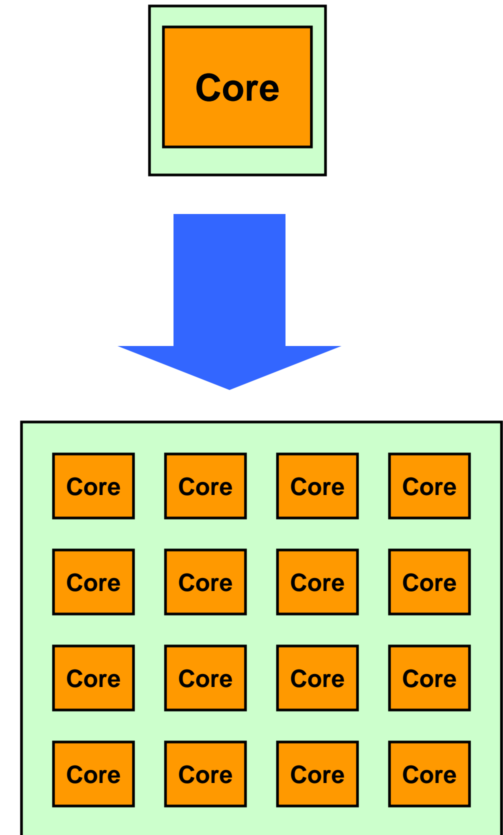
- > 1000 cores by 2020
  - MPU / logic
  - Memory
  - Analog / RF
  - HS serial
- Per core DFT
- SoC test challenges
  - Management of per core DFT
  - Standardization of core “wrappers”
    - IEEE 1500 core test
    - IEEE P1687 JTAG chip-test





High End Logic

- Trend: Single to Multi core
  - Forecast: 22 cores by 2020
- I/O GT/s increasing
  - Aligned to number of cores
  - Multi-lane HS serial to 20GT/s
- Non-diff I/O will remain below 2 GT/s
  - Accuracy and noise limitations
- Structural test at low speed
  - Vectors increasing with Flip-Flop count



MPU "GHz" by "Cores"

2008 update

Actual

Forecast

CPU "GHz"

CLK (GHz)	
Clk Roadmap	
Cores * Clock	

~17x

Assumes 2007 CLK & cores roadmap

Pentium

8080

4004

Multiple cores will continued historic "GHz" trend with a slower ramp in CLK rates

1000, 100, 10, 1, 0.1, 0.01, 0.001, 0.0001

1970, 1980, 1990, 2000, 2010, 2020, 2030

Proliferation of Cores

10000
1000
100
10
1

CPU total cores
CPU Unique cores
Consumer total cores
Consumer Unique cores

Consumer devices lead CPUs in core quantity and types

~10x

Consumer

CPU

2007 2008 2009 2010 2011 2012 2013 2014 2015 2016 2017 2018 2019 2020 2021 2022

High Speed Interfaces

SONET
SATA
XAUI
FB DIMM
Ethernet
PCIe
OIF
25Gbps standards
FC
Infiniband
SAS

PHY Bit Rate (Gb/s)

1000
100
10
1
0.1

1990 1995 2000 2005 2010 2015 2020 2025

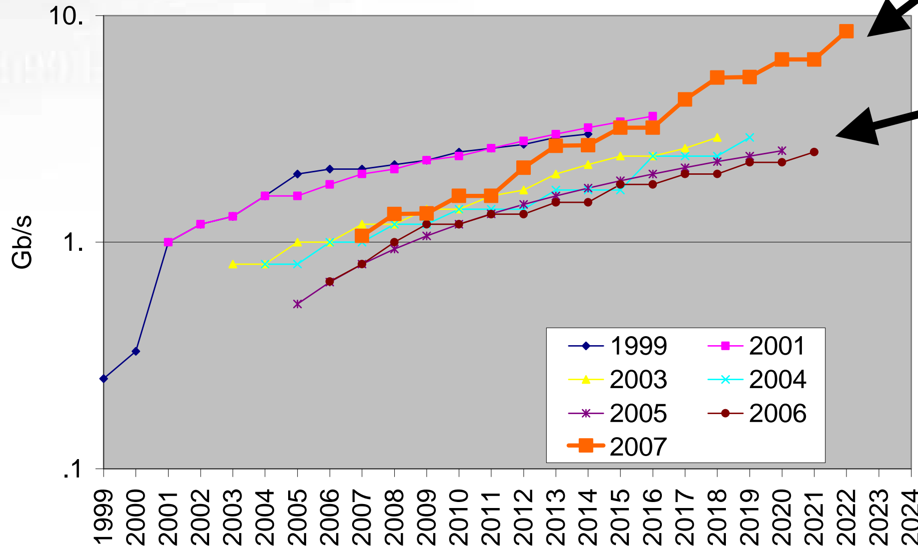
Physical Limit due to packaging and test socket

Technology Leverage Point

Test Sockets are not able to support controlled impedance contacts at >15 GT/s

- Bit bandwidth increasing – Physical limit? Test limit?

DRAM Model



2007 DDR model removed previous fcst I/O rate "flatness"

		single I/O MegaTransitions per second						
	Clk	SDR	DDR	DDR2	DDR3	DDR4	DDR5	DDR6
1997	133	133						
1998	133	133						
1999	166	166						
2000	166	166	266 333					
2001	200		400					
2002	200		400					
2003	266			400 533				
2004	333			666				
2005	333			666				
2006	400			800				
2007	533				800 1066			
2008	666				1333			
2009	666				1333			
2010	800				1600			
2011	800				1600			
2012	1066					1600 2133		
2013	1333					2666		
2014	1333					2666		
2015	1600					3200		
2016	1600					3200		
2017	2133						3200 4266	
2018	2666						5333	
2019	2666						5333	
2020	3200						6400	
2021	3200						6400	
2022	4266							6400 6532

DDR4 thru DDR6 roadmaps are pure speculation

- DDRx family trends
  - 3 primary bit rates + two optional
  - Intro year → First two speeds
- DDRx to DDRy cycles
  - 2000→2007 - 3 years
  - 2007+ - 5 years

RF

Roadmap mm-Wave Tables

0.8 GHz		2 GHz			5 GHz	10 GHz	28 GHz	77 GHz	94 GHz
GSM CDMA ISM	PDC GPS SAT Radio	DCS PCS DECT CDMA	WLAN 802.11b/g Bluetooth ZigBee	SAT TV	WLAN 802.11a	SAT TV WLAN Hyperlink UWB	LMDS WLAN	AUTO Radar	All Weather Landing

Year of Production	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*	*2014*	*2015*	*2016*	*2017*	*2018*	*2019*	*2020*	*2021*	*2022*
Carrier Frequency (GHz) Leading edge	**18**	**18**	**22**	**22**	**60**	**77**	**77**	**95**	**95**	**95**	**95**	**95**	**95**	**95**	**95**	**95**
Carrier Frequency (GHz) High Volume	**6**	**8**	**12**	**12**	**22**	**22**	**36**	**36**	**36**	**36**	**36**	**36**	**36**	**36**	**36**	**36**
Modulation RF BW (MHz) Leading edge	**80**	**528**	**528**	**528**	**528**	**528**	**528**	**528**	**528**	**528**	**528**	**528**	**1000**	**1000**	**1000**	**1000**
Modulation RF BW (MHz) High Volume	**20**	**40**	**80**	**528**	**528**	**528**	**528**	**528**	**528**	**528**	**528**	**528**	**528**	**528**	**1000**	**1000**
Amplitude Accuracy (dB)	**<0.8**	**<0.6**	**<0.5**	**<0.5**	**<0.5**	**<0.25**	**<0.25**	**<0.25**	**<0.25**	**<0.25**	**<0.25**	**<0.25**	**<0.125**	**<0.125**	**<0.125**	**<0.125**
ACLR (dB)	**65**	**65**	**70**	**72**	**72**	**72**	**75**	**75**	**80**	**80**	**80**	**85**	**85**	**85**	**85**	**85**
Number of RF Ports per Device	**<9**	**<12**	**<16**	**<20**	**<24**	**<20**	**<18**	**<16**	**<16**	**<16**	**<16**	**<16**	**<16**	**<16**	**<16**	**<16**
Phase Noise (dBc/Hz @ 100k offset)	**-125**	**-130**	**-135**	**-140**	**-142**	**-145**	**-148**	**-150**	**-150**	**-150**	**-152**	**-152**	**-152**	**-152**	**-152**	**-152**
Error Vector Magnitude 3G/4G	**1-2%**	**1-2%**	**0.5%**	**0.5%**	**0.5%**	**0.5%**	**0.5%**	**0.5%**	**0.5%**	**0.5%**	**0.5%**	**0.5%**	**0.5%**	**0.5%**	**0.5%**	**0.5%**
OIP3 (dBm)	**30**	**30**	**30**	**30**	**30**	**30**	**30**	**30**	**30**	**30**	**30**	**30**	**30**	**30**	**30**	**30**
IIP3 (dBm)	**40**	**50**	**60**	**60**	**60**	**60**	**60**	**60**	**60**	**60**	**60**	**60**	**60**	**60**	**60**	**60**

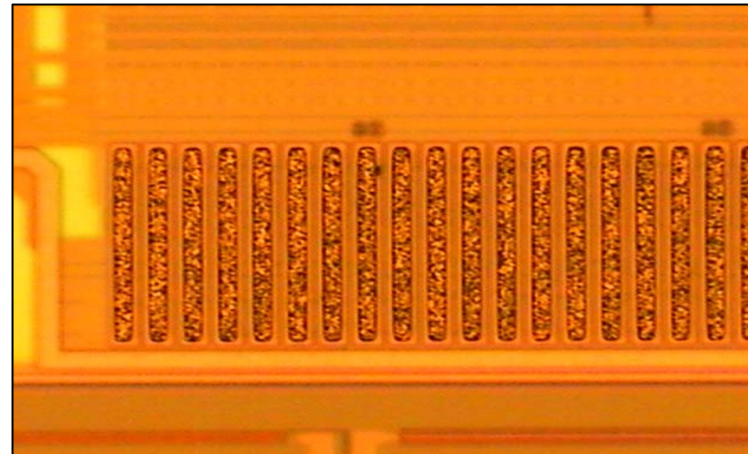
- High Frequency RF is characterized and sample tested
- >50 GHz testing is a roadblock

DUT Interface

- Probe
  - Wide range of test parallelism
    - High end logic – x1
    - NAND – Full wafer
  - Pad size requirements based on probing area & temp range
  - KGD performance test difficult – interface effects
- Sockets
  - Tables added for 2007
    - TSOP – Flash (NAND) – Contact blade
    - BGA – DRAM – Spring Probe
    - BGA – SoC – Spring Probe (50 ohm)
    - BGA – SoC – Conductive Rubber
  - Test limitations for pitch below 0.5mm and frequency > 30GHz

Specialty Devices

- LCD drivers
  - Form factor of 30mm x 1.5mm
  - Long bond pads on 20um centers
- Image sensors
  - Micro lens check with pupil test
- 3 axis MEMS Accelerometer
  - Consumer drop/rotate applications



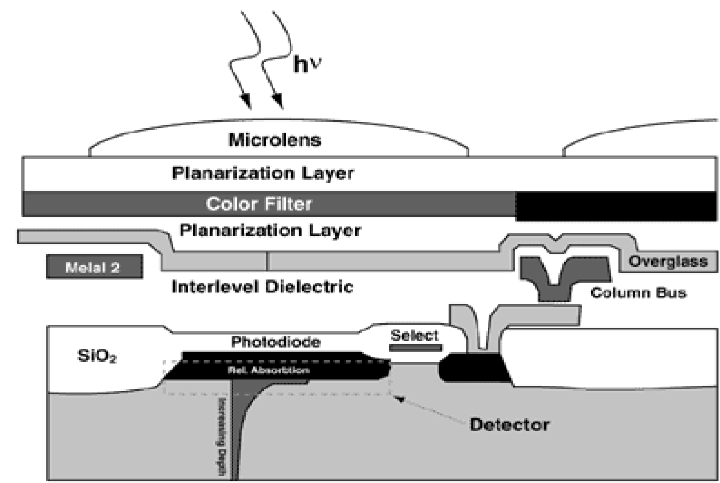


Image sensor structure cross section

Test Roadmap Issues for 2008-2009

- DFT
  - Models going forward
- More than Moore test model
  - SoC, SiP
- Test Cost
- Memory
  - Very high speed differential bus – Protocol based?
- I/O bandwidth
  - Test driven walls
- Adaptive Test

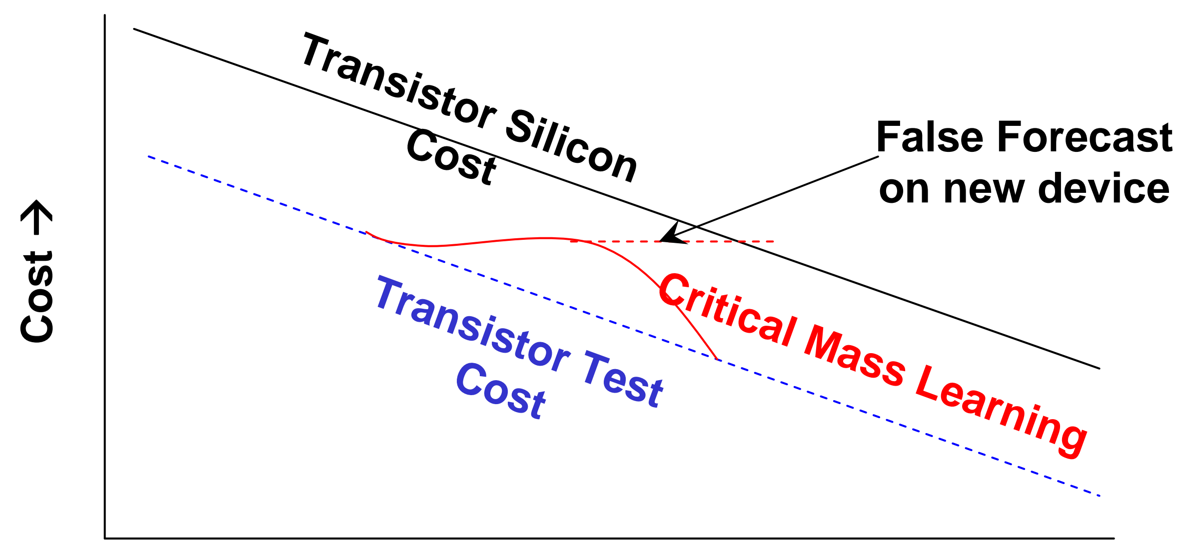
2008 Plans

- Table update only
- Plan 2009 changes
  - DFT alignment with design TWG
  - Socket performance vs. frequency
  - Expansion of specialty devices
  - Adaptive Test
  - SiP & 3D silicon Test

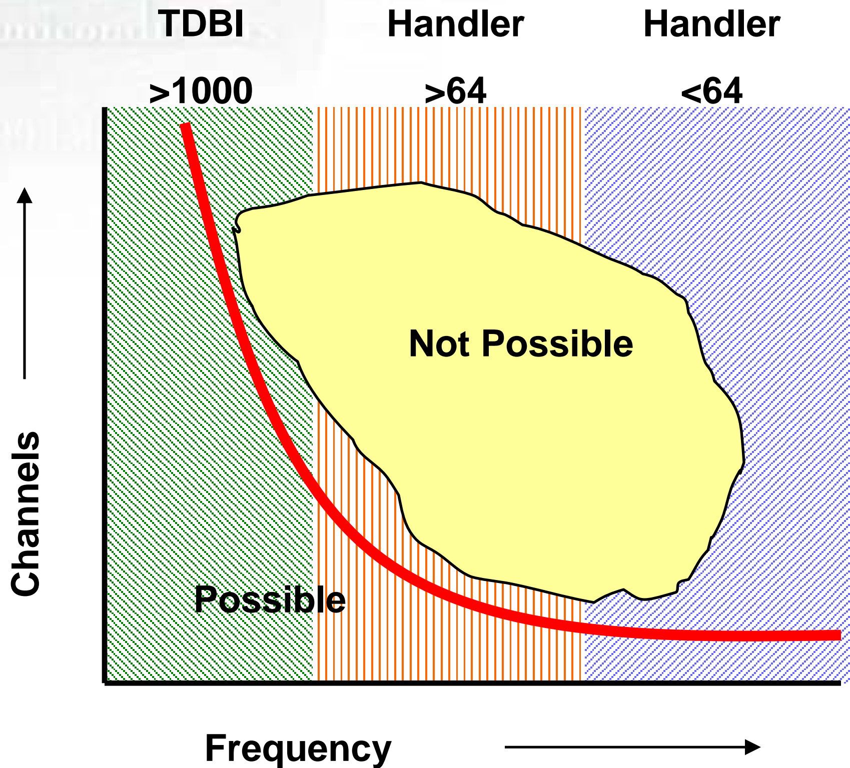
Backup

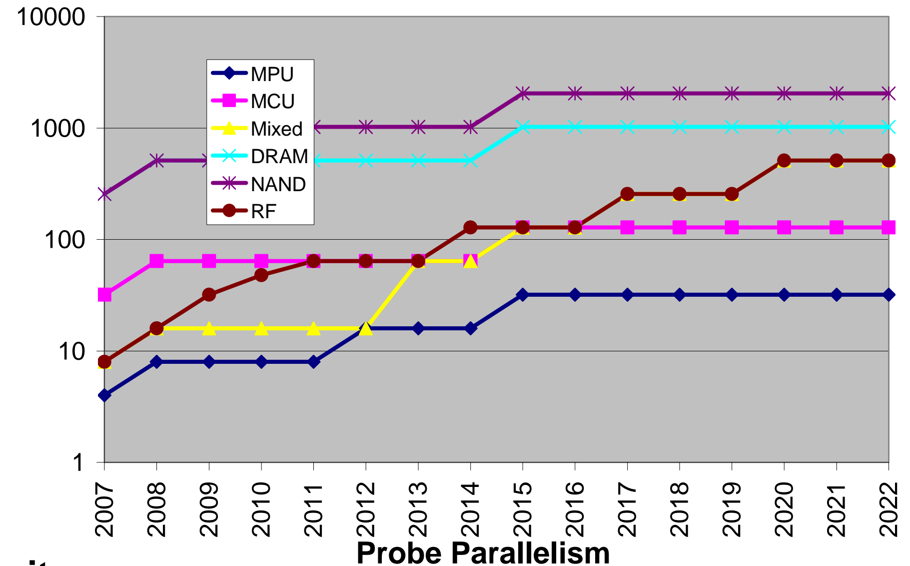
Challenge: Cost Trend

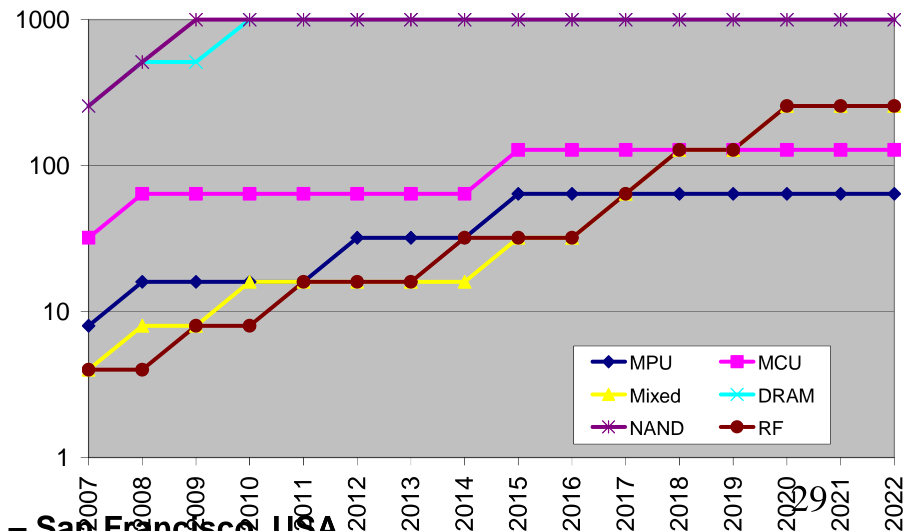
- Maintain Moore's Law learning
  - Deviations are a call to action - i.e. Functional to Structural test
- Learning curve lag on new devices, integrations or architectures
  - Low cost test methods require critical mass learning



Challenge: Limits to test parallelism







- Low Frequency: Mechanical - Cables and connections
- High Frequency: Electrical - Signal integrity
- Parallelism is a function of test time

Digital Logic Test Data Volume

Concurrent core test can reduce test data volume

Giga Pin Vectors

10,000
1,000
100
10
1

2007 2008 2009 2010 2011 2012 2013 2014 2015 2016 2017 2018 2019 2020 2021 2022

- CPU - Concurrent Core Test
- Consumer - Concurrent Core Test
- CPU - No Concurrent Test
- Consumer - No Concurrent Test

CPU

Consumer

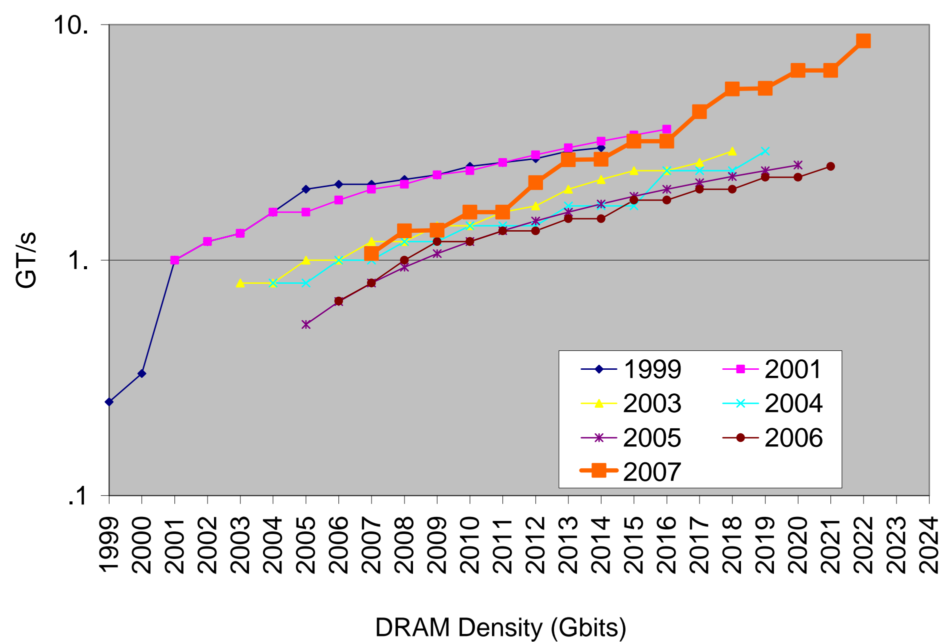
Assumes only identical cores are tested in parallel.

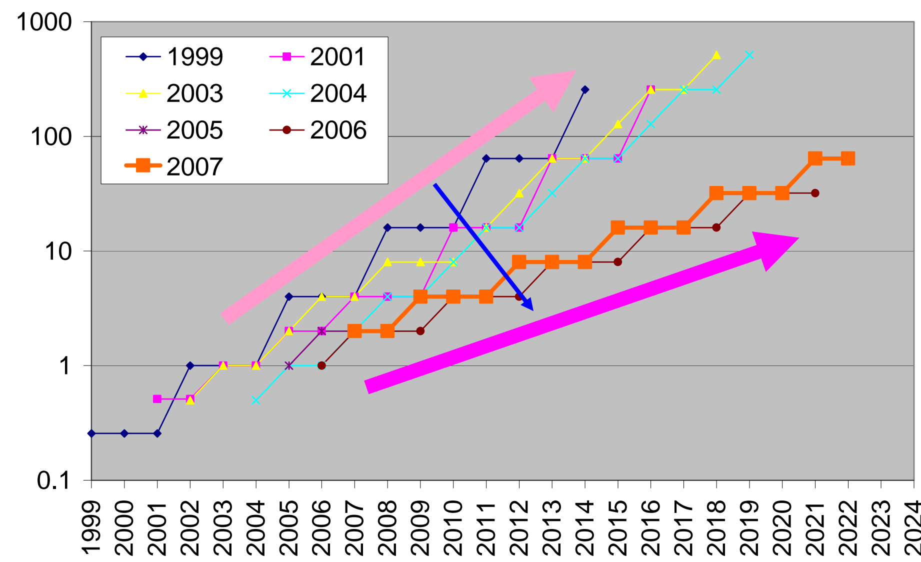
4-10x Reduction in Test Data volume with Concurrent Test

DRAM Trends

vs. Fcst

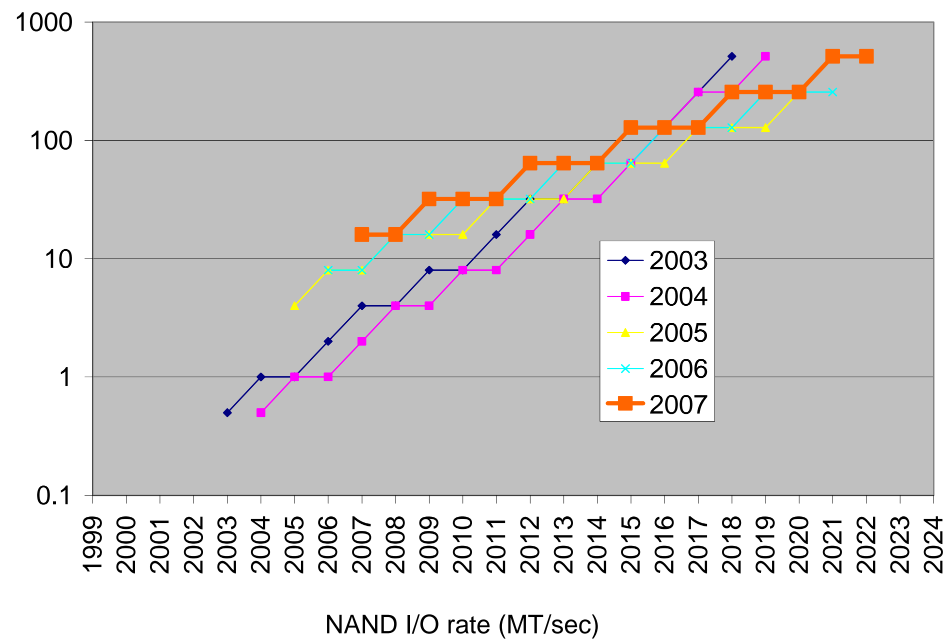
- Speculative beyond DDR3
- Cell size remains $6F^2$
- Increased I/O rate in 2007 to support revised DDR4→DDR6 model
- Density aligned to litho roadmap





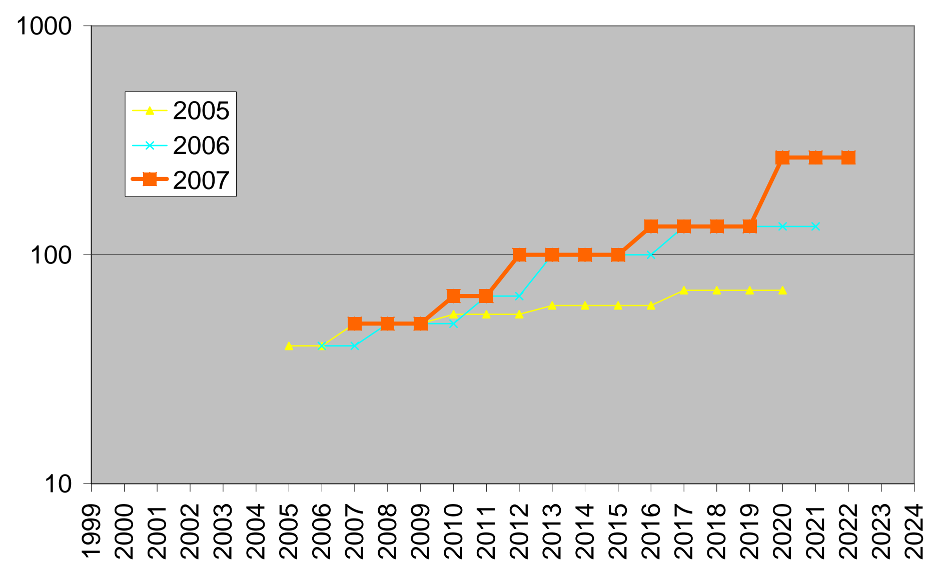
NAND Trends
vs. Fcst

- Density growth has flattened slightly
  - $4F^2$ Cell size (SBC)
  - 3 year Litho trend
  - 2 B/C assumed



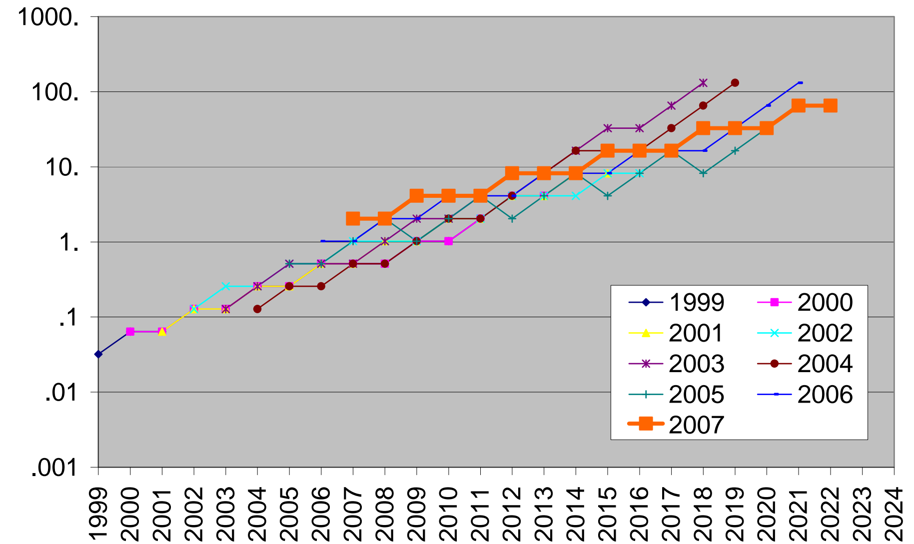
- I/O MT/s W/R rate driven

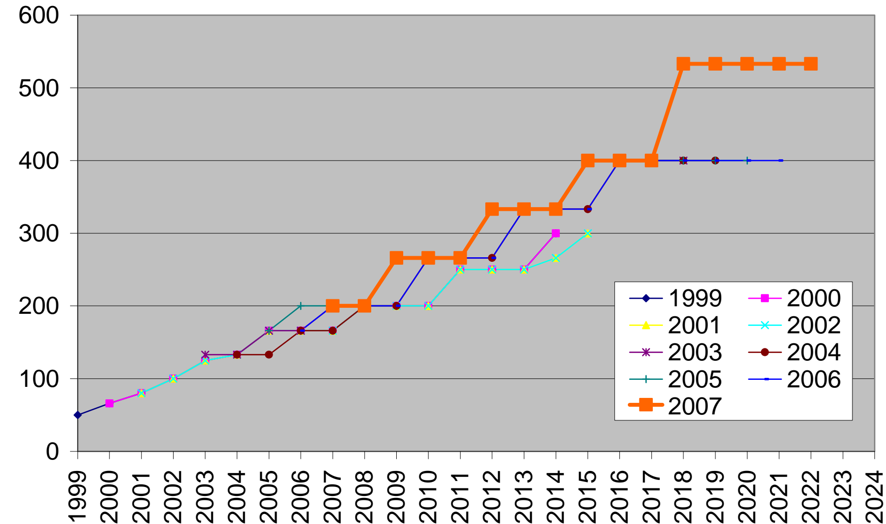
- ONFI spec
  - DDR
  - Block Abstraction
  - Common command set



NOR Trends
vs Forecasts

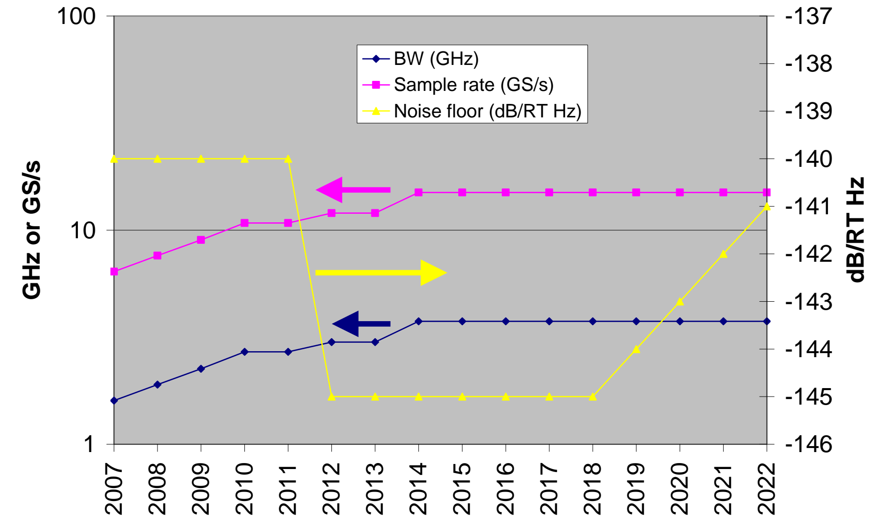
- I/O rate scaling to Cellular requirements
- Density roadmap well known
  - MLC prior to 1999
- X32 data has not appeared
  - Dropped from forecast





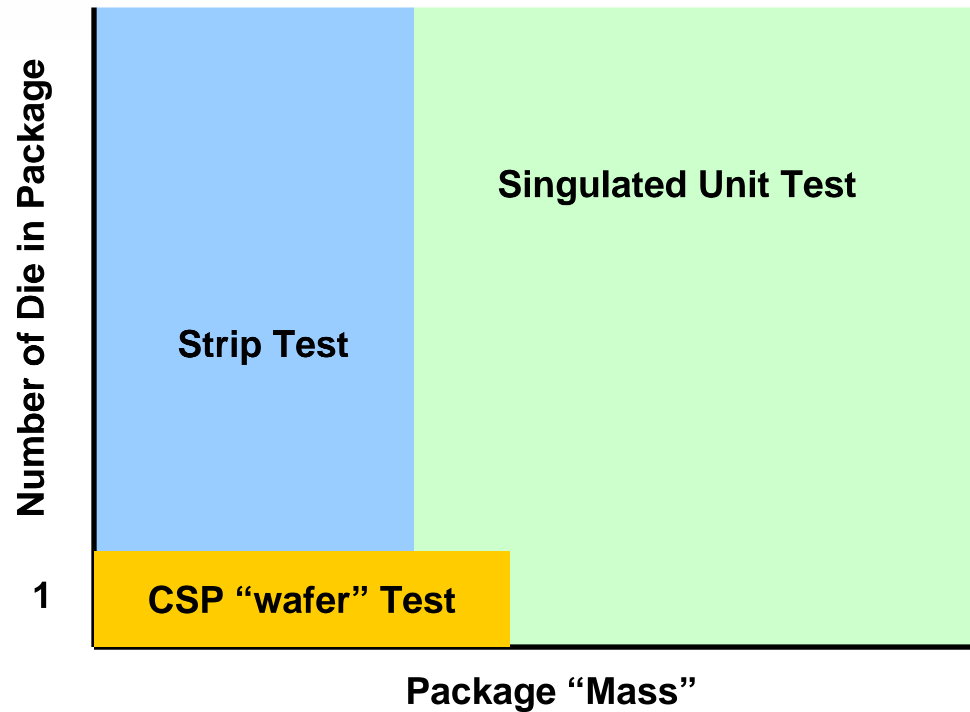
Mixed Signal

- Small changes from 2005
  - Noise floor flattened
  - Sampling rate increased



	2007	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*	*2014*	*2015*	*2016*	*2017*	*2018*	*2019*	*2020*	*2021*	*2022*
Low Frequency Waveform																
BW (MHz)	**50**	**75**	**75**	**75**	**100**	**100**	**100**	**100**	**100**	**100**	**100**	**100**	**100**	**100**	**100**	**100**
Sample rate (MS/s)	**Moving from Nyquist sample rates to over/under sampling sources/digitizers**															
Resolution (bits)	**DSP computation to 24 bits, effective number of bits limited by noise floor**															
Noise floor (dB/RT Hz)	**-155**	**-160**	**-160**	**-160**	**-165**	**-165**	**-165**	**-165**	**-165**	**-165**	**-165**	**-165**	**-165**	**-165**	**-165**	**-165**
Very High Frequency Waveform Source																
Level V (pk–pk)	**4**	**4**	<4	<4	<4	<4	<4	<4	<4	<4	<4	<4	<4	<4	<4	<4
Accuracy (±)	**0.50%**	**0.50%**	**0.50%**	**0.50%**	**0.50%**	**0.50%**	**0.50%**	**0.50%**	**0.50%**	**0.50%**	**0.50%**	**0.50%**	**0.50%**	**0.50%**	**0.50%**	**0.50%**
BW (GHz)	**1.6**	**1.9**	**2.25**	**2.7**	**2.7**	**3**	**3**	**3.75**	**3.75**	**3.75**	**3.75**	**3.75**	**3.75**	**3.75**	**3.75**	**3.75**
Sample rate (GS/s)	**6.4**	**7.6**	**9**	**10.8**	**11**	**12**	**12**	**15**	**15**	**15**	**15**	**15**	**15**	**15**	**15**	**15**
Resolution (bits) AWG/Sine†	**8/10**	**8/10**	**8/10**	**8/10**	**8/10**	**10/12**	**10/12**	**10/12**	**10/12**	**10/12**	**10/12**	**10/12**	**10/12**	**10/12**	**10/13**	**10/14**
Noise floor (dB/RT Hz)	**-140**	**-140**	**-140**	**-140**	**-140**	**-145**	**-145**	**-145**	**-145**	**-145**	**-145**	**-145**	**-145**	**-145**	**-145**	**-145**
Very High Frequency Waveform Digitizer																
Level V (pk–pk)	**4**	**4**	<4	<4	<4	<4	<4	<4	<4	<4	<4	<4	<4	<4	<4	<4
Accuracy (±)	**0.50%**	**0.50%**	**0.50%**	**0.50%**	**0.50%**	**0.50%**	**0.50%**	**0.50%**	**0.50%**	**0.50%**	**0.50%**	**0.50%**	**0.50%**	**0.50%**	**0.50%**	**0.50%**
BW (GHz) (under sampled)	**9.2**	**10.8**	**10.8**	**12.5**	**12.5**	**15**	**15**	**15**	**15**	**15**	**15**	**15**	**15**	**15**	**15**	**15**
Sample rate (GS/s)	**0.4**	**0.4**	**0.4**	**0.4**	**0.4**	**0.6**	**0.6**	**0.6**	**0.6**	**0.6**	**0.6**	**0.6**	**0.6**	**0.6**	**0.6**	**0.6**
Min resolution (bits)	**12**	**12**	**12**	**12**	**12**	**14**	**14**	**14**	**14**	**14**	**14**	**14**	**14**	**14**	**14**	**14**
Noise floor (dB/RT Hz)	**-145**	**-145**	**-145**	**-145**	**-145**	**-150**	**-150**	**-150**	**-150**	**-150**	**-150**	**-150**	**-150**	**-150**	**-150**	**-150**
Time Measurement																
Jitter measurement (ps RMS)	**Will be driven by high-speed serial communication ports**								**Will be driven by high-speed serial communication ports**							
Frequency measurement (MHz)	**Will be driven by high-performance ASIC clock rates**								**Will be driven by high-performance ASIC clock rates**							
Single shot time capability (ps)	**Will be driven by high-speed serial communication ports**								**Will be driven by high-speed serial communication ports**							

Package Size & Test



Package roadmap supports 0.2mm thickness

Singulated Unit test appears to have limits based on mass

Mechanical

- Single Prober Roadmap
  - 450mm wafers assumed in 2014

Year of Production	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*	*2014*	*2015*	*2016*	*2017*	*2018*	*2019*	*2020*	*2021*	*2022*
Wafer diameter (mm)	**300**	**300**	**300**	**300**	**300**	**300**	**300**	**450**	**450**	**450**	**450**	**450**	**450**	**450**	**450**	**450**
Wafer thickness (um)	**80–775**	**80–775**	**80–775**	**80–775**	**80–775**	**80–775**	**80–775**	**50–1000**	**50–1000**	**50–1000**	**50–1000**	**50–1000**	**50–1000**	**50–1000**	**50–1000**	**50–1000**
Maximum I/O pads	**3000**	**4000**	**4000**	**5300**	**5300**	**5300**	**5300**	**5300**	**5300**	**5300**	**5300**	**5300**	**5300**	**5300**	**5300**	**5300**
Chuck X & Y positioning accuracy (um)	**2**	**2**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**
Chuck Z positioning accuracy (um)	**1**	**1**	**0.5**	**0.5**	**0.5**	**0.5**	**0.5**	**0.5**	**0.5**	**0.5**	**0.5**	**0.5**	**0.5**	**0.5**	**0.5**	**0.5**
Probe-to-pad alignment (µm)	**4.5**	**4.5**	**4.5**	**3.5**	**3.5**	**3.5**	**3.5**	**3.5**	**3.5**	**3.5**	**3.5**	**3.5**	**3.5**	**3.5**	**3.5**	**3.5**
Maximum chuck force (kg)	**100**	**100**	**100**	**100**	**100**	**100**	**100**	**100**	**100**	**100**	**100**	**100**	**100**	**100**	**100**	**100**
Set point range (°C)	**-30 to +85**	**-30 to +85**	**-30 to +85**	**-45 to +125**	**-45 to +125**	**-45 to +125**	**-45 to +125**	**-45 to +125**	**-45 to +125**	**-45 to +125**	**-45 to +125**	**-45 to +125**	**-45 to +125**	**-45 to +125**	**-45 to +125**	**-45 to +125**
Total power (Watts)	**130**	**130**	**250**	**250**	**250**	**250**	**250**	**250**	**250**	**250**	**250**	**250**	**250**	**250**	**250**	**250**
Power density (Watt/cm^2)	**60**	**60**	**120**	**120**	**120**	**120**	**120**	**120**	**120**	**120**	**120**	**120**	**120**	**120**	**120**	**120**

- Three handler groups
  - High power - > 10W
    - Low parallelism: < 4
  - Medium Power → 0.5 to 10W
    - Medium parallelism: < 16
  - Low Power → < 0.5W (Memory, MCU, etc)
    - High parallelism: <250