Modeling and Simulation ITWG

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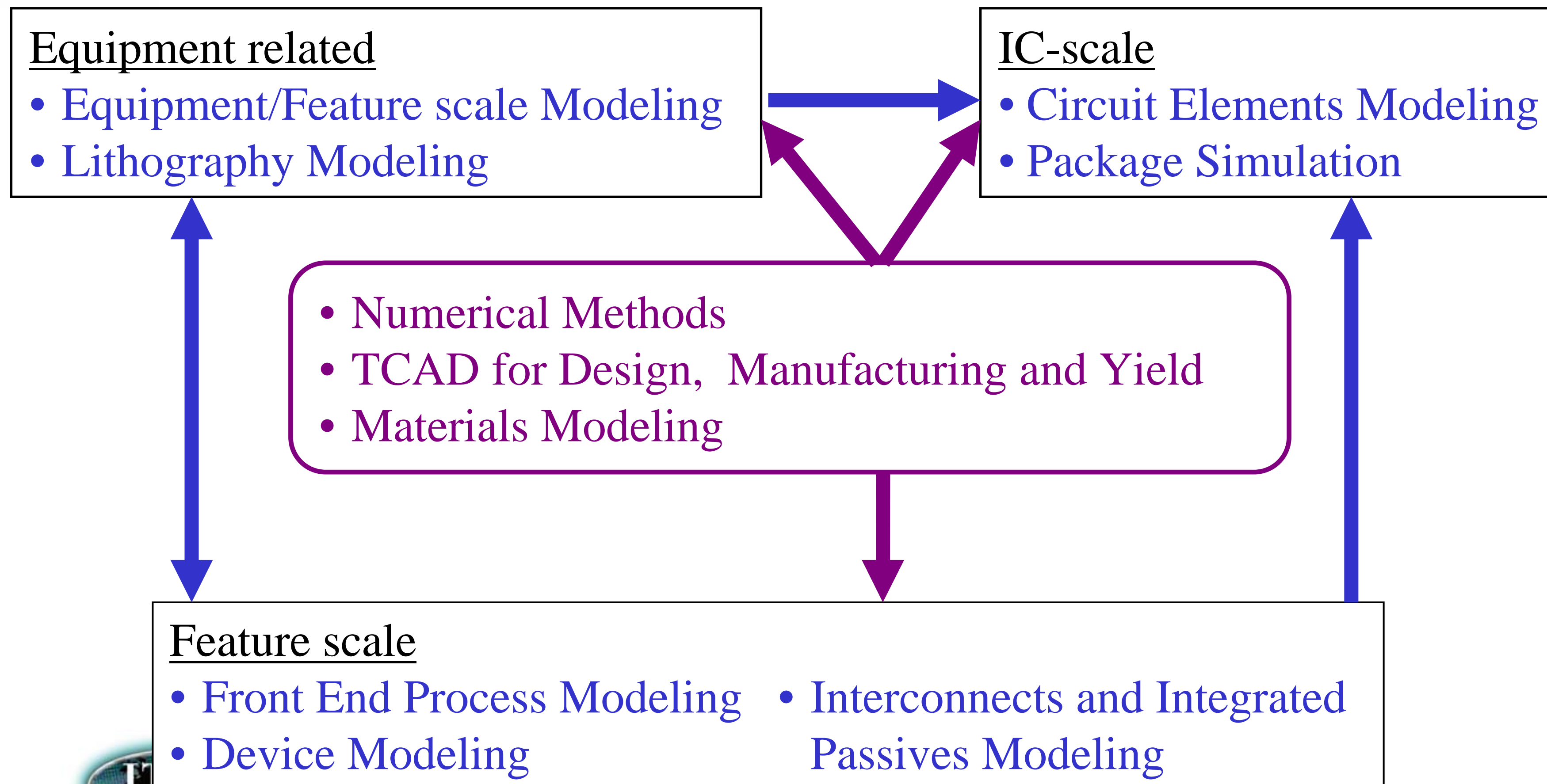
2008 Modeling & Simulation SCOPE & SCALES

Modeling Overall Goal

- Support technology development and optimization
- Reduce development times and costs



Key Messages (I)

- Mission of Modeling and Simulation as cross-cut topic:
  Support areas covered by other ITWGs
  ⇒ Continued in-depth analysis of M&S needs of other ITWGs, based on documents + inter-ITWG discussions – holds also for 2008
  ⇒ Strong links with ALL ITWGs – see also crosscut texts in 2007 ITRS
- Modeling and simulation provides an 'embodiment of knowledge and understanding'. It is a tool for technology/device development and optimization and also for training/education
- Technology modeling and simulation is one of a few methods that can reduce development times and costs:
  - 2008 major action on assessment of industrial use of TCAD and reduction of development times and costs in best-practice cases

Key Messages (II)

- Art of modeling:
  - Combine dedicated experiments & theory to reveal physical mechanisms & extract parameters
  - Find appropriate trade-off between detailed physical simulation (CPU and memory costly) and simplified but physically appropriate approaches
- Accurate experimental characterization methods are essential
- Reliable experimental reference data required on all levels – profiles, electrical data, ….. – must partly be provided e.g. by device makers!
- Further growing importance of atomistic/materials/hierarchical/multilevel simulation - appropriate treatment of nanostructures
- Ongoing invitation for extended participation
  - also include suppliers (equipment and software)

Example for Success Cases (I)

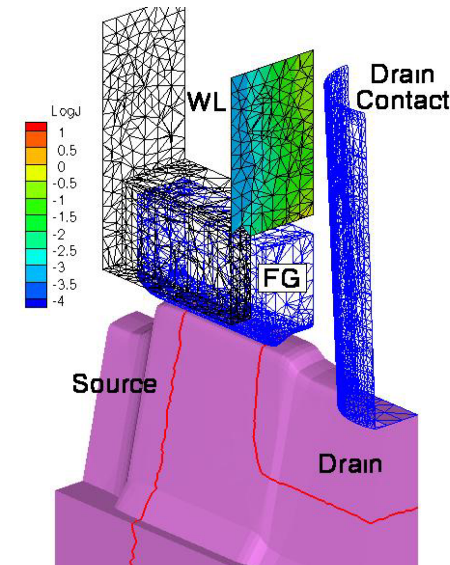
NOR Flash Reliability: Contact-Gate Leakage

Requirements met during simulation:

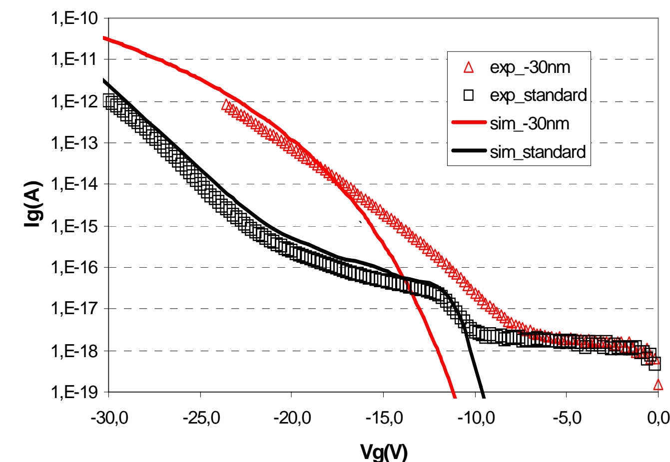
- Accurate 3D description of memory cell morphology
- Leakage through non-planar multi-layer dielectric stack
- 3D non-local tunneling model to account for local curvature radii
- Floating Gate charging during measurement

Main results:

- Sound interpretation of physical mechanisms involved
- Lateral trap-assisted conduction dominates for aggressively scaled contact-gate distance
- Guidelines for reliable scaling of NOR cell

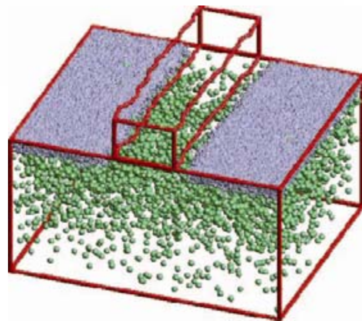


Source: STMicroelectronics Agrate (IRPS 2007)



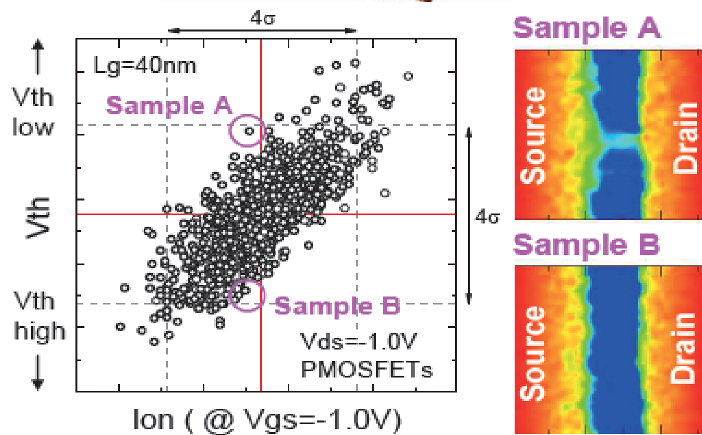
Examples for Success Cases (II)

SRAM critical yield evaluation based on comprehensive physical / statistical modeling, considering anomalous non-Gaussian intrinsic transistor fluctuations

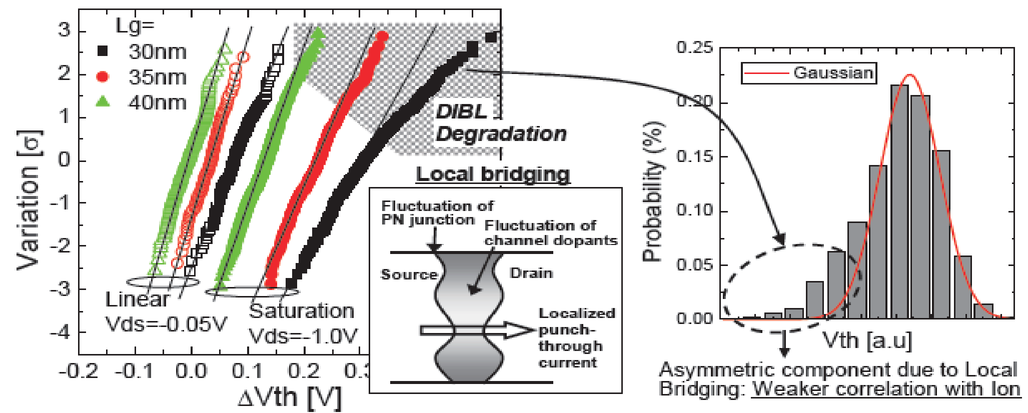


VL2007, 3A-1 M. Miyamura et. al.,*NEC*

Typical atomistic process simulation incorporating random discrete dopant atoms and LWR as the source of intrinsic fluctuation



Typical examples of large-V_{th}-deviation with almost identical I_{on}



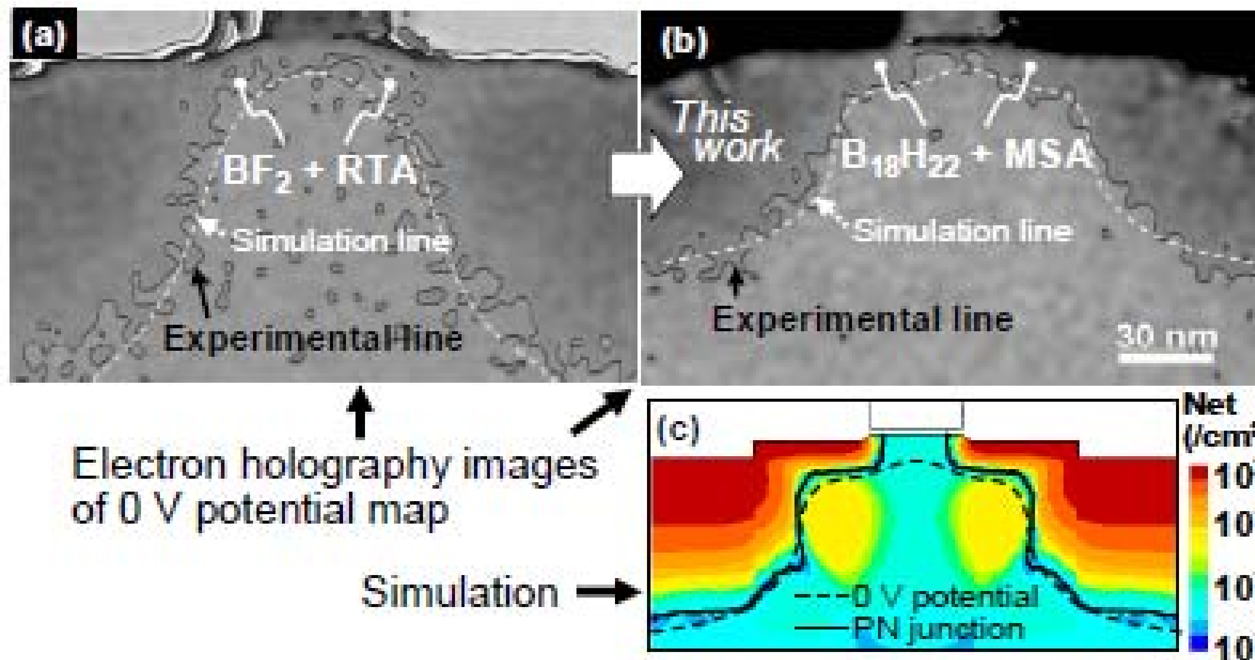
V_{th} distribution
DIBL degradation for shorter L_g

V_{th} distribution
showing non-Gaussian tail

Atomistic-3D-TCAD predicts the non-Gaussian Vth-distribution

Example for Success Cases (III)

Pushing Planar Bulk CMOSFET Scaling to its Limit by Ultimately Shallow Diffusion-Less Junction



IEDM2007 -
K. Uejima et. al.,
NEC,NECEL

Cross-sectional 0 V potential maps of PFETs fabricated (a) by conventional spike RTA process and (b) by msec annealing (MSA) . The electron holography imaging has proven device concept based on predictive TCAD simulation (c): 0V-potential line by electron holography agrees with simulated one

Basic Approach and Focus of 2008 Work

1) Detailed cross-cuts worked out since 2003 – regularly updated together with other ITWGs – continued in 2008 as input to table update and preparatiom for 2009

2) Detailed revision of M&S tables based on state-of-the-art & cross-cut requirements – several details traced but shifted to 2009 text

3) Major action on assessment of use of TCAD in companies:
   - WWW questionnaire worked out and distributed to industrial TCAD users (NOT to developers!)
   - So far about 140 replies received
   - Results being used for update of cost reduction estimate & as input to 2009 work

Main Changes in 2008 Challenges

Short-term challenges:

- In challenge “Ultimate nanoscale device simulation capability”:
    - New item “Treatment of individual dopant atoms and traps in (commercial) continuum and MC device simulation”
    - Item “Models for device impact of statistical fluctuations in structures and dopant distribution” skipped because quite similar to another item
- New item “Thermal modeling for 3D ICs and assessment of modeling tools capable of supporting 3D designs. Thermo-mechanical modeling of Through Silicon Vias and thin stacked dies, and their impact on active device properties (stress, expansion, keepout regions, …). “ in challenge “Thermal-mechanical-electrical modeling for interconnections and packaging”

Long-term challenges:

- Challenge “Nano-scale modeling for Emerging Research Devices including Emerging Research Materials” extended to also include interconnects. Additional item added on “Modeling impact of geometry, interfaces and bias on transport for carbon-based nanoelectronics” to second item.

General: Some changes in the details of the issues (blue/red in viewfoils)

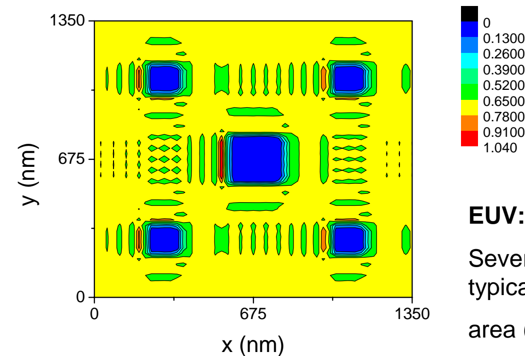
2008 Short-Term Difficult Challenges- so far no changes compared to 2007

Lithography Simulation including EUV

Needs

- Experimental verification and simulation of ultra-high NA vector models, including polarization effects from the mask and the imaging system
- Models and experimental verification of non-optical immersion lithography effects (e.g. topography and change of refractive index distribution)
- Simulation of multiple exposure/patterning
- Multi-generation lithography system models
- Simulation of defect influences / defect printing
- Optical simulation of resolution enhancement techniques including combined mask/source optimization (OPC, PSM) and including extensions for inverse lithography
- Models that bridge requirements of OPC (speed) and process development (predictive) including EMF effects and ultra-high NA effects (oblique illumination)
- Predictive resist models (e.g. mesoscale models) incl. line-edge roughness, etch resistance, adhesion, mechanical stability, and time-dependent effects in multiple exposure
- Resist model parameter calibration methodology (including kinetic and transport parameters)
- Simulation of e-beam mask making
- Simulation of direct self-assembly of sublitho patterns
- Modeling lifetime effects of equipment and masks

Example (Fraunhofer IISB):
Near-field intensity simulated on 1.9 Ghz laptop for large area with waveguide method and decomposition technique

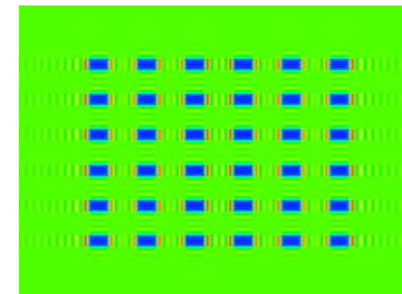


EUV:

Several absorbers on typical multilayer,

area $(100\ \lambda)^2$,

simulation time 20 sec.



193 nm optical:

Several absorbers on CoG mask,

area $(52\ \lambda)^2 = 10\mu m \cdot 10\mu m$,

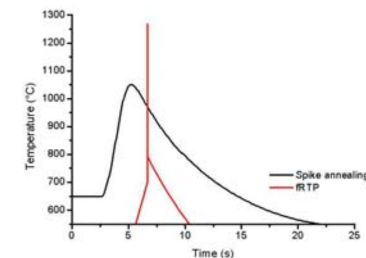
simulation time 17 min.

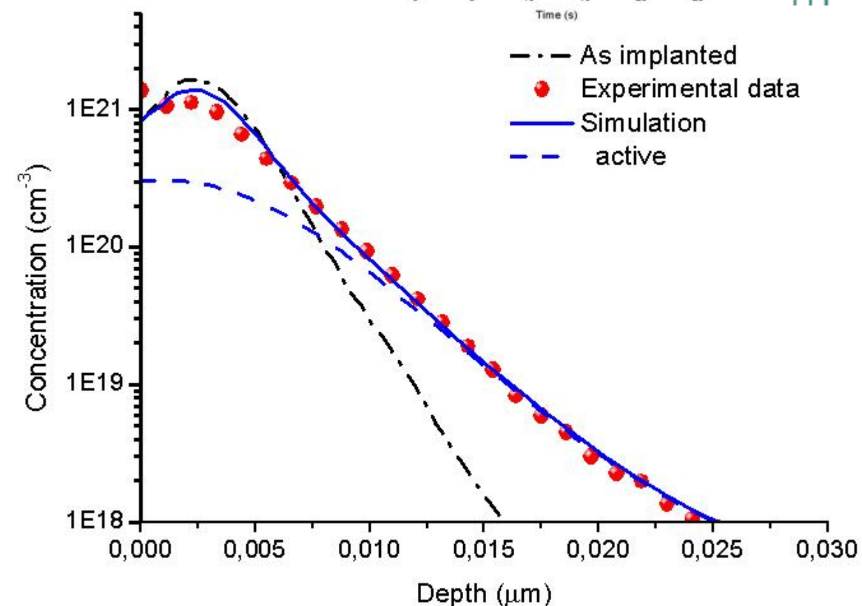
2008 Short-Term Difficult Challenges – changes from 2007 in blue

Front-End Process Modeling for Nanometer Structures

Needs

- Coupled diffusion/activation/damage/stress models and parameters incl. SPER and millisecond processes in Si-based substrate, that is, Si, SiGe:C, Ge, GaAs, SOI, epilayers and ultra-thin body devices, taking into account possible anisotropy in thin layers
- Modeling of epitaxially grown layers: Shape, morphology, stress
- Modeling of stress memorization (SMT) during process sequences
- Characterization tools/methodologies for ultra-shallow geometries/junctions, 2D low dopant level, and stress
- Modeling hierarchy from atomistic to continuum for dopants and defects in bulk and at interfaces
- Efficient and robust 3D meshing for moving boundaries
- Front-end processing impact on reliability





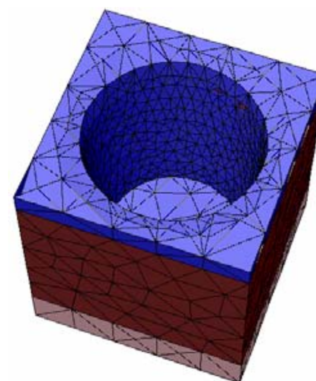
Source: P. Pichler et al. (FhG-IISB), Defect and Diffusion Forum 258-260, 510 (2006)

2008 Short-Term Difficult Challenges

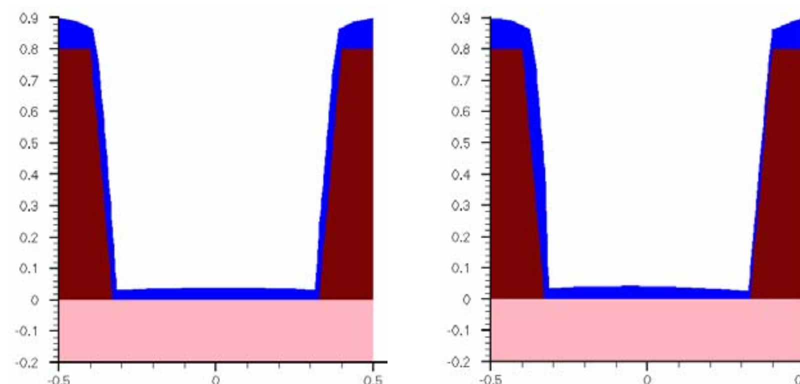
Integrated Modeling of Equipment, Materials, Feature Scale Processes and Influences on Devices – no changes compared to 2007

Needs

- Fundamental physical data (e.g. rate constants, cross sections, surface chemistry for ULK, photoresists and high-k metal gate); reaction mechanisms (reaction paths and (by-)products, rates ...) , and simplified but physical models for complex chemistry and plasma reaction
- Linked equipment/feature scale models (including high-k metal gate integration, damage prediction)
- Removal processes: CMP, etch, electrochemical polishing (ECP) (full wafer and chip level, pattern dependent effects)
- Deposition processes: MOCVD, PECVD and ALD, electroplating and electroless deposition modeling
- Efficient extraction of impact of equipment- and/or process induced variations on devices and circuits, using process and device simulation



Simulated across-wafer variation of feature profile for a sputter-deposited barrier.



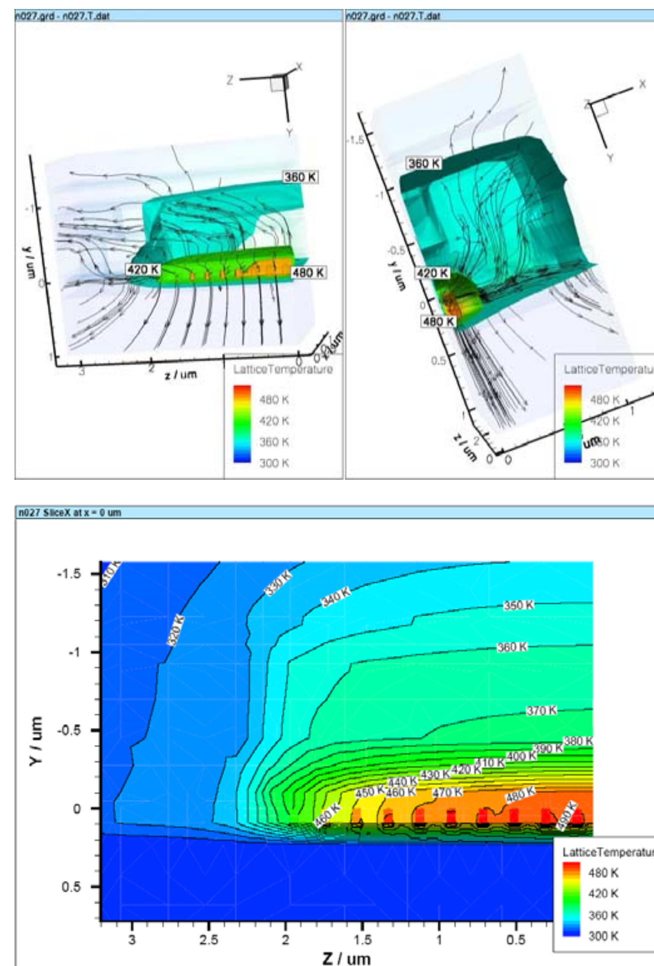
(From Fraunhofer IISB)

2008 Short-Term Difficult Challenges

Ultimate Nanoscale Device Simulation Capability – changes from 2007 in blue/red

Needs

- Methods, models and algorithms that contribute to prediction of CMOS limits
- General, accurate, computationally efficient and robust quantum based simulators incl. fundamental parameters linked to electronic band structure and phonon spectra
- Models and analysis to enable design and evaluation of devices and architectures beyond traditional planar CMOS
- Models (incl. material models) to investigate new memory devices like MRAM, PCRAM/PRAM, etc
- Gate stack models for ultra-thin dielectrics
- SKIPPED (because quite similar to next item): Models for device impact of statistical fluctuations in structures and dopant distributions
- Efficient device simulation models for statistical fluctuations of structure and dopant variations and efficient use of numerical device simulation to assess the impact of variations statistics on statistics of device performance.
- Physical models for novel materials, e.g. high-k stacks, Ge and compound III/V channels ….: Morphology, band structure, defects/traps, ….
- Treatment of individual dopant atoms and traps in (commercial) continuum and MC device simulation
- Reliability modeling for ultimate CMOS
- Physical models for stress induced device performance



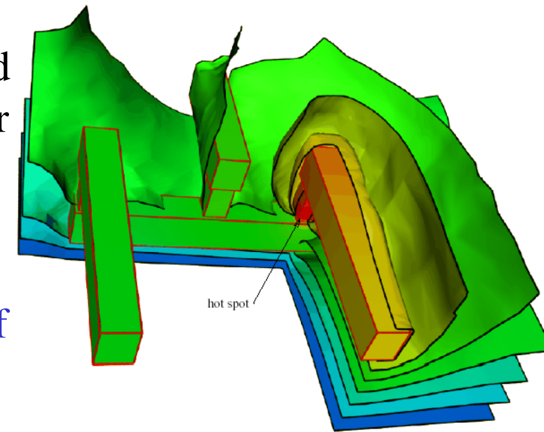
Lattice temperatures in device
Source: Infineon / ESSDERC 2006

2008 Short-Term Difficult Challenges

Thermal-Mechanical-Electrical Modeling for Interconnects and Packaging – changes from 2007 in blue/red

Needs

- Model thermal-mechanical, thermodynamic and electrical properties of low-k, high-k and conductors for efficient on-chip and off-chip incl. SIP ~~layout and~~ and wafer level packages, including power management, and the impact of processing on these properties especially for interfaces and films under 1 micron
- Thermal modeling for 3D ICs and assessment of modeling tools capable of supporting 3D designs. Thermo-mechanical modeling of Through Silicon Vias and thin stacked dies, and their impact on active device properties (stress, expansion, keepout regions, …).
- Model effects which influence reliability of packages and interconnects incl. 3D integration (e.g. stress voiding, electromigration, fracture, dielectric breakdown, piezoelectric effects)
- Models to predict adhesion on interconnect-relavant interfaces (homogeneous and heterogeneous)
- Simulation of adhesion and fracture toughness characteristics for packaging and die interfaces
- Models for electron transport in ultra fine patterned interconnects



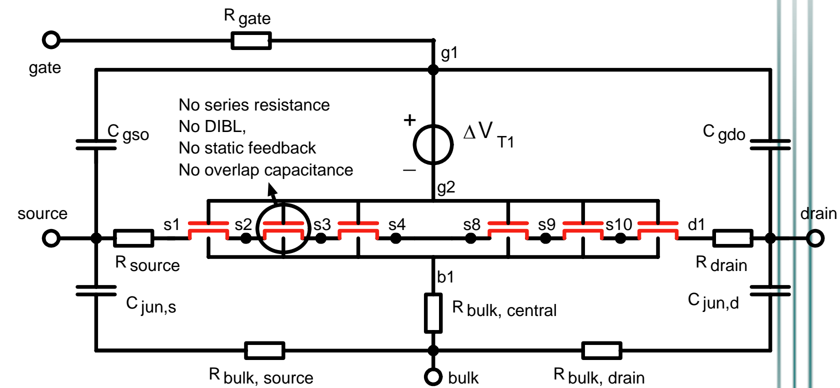
courtesy TU Vienna / IST project MULSIC

Temperature distribution in an interconnect structure

2008 Short-term Difficult Challenges

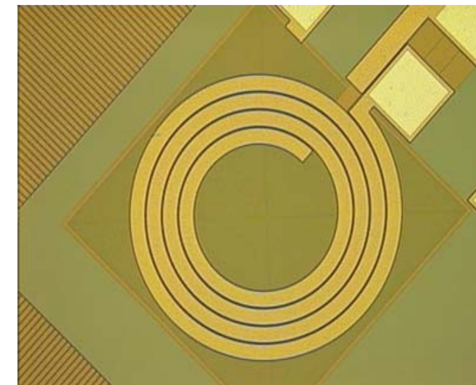
Circuit Element and System Modeling for High Frequency (up to 160 Ghz) Applications

- No change from 2007



Needs

- Supporting heterogeneous integration (SoC+SiP) by enhancing CAD-tools to simulate mutual interactions of building blocks, interconnect, dies and package:
  - possibly consisting of different technologies,
  - covering and combining different modelling and simulation levels as well as different simulation domains
- Scalable active component circuit models including non-quasi-static effects, substrate noise, high-frequency and 1/f noise, temperature and stress layout dependence and parasitic coupling
- Scalable passive component models for compact circuit simulation, including interconnect, transmission lines, RF MEMS switches, …
- Physical circuit element models for III/V devices
- Computer-efficient inclusion of variability including its statistics (including correlations) before process freeze into circuit modeling, treating local and global variations consistently
- Efficient building block/circuit-level assessment using process/device/circuit simulation, including process variations



(From Philips)

2008 Difficult Challenges < 22 nm

Table 122 Modeling and Simulation Difficult Challenges

Difficult Challenges < 22 nm	*Summary of Issues*
Modeling of chemical, thermomechanical and electrical properties of new materials	Computational materials science tools to predict materials synthesis, structure, properties, process options, and operating behavior for new materials applied in devices and interconnects, including especially for the following:
	1) Gate stacks: Predictive modeling of dielectric constant, bulk polarization charge, surface states, phase change, thermomechanical (including stress effects on mobility), optical properties, reliability, breakdown, and leakage currents including band structure, tunneling from process/materials and structure conditions.
	2) Models for novel integrations in 3D interconnects including airgaps and data for ultrathin material properties. Models for new ULK materials that are also able to predict process impact on their inherent properties
	3) Linkage between first principle computation, reduced models (classical MD or thermodynamic computation) and metrology including ERD and ERM applications. Modeling-assisted metrology.
	4) Accumulation of databases for semi-empirical computation.
Nano-scale modeling for Emerging Research Devices and Interconnects including Emerging Research Materials	~~Process~~ Ab-initio materials modeling tools for the development of novel nanostructure devices (nanowires, carbon nanotubes (including doping), nano-ribbons (graphene), quantum dots, ~~molecular~~ atomic electronics, multiferroic materials and structures, strongly correlated electron materials) Device modeling tools for analysis of nanoscale device operation (quantum transport, tunneling phenomena, contact effects, spin transport, …). Modeling impact of geometry, interfaces and bias on transport for carbon-based nanoelectronics
Optoelectronics modeling	Materials and process models for on-chip/off-chip optoelectronic elements (transmitters and receivers, optical couplers). Coupling between electrical and optical systems, optical interconnect models, semiconductor laser modeling. Physical design tools for integrated electrical/optical systems
NGL simulation	• Simulation of mask less lithography by e-beam direct write (shaped beam / multi beam), including advanced resist modeling (low activation energy effects for low-keV writers (shot noise effects & impact on LER); heating and charging effects), including impact on device characteristics (e.g. due to local crystal damage by electron scattering or charging effects) • Simulation of nano imprint technology (pattern transfer to polymer = resist modeling, etch process)

2008 Requirement Tables

Only some general remarks here:

- Continued trend to delay items: Necessary research could not be done due to lack of resources (research funding)
- Many changes in technical details included
- Table continues to contain some items in “zebra” colour - according to ITRS guidelines: “Limitations of available solutions will not delay the start of production. In some cases, work-arounds will be initially employed. Subsequent improvement is expected to close any gaps for production performance in areas such as process control, yield, and productivity.“

  ⇒ This means for simulation: It can be used, but with more calibration, larger CPU time/memory, less generality than in the end required ...
- Red here means “Solution not known, but this does not stop manufacturing”

2008 Short-Term Requirements

	Year of Production	2007	2008	2009	2010	2011	2012	2013	2014	2015
	DRAM ½ Pitch (nm) (contacted)	65	57	50	45	40	36	32	28	25
	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	68	59	52	45	40	36	32	28	25
	MPU Physical Gate Length (nm)	25	23	20	18	16	14	13	11	10
	Lithography									
IS	Exposure	Simulation of immersion lithography for high NA liquids (NA about 1.5) [1]		Simulation of EUV incl. optical flare, optical lithography for very high NA (about 1.7), ML2, imprint lithography options; models bridging OPC and predictive feature scale simulation [2]			NGL models and modeling of materials and components (~~immersion,~~ EUV, ML2 lithographic processes, imprint)			
IS	Resist models	Predictive chemically amplified resist models including LER and immersion (liquid-solid interface), and methods to easily calibrate parameters. Multiple exposure and lithography on topography		~~Multiple exposure;~~ EUV resists; finite polymer-size effects; line collapsing; ~~lithography on topography;~~ coupling with etch models		Meso-scale resist models with finite molecule effects; resist flare			Models for non-conventional photoresists ~~models~~ and coupling with etch models	
IS	Large area lithography simulation*	TCAD-based methods to detect weak spots in lithography and etching across chip ~~whole exposure field *~~			TCAD-based inverse lithography modeling					
	Front End Process Modeling									
IS	Gate stack*	◆ High-κ dielectrics and gate materials (interfaces, impurity diffusion, electrical barrier) [3]		Model material properties and electrical behavior of prioritized alternative dielectrics (e.g. Hf-based) and gates (interfaces, defects, impurities, stress, work function and band gap offset, mobility, leakage - incl. metal gates and FUSI) [4]					Modeling of new process steps / processing and properties of alternative materials	
	Continuum diffusion and activation models	Calibration of present models for Si based materials incl. stress/strain,silicidation and new annealing steps (e.g. millisecond anneal)		Refined and predictive models with better accuracy for upcoming process steps and applications						
	Atomistic modeling for activation and diffusion*	◆ Speedup of Kinetic Monte-Carlo		Inclusion of stress, extension to other materials used in active device, calibration of atomistic modeling on first-principle calculations and experiments, integration with continuum process simulation						
	Topography and Material Modeling [5]									
	Etching / deposition	(Surface) physics based feature scale models (incl. redeposition and stress)		Integration of feature-scale simulation with equipment (plasma) models; electrical properties and stress incl. microstructure in deposition; layout dependence; process integration (coupling of etch-deposition-plating-CMP-lithography)			Including data beyond topography to also include surface and sub-surface material property prediction, full molecular dynamcs (or atomistic) feature scale models			
	Alternative material modeling	Calculation of thermodynamic and electronic properties		Calculation of mechanical properties; process impact on intrinsic material behavior, integrity and electrical performance under strain						
	Equipment impact on process results including material properties				Computer engineered materials and process recipes; predictive manufacturability and yield; full process integration models. Integrated equipment/feature scale modeling extended to include material information from the atomic scale					
	Numerical Device Modeling [6]									

2008 Short-Term Requirements (cont.)

	Transport modeling [7]	Orientation-dependent mobility models incl. field-dependent non-linear strain effects, surface roughness effects of nitrided oxides and orientation of the channel		Mobility models for high-κ gate stacks; efficient inclusion of quasi-ballistic transport		Mobility models consistent with QM confinement in thin films (esp. SOI)				
	Additional requirements for non-classical CMOS	Device models to include additional interfaces (esp. w.r.t. mobility in thin films)		Efficient quantum-mechanical simulation of 3D device structures, including thin films, consistent with mobility models					Nanoscale simulation capability including accurate atomistic and quantum effects	
IS	Novel devices *	◆ Single-cell modeling of MRAMs, PCMs, FeRAMs and SONOS/NROMs		Material properties and reliability modeling of novel memory devices			Modeling of nanowires, carbon-based nanoelectronics ~~graphene, etc.~~ and spin-based devices			
IS	Reliability and noise modeling	HF, 1/f and RTS noise modeling		Trap generation during operation (HCI, NBTI, PBTI, ….) for conventional and new gate stacks						
	Circuit Component Modeling [8]									
IS	Active devices*	Compact models for non-classical CMOS/ non-quasi-static models for CMOS		Circuit models for non-classical CMOS devices including reliability and influences of statistics; circuit models for classical CMOS devices including inhomogeneous doping and quasi-ballistic effects; include models for self-heating					Circuit models for nanoscale devices and interconnects	
IS	Interconnects and integrated passives*	Hierarchical process-aware full chip RLC [10]		Include em-coupling ~~self-healing~~ and reliability					Include self-healing	
	Process and materials impact on electricalperformance of interconnects *	◆ Models that relate material properties (process related or fundamental) to electron transport (e.g. in conducting lines). Includes models for electron scattering. Models that predict paths to material property repair (e.g. low κ repair, capacitance repair)								
ADD	Heterogeneous integration				Include EM and thermal coupling in device models		Robust and rapid construction of behavioural models of building blocks or subcircuits	Include EM and thermal coupling between building blocks		
	Package Modeling									
	Electrical modeling*	◆ Unified RLC extraction and multiscale modeling for package / chips		Reduced order models		Full-wave analysis		Mixed electrical/optical analysis		
	Thermal-mechanical modeling *	◆Thermo-mechanical-integrated models	◆ Include non-bulk and porous/air gap materials properties		Include reliability (esp. life prediction)					
IS	Material properties *	◆ Improved material models (visco-elasticity, creep, plasticity), interfaces								
IS	*General requirements on tools*									
	Meshing *	◆ Robust, reliable, efficient and user-friendly 3D grid generation including moving boundaries								
	Algorithms	More robust and more parallelizable algorithms		Discretization schemes alternative e.g. to box methods		Efficient atomistic/quantum methods; ab-initio or molecular dynamics based topography simulations				
ADD	Tool interoperability	Documented file formats		Open documented file formats (synatax and semantics), exchangability of data between different tools						

More details given in tables & ITRS text

Thank you