Metrology Roadmap

2008

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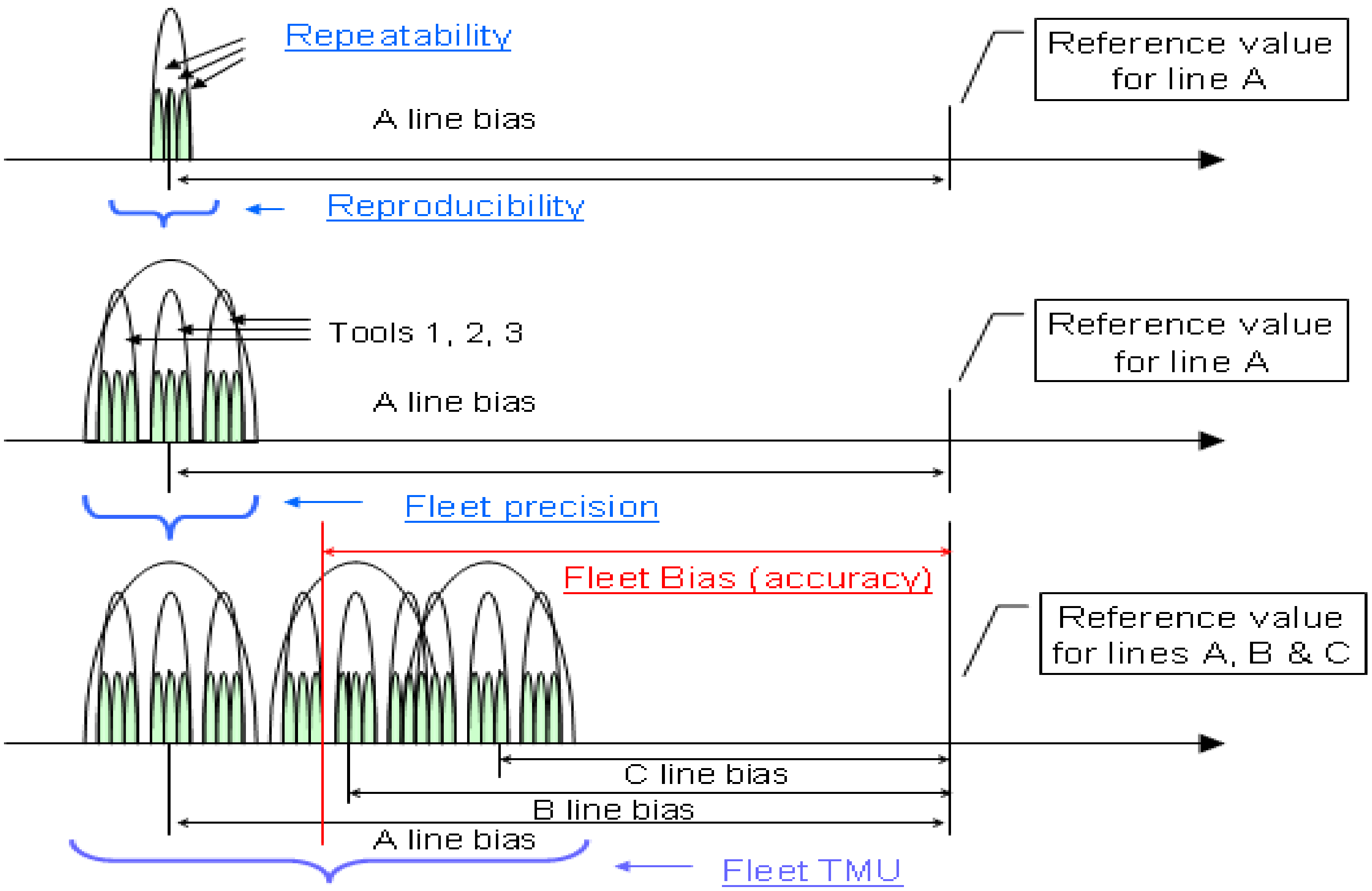
AGENDA

- 2008 Changes
- Lithography Metrology
- FEP Metrology
- Interconnect Metrology
- ERM Metrology
- Key Messages 2008
- Conclusions

2008 ITRS Changes

		2008	2010	2012	2014	2016
	Flash 1/2 pitch (nm)	***45***	***36***	***28***	***22***	***18***
	DRAM ½ Pitch (nm)	**59**	**45**	**36**	**28**	**23**
	MPU Printed Gate Length (nm)	**38**	**30**	**24**	**19**	**15**
	MPU Physical Gate Length (nm)	**29**	**24**	**20**	**17**	**14**
	Wafer Overlay Control (nm) - 20% DRAM	**11.8**	**9**	**7.2**	**5.6**	**4.6**
	Wafer Overlay Control Double Patterning (nm)	**8**	**6**	**5**	**4**	**3**
	Lithography Metrology					
Gate	Physical CD Control (nm) Allowed Litho Variance = 3/4 Total Variance	**3.0**	**2.5**	**1.3**	**1.8**	**1.5**
	Wafer CD metrology tool **uncertainty** (3s, nm) at P/T = 0.2	**0.60**	**0.50**	**0.26**	**0.35**	**0.29**
	Etched Gate Line Width Roughness (nm) <8% of CD	**2.3**	**1.9**	**1.6**	**1.4**	**1.1**
Dense Lines	Printed CD Control (nm) Allowed Litho Variance = 3/4 Total Variance	**4.7**	**3.7**	**2.9**	**2.3**	**1.9**
	Wafer CD metrology tool **uncertainty** (3s, nm) at P/T = 0.2	**1.1**	**0.8**	**0.7**	**0.5**	**0.4**
	Double Patterning Overlay Metrology					
	Double Exposure and Etch - Process Range (nm)	**8.3**	**6.4**	**5.1**	**4.0**	**3.3**
	Double Exposure and Etch - **Uncertainty** (nm)	**0.8**	**0.6**	**0.5**	**0.4**	**0.3**
	Spacer PEE process					
	First pass CD control (after etch) - Process Variation (nm)	3.9	3.0	2.4	1.9	1.6
	First pass CD control (after etch) - Uncertainty (nm)	0.4	0.3	0.2	0.2	0.2
	Front End Processes Metrology					
	High Performance Logic EOT equivalent oxide thickness (EOT), nm	**1.1**	**0.65**	**0.5**	**0.5**	**0.5**
	Logic Dielectric EOT Precision 3□□nm	**0.0044**	**0.0026**	**0.002**	**0.002**	**0.002**
	Interconnect Metrology					
	Barrier layer thick (nm)	**5.2**	**3.3**	**2.4**	**1.7**	**1.3**
	Void Size for 1% Voiding in Cu Lines	**5.9**	**4.5**	**3.6**	**2.8**	**2.3**
	Detection of Killer Pores at (nm) size	**5.9**	**4.5**	**3.6**	**2.8**	**2.3**

Replace Precision with Measurement Uncertainty



Lithography Metrology for Advanced Patterning

Double Exposure

Metrology Need:

Latent Image CD

CD-AFM after both exposures but no Solution for CD between exposures

Double Patterning

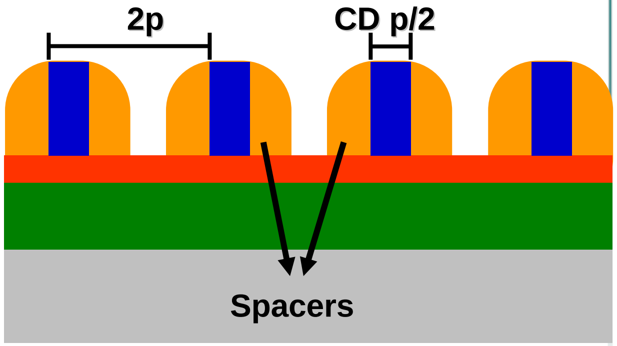
Metrology Need:

Overlay with

Precision of 70%

Of Single Layer

Spacer Patterning



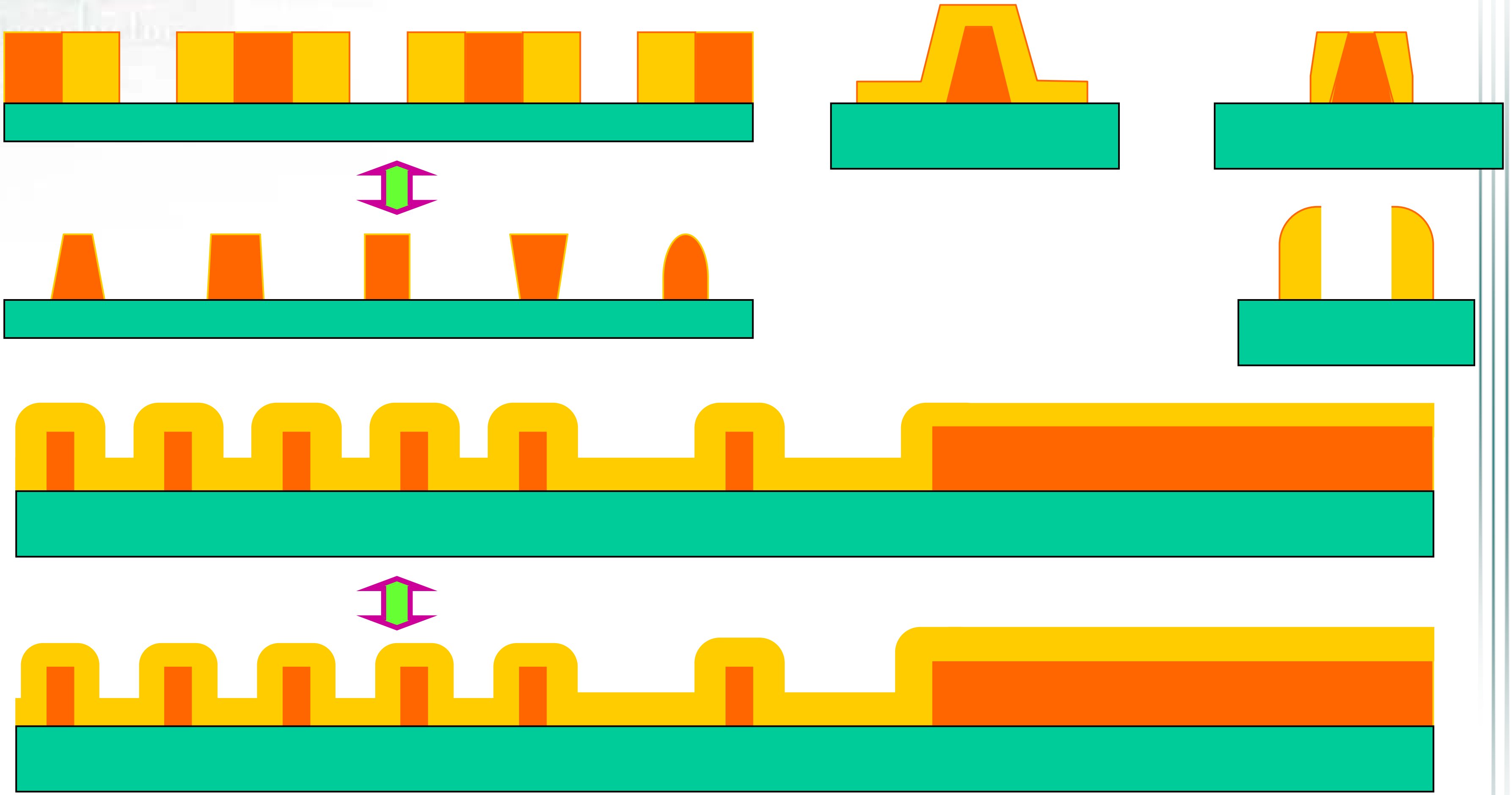
Metrology Need:

Spacer Thickness on Sidewall

Spacer Profile

22 nm Dense lines

Impact of Process on Metrology : courtesy Litho TWG



Loading effects of etching and CVD depend on not only pattern environment but resist pattern shape. So the shape itself is important requirement of metrology.

Requirements of shape should cover not only top CD, bottom CD, height and SWA, but 2D(or 3D) structure.

Metrology Challenges for Advanced Litho Processes

Double Exposure	Double Patterning	Spacer Double Patterning
	32/22 nm 1/2 Pitch	
For alignment need to measure latent image in	Sidewall Angle (SWA) and Height Accuracy for odd and	Spacer sidewall Thickness Uniformity across entire
	Overlay at resolution (i.e. with targets at device size) : what is	SWA of odd and even lines
		shape
Mask im M		uniformity er
	Mask CD Uniformity Metrology	ormity Metrology

2 Population CD, SWA, height and pitch

Potential Solution -> scatterometry

Q: is there enough sensitivity for odd-even line scenario

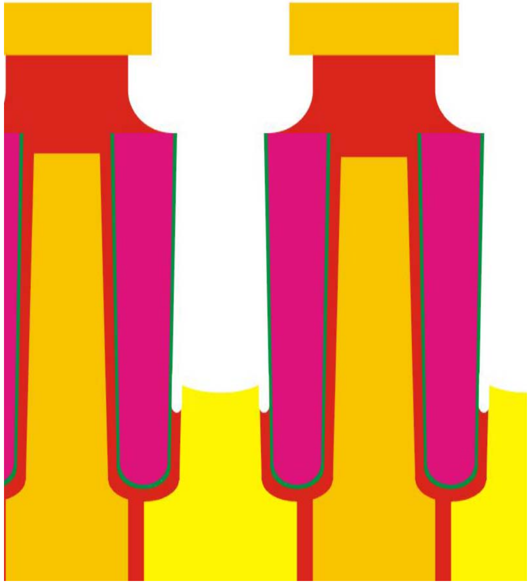
Metrology for Latent Image at 1st exposure

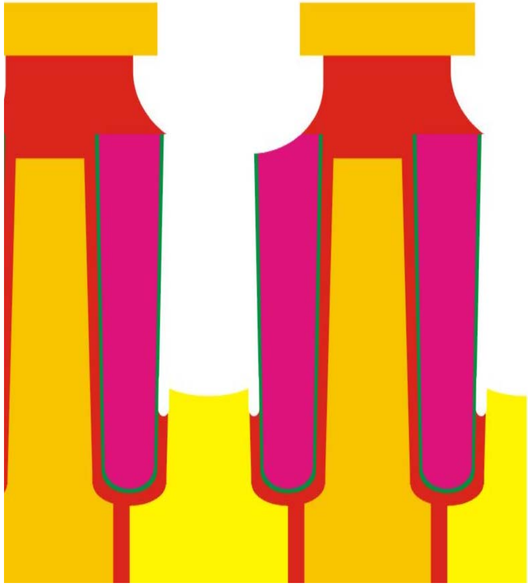
might be avoided using

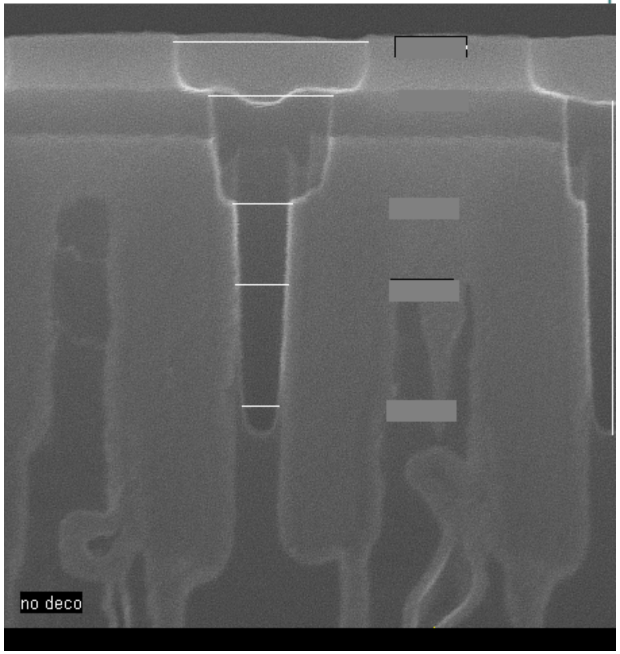
AEC/APC approaches & CD/Overlay

after double exposure

3D Metrology Requirements


perfect overlay


overlay shift
creates asymmetry



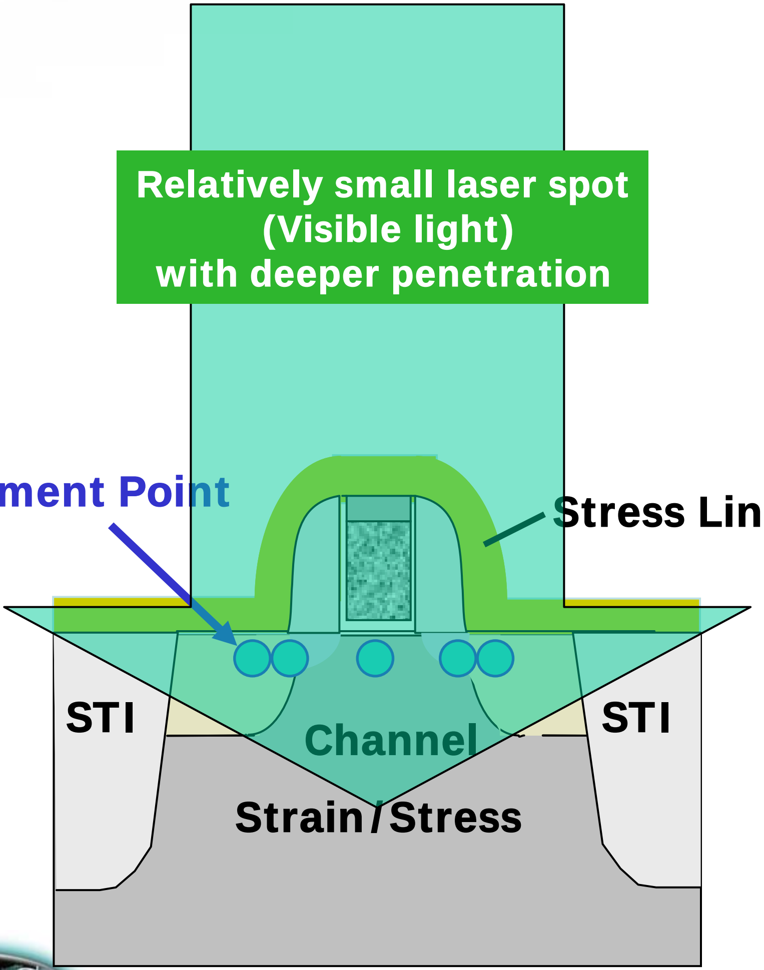
cross section example

New FEP Metrology Requirements for Ultimately Scaled and Functionally Enhanced CMOS:

- Non-Destructive local strain/stress measurement
- Dopant activation Metrology for USJ
- Interface Metrology
- New channel material or structures challenges
  - SiGe & III-V
  - Trigate FinFET, Nanowire
  - Carbon nanotubes & Graphene
- Surface/film analysis on vertical surfaces
  - In-situ monitoring of multi-component oxides
- In-Line work function measurements – band gap engineering for flash and gates

• Local Strain/Stress Measurement

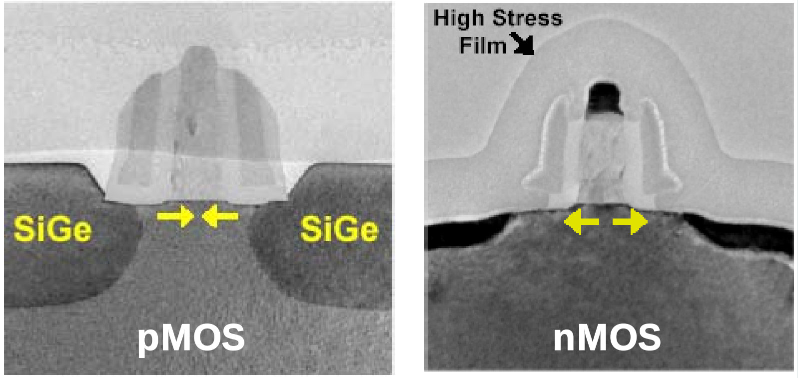
Proposal of new item on FEP table



Relatively small laser spot (Visible light) with deeper penetration

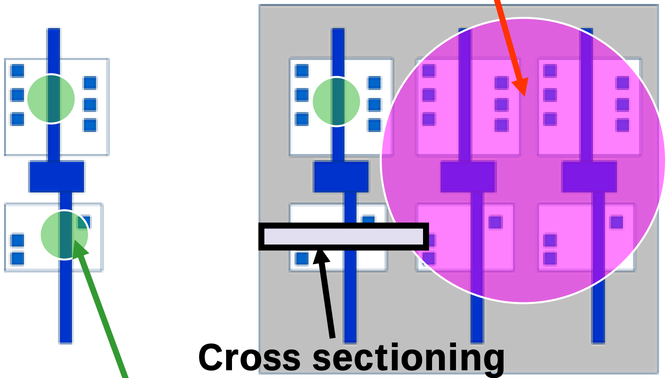
Measurement Point

Stress Liner



Ghani, et al (Intel)

Wide laser spot for extracting average stress



Cross sectioning

Modified from Fichtner's figure

Small laser spot for extracting single Tr. stress

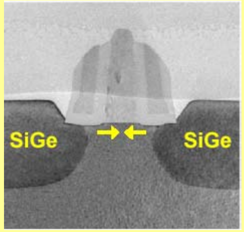
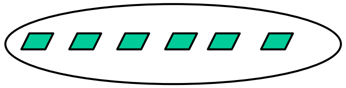
New table for Local Strain/Stress Measurement

need inputs from FEP and PIDS

Table 120a Front End Processes Metrology Technology Requirements—Near-term Years

Year of Production	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*	*2014*	*2015*
DRAM ½ Pitch (nm) (contacted)	*65*	*57*	*50*	*45*	*40*	*36*	*32*	*28*	*25*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	*68*	*59*	*52*	*45*	*40*	*36*	*32*	*28*	*25*
MPU Physical Gate Length (nm)	*25*	*22*	*20*	*18*	*16*	*14*	*13*	*11*	*10*
Mobility Enhancement Factor For Idsat (Table 40ab)									
- Extended Planar Bulk	1.08	1.09	1.1	1.1	1.12	1.11			
- UTB FDS		~~1.06~~	~~1.06~~	1.06	1.06	1.05	1.05	1.04	1.04
- DG					1.05	1.04	1.05	1.04	1.04
Stress measurement with 50MPa resolution									
Spatial resolution (Offline, destructive, single Tr.)	1/5 of Gate Length								
	5	4.4	4	3.6	3.2	2.8	2.6	2.2	2
Spatial resolution (Inline, non-destructive, Test pattern for average stress measurement)	Same size with HP								
	65	57	50	45	40	36	32	28	25
	Using test pad of 100um X 100um								
	100	100	100	100	100	100	100	100	100
Throughput (wafers/hour) (Inline, non-destructive, Test pattern)	25 sites per wafer								
	2	2	2	2	2	2	2	2	2

Local Strain/Stress Measurement Method (Tentative)

Area of Interest	Measurement Method	Sensitivity		Measurement Area	Sample Thickness	
		Stress	Strain			
Transistor Level 	- CBED	20 MPa	0.02%	10-20nm	<100nm	Destructive
	- NBD	100 MPa	0.1%	~10nm	<300nm	Destructive
	- TERS	50 MPa	0.05%	<50nm		Destructive Non-Destructive
Micro-Area Level 	- Confocal Raman	20 MPa	0.05%	~150nm		Non-Destructive
	- XRD	10 MPa	0.01%	100um		
	- Photoreflectance Spectroscopy					
Die 	- Die level flatness - Laser Interferometry - Coherent Gradient Sensing					Non-Destructive
Wafer 	- Laser Interferometry - Coherent Gradient Sensing	10 MPa	0.001%	wafer		Non-Destructive

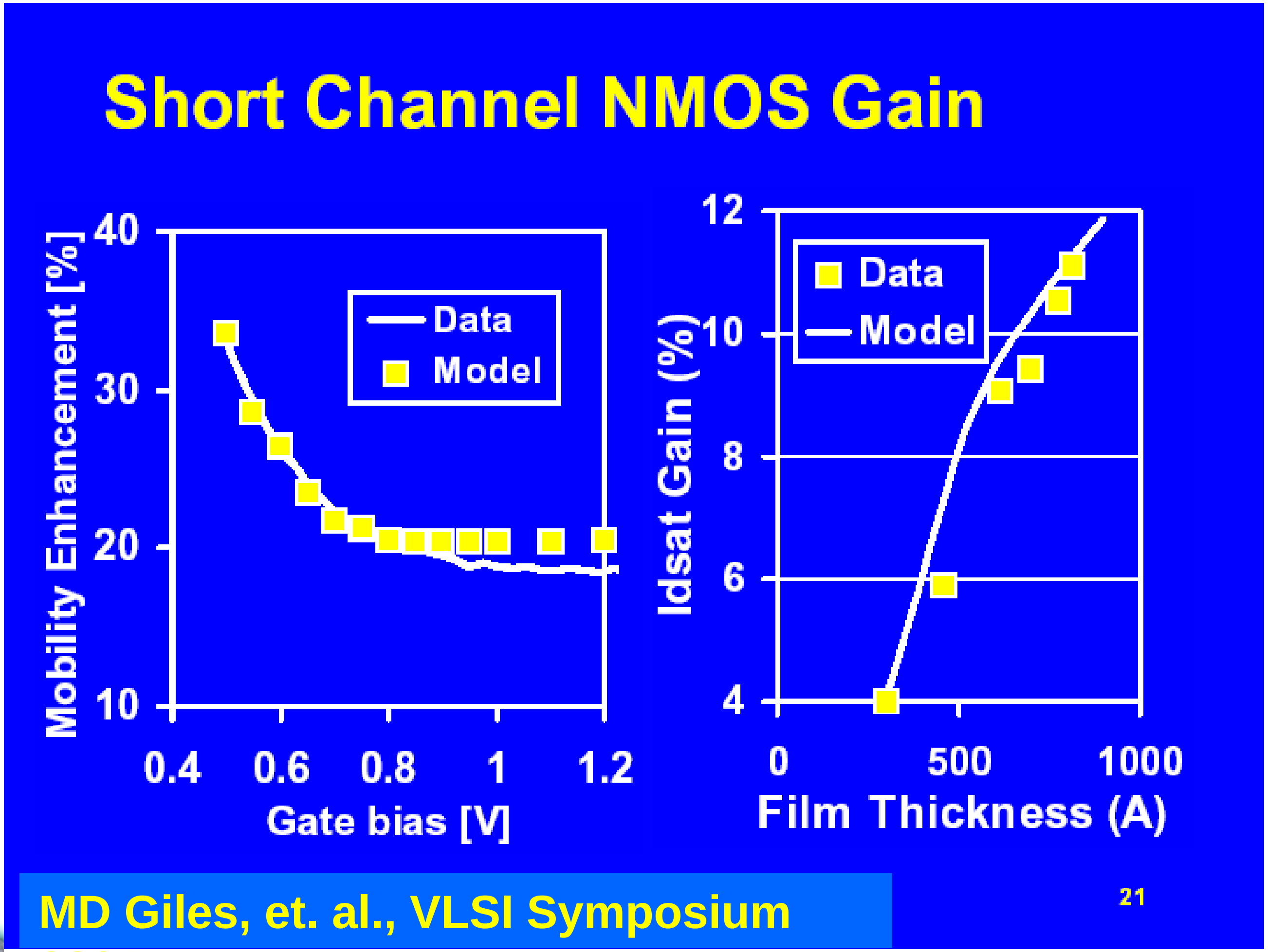
<u>Handling Area of ITRS</u>

* Stress – Strain relation : need to be clarified

TERS (Tip Enhanced Raman Scattering)
CBED (Convergent Beam Electron Diffraction)
NBD (Nano Beam Electron Diffraction)
XRD (X-ray Diffraction)

Trend : Use Modeling to connect what you can measure with what you need to know

Example: Metrology of Strained Channel Devices



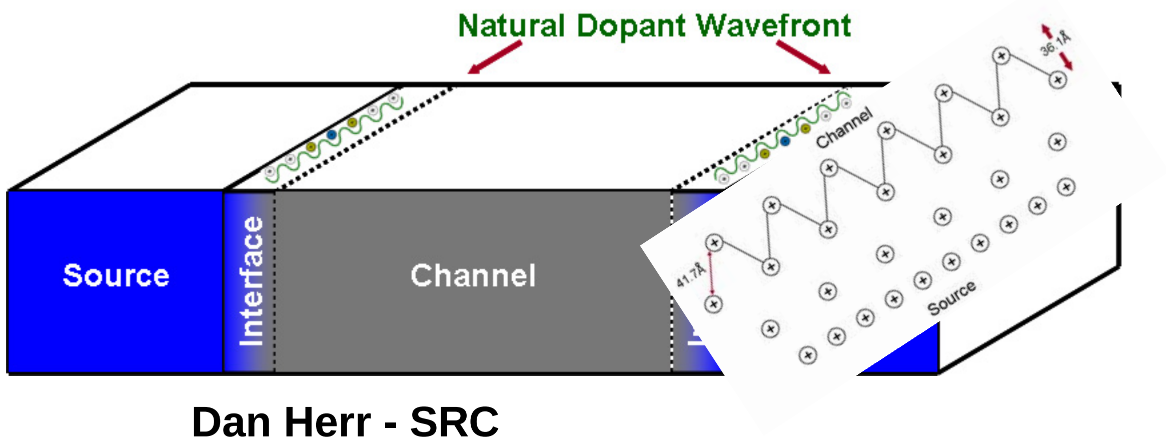
MD Giles, et. al., VLSI Symposium 2004

Dopant profile measurement (Essentially destructive)

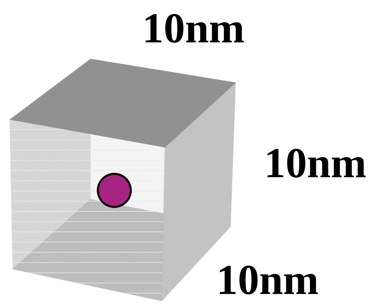
- 2008 Update

Table 120a Front End Processes Metrology Technology Requirements—Near-term Years UPDATED

	Year of Production	2005	2006	2007	2008	2009	2010	2011	2012	2013
	DRAM ½ Pitch (nm) (contacted)	80	70	65	57	50	45	40	36	32
	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	90	78	68	59	52	45	40	36	32
	MPU Physical Gate Length (nm)	32	28	25	22	20	18	16	14	13
WAS	Lateral/depth spatial resolution for 2D/3D dopant profile (nm)	3.5	3.1	2.8	TBD	TBD	TBD	TBD	TBD	TBD
IS	Lateral/depth spatial resolution for 2D/3D dopant profile (nm)	3.5	3.1	2.8	2.5	2.2	2	1.8	1.5	TBD
	At-line dopant concentration precision (across concentration range) [D]	4%	4%	4%	4%	4%	2%	2%	2%	2%



Dan Herr - SRC

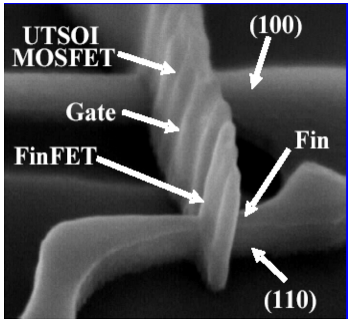


1×10^{18}atoms/cm^3

Total throughput of analysis is one of remaining issues

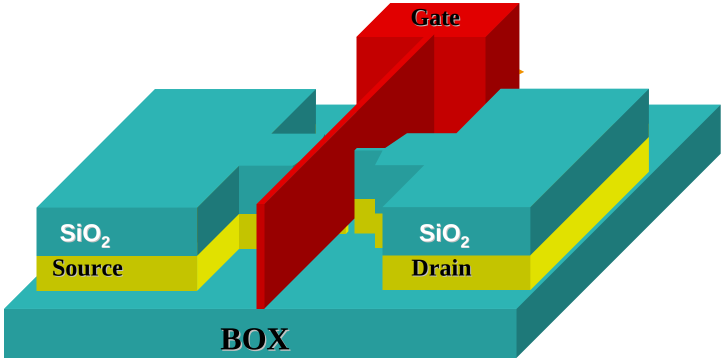
Do we need to put in a throughput requirement?

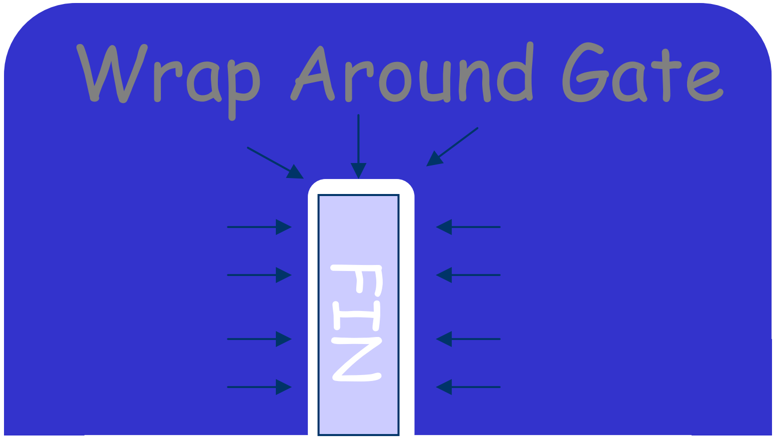
Wrap Around Gate Metrology



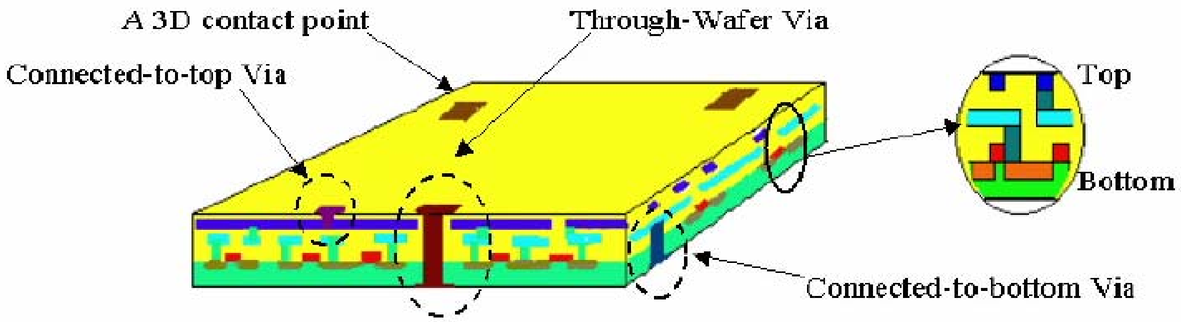
FINFET

Side Wall and Top Dielectric Thickness and Composition



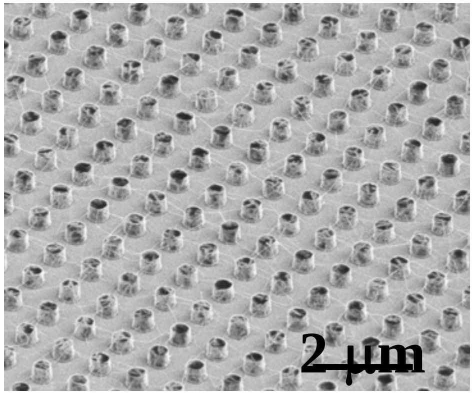


Future Interconnect (ITRS 2008)



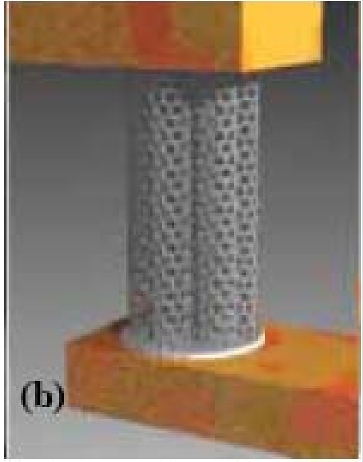
- 3D Interconnect ?

- Carbon Nanotubes ?

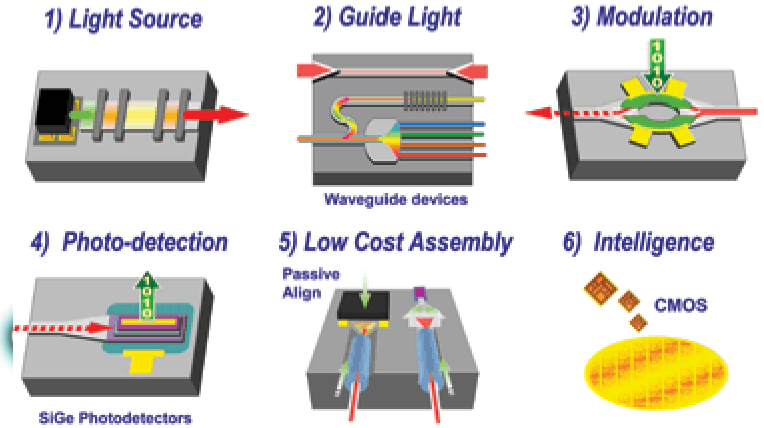


MARCO Center

Kreupl, Infineon



Intel



- Optical Interconnect ?

2008 Interconnect Metrology

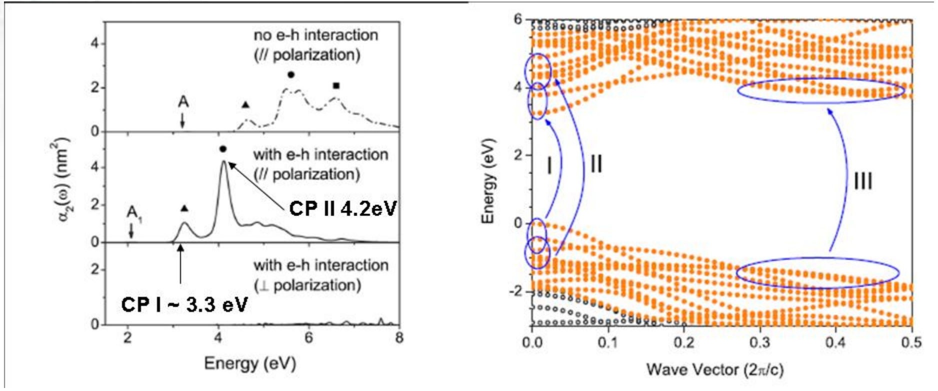
- Existing Challenges
  - Measurements of Sidewall barrier thickness and sidewall damage (compositional changes in low k) after etch remains a Major Gap - It will soon also be a Gap for FEP Metrology
  - New - Porous low k is projected for 32 nm ½ Pitch
  - Detection of Voids after electroplating
- Air Gap sacrificial layer does not require unique metrology
- Metrology is needed for 3D Integration
  - TSV Depth and Profile through multiple layers
  - Alignment of chips for stacking – wafer level integration
  - Bond strength
  - Defects in bonding
  - Damage to metal layers
  - Defects in vias between wafers
  - Through Si via is high aspect ratio CD issue
  - Wafer thickness and TTV after thinning
  - Defects after thinning including wafer edge

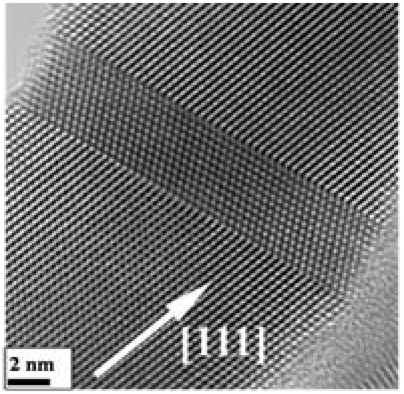
ERD/Metrology Collaboration Discussion

- Small geometrical metrologies, obtaining a reasonable signal/noise ratio – study, determine, and manage noise sources. Extract the signal from noise.
- Issue of contamination of nano-scaled devices
- Time resolved magnetic measurements.
- Ability to perform real time measurements, e.g. phase transitions.
- Wide band characterizations of rf devices – above 100 GHz.
- Questions from Metrology
  - PCM – Near mfg?
  - MRAM – Near mfg? – In production. Spin torque RAM
  - Contamination -

Metrology Summary

1.2 nm diameter Si NW



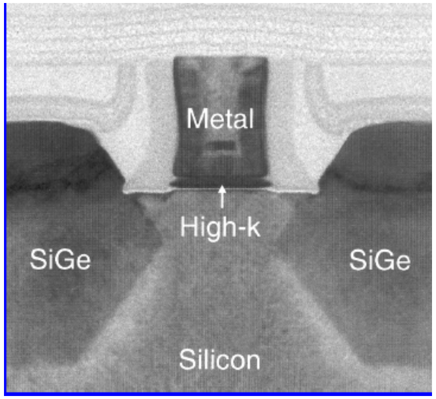


- **FEP-Interconnect-Litho**
  - 3D Metrology – Confirm Geometry Requirements e.g. film thickness on sidewall
  - Reference Methods for 3D
  - Stress – e.g. buried channels
- **ERD-ERM**
  - Properties of low Dimensional Materials
  - Microscopy and feature size/function
  - Time resolved magnetic measurements
  - Ability to perform real time measurements, e.g. phase transitions

High K changes

Litho scaling

& Metrology



Conclusions

- CD Measurement improvements show a path to the 32/22 nm ½ Pitch
- Propose definition for LWR and including LER
- Transistor channel engineering requires Stress and Mobility Measurement
- Interconnect requires Sidewall Measurements for barrier/seed and low κ trench
- ERM and ERD require both improved imaging (such as aberration corrected TEM) and image simulation