

# **ITRS Assembly & Packaging Report More than Moore Initiative**

**Assembly and Packaging  
July 16, 2008**



# 2008 Assembly & Packaging Summer Conference Participants

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Clinton Chao

Richard Otte



# 2008 Assembly & Packaging Summer Conference Participants



# Assembly & Packaging 2008 Work Plan

Europe Spring Conference	April 3-4
AP ITWG, ECTC work session	May 28
AP ITWG Pre-meeting session	July 13
US Summer Conference	July 14-16
AP ITWG, Shanghai work session	July 28
AP ITWG, Japan work session	August 1
AP ITWG, Taiwan work session	August 4
Korea Winter Conference	December 7-9
Joint Working Sessions with ERM	September



# 2008 Highlights

## Assembly and Packaging

Major Changes have occurred:

- Wafer level Packaging
- System in Package (White Paper)
- 3D Integration
- Materials Changes
- Embedded Components
- Cooperation across the world



# Assembly and Packaging Chapter Changes for 2008

Changes include:

- Major changes to 12 tables
- 2 new tables added
- Text changes to explain the significance of table changes
- Further review with TWG in Taiwan & Japan
- Expanded participation by adding China




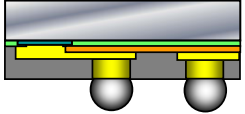


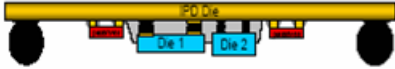

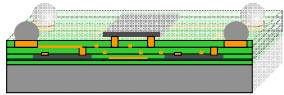
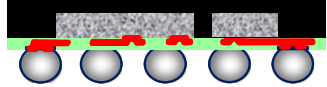
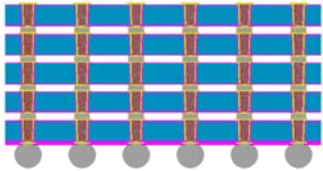
# Wafer Level Packaging

The answer to the historical lack of scaling in packaging to match the scaling in IC production

WLP offers portable consumer products :

- inherent lower cost
- improved electrical performance
- lower power requirements
- Smaller size

Several architectural variations are in use today

	
<p>Wafer level CSP in the simplest structure</p>	<p>Wafer level CSP with copper post and resin mold</p>
	
<p>Opto wafer level CSP with tapered TSV interconnection</p>	<p>Opto wafer level CSP with beam lead metallurgy</p>
	
<p>IPD embedded silicon substrate</p>	<p>Build-up substrate through wafer level fabrication</p>
	
<p>Thin Chip Integration (Embedded device in polymer dielectric)</p>	<p>embedded Wafer Level Ball Grid Array</p>
	
<p>Stacked devices with Through Silicon Via's (TSV)</p>	



# System in Package

The key to MtM functional diversification is System in Package.  
This technology enables:

- Embedded active and passive components
- MEMS integration
- Wireless integration
- Sensor integration
- Analog circuit integration

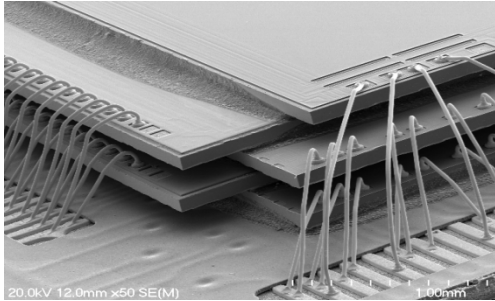
---with traditional logic and memory  
integrated circuits

ITRS Assembly & Package System In Package White Paper

[http://www.itrs.net/Links/2007ITRS/LinkedFiles/AP/AP\\_Paper.pdf](http://www.itrs.net/Links/2007ITRS/LinkedFiles/AP/AP_Paper.pdf)

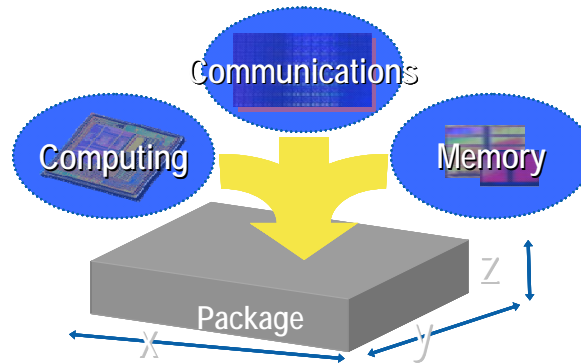


# 3D Packaging increases Performance Density and enables system level integration

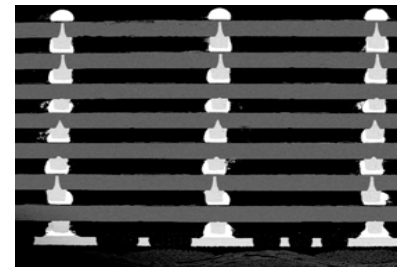


Wire bonded stacked die

New System in Package (SIP) solutions enables rapid integration of different functions



Small form factor for ultramobile PCs, hand-helds, phones & other consumer electronics



Thru-Si via Stacking



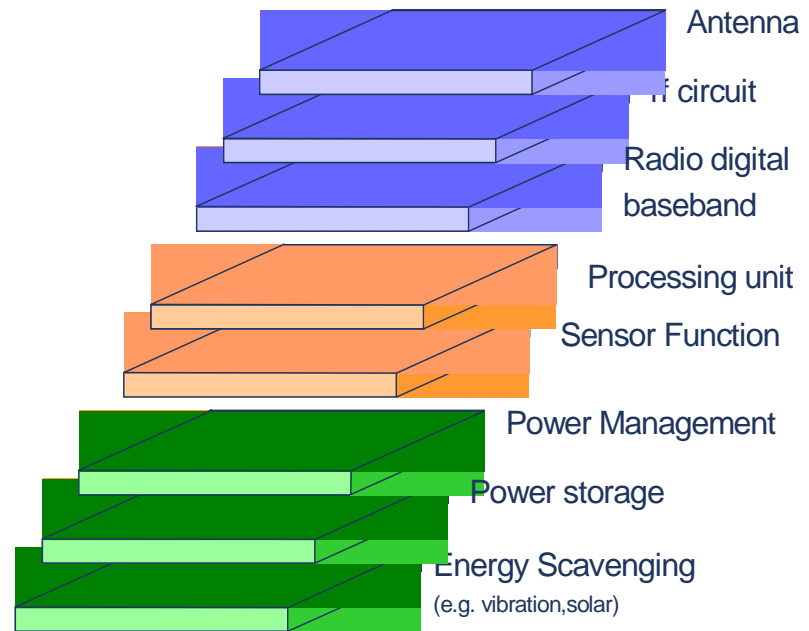
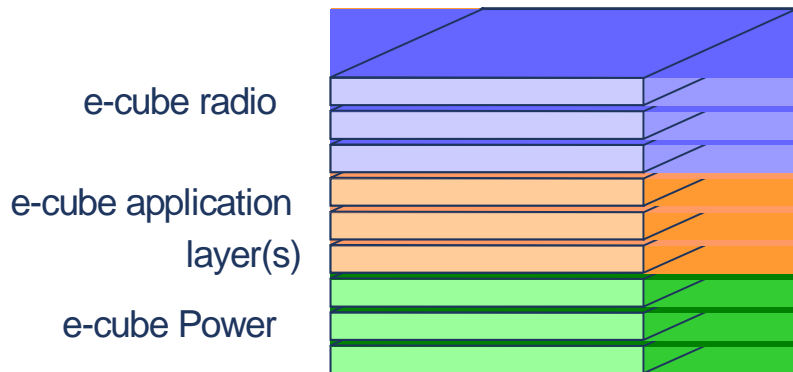
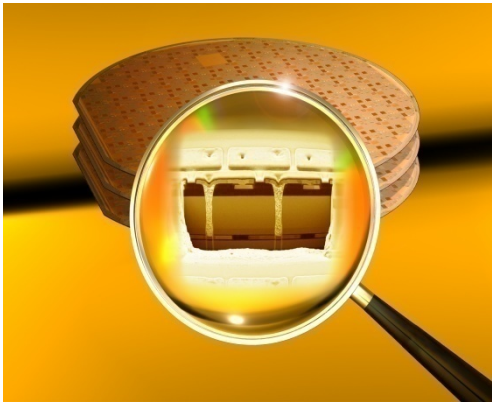
# 3D Integration

**Table AP11: System in Package Requirements**

<i>Year of Production</i>	<i>2008</i>	<i>2009</i>	<i>2010</i>	<i>2011</i>	<i>2012</i>	<i>2013</i>	<i>2014</i>	<i>2015</i>	<i>2016</i>
Number of terminals—low cost handheld	800	800	900	900	1000	1000	1000	1000	1000
Number of terminals—high performance (digital)	3190	3350	3509	3684	3860	4053	4246	4458	4670
Number of terminals—maximum RF	200	200	200	200	200	200	200	200	200
Low cost handheld / die / stack	8	9	10	11	12	13	14	14	15
High performance / die / stack	3	3	4	4	4	5	5	5	6
Low cost handheld / die / SiP	8	9	11	12	13	14	14	14	15
High performance / die / SiP	6	6	7	7	7	8	8	8	9
Minimum TSV pitch	8	6	5	4	3.8	3.6	3.4	3.3	3.1
TSV maximum aspect ratio	10	10	10	10	10	10	10	10	10
TSV exit diameter(um)	4	3	2.5	2	1.9	1.8	1.7	1.6	1.5
TSV layer thickness for minimum pitch	20	15	15	10	10	10	10	8	8
Minimum component size (micron)	400X200	400X200	400x200	400x200	200X100	200x100	200x100	200x100	200x100
Maximum reflow temperature (°C)	260	260	260	260	260	260	260	260	260



# 3D System Integration & Packaging



**Stacked functional Layers with TSV and /or flexible polymer Inetrposer**



Source: Fraunhofer IZM

# Materials Changes

After 30 years or more with only limited changes in materials used we are seeing unprecedented changes.

- In this decade 100% of packaging materials will change
- In the next decade most materials will change again



# Embedded Components

SiP includes embedded components for size reduction and performance improvement:

- Embedded Active and Passive in Substrates
- Many Variations on Same Theme
- Consumer Drivers for
  - Space
  - 3D shorten path
  - Reduced passive components



# More than Moore

## Cross TWG Collaborations

Integration of the work product of all TWGs delivers “More than Moore” Roadmap and support continuation of growth driven by “More Moore”.

- Assembly and Packaging
- Design
- Test
- ERM
- Wireless
- Interconnect



# World Wide Collaboration in Materials

Company	Address	Website
<b>EPACK Lab/CAMP</b> (Electronic Packaging Laboratory/Center for Advanced Microsystems Packaging)	Hong Kong University of Science & Technology	<a href="http://www.ust.hk/epack-lab">www.ust.hk/epack-lab</a>
<b>Fraunhofer IZM</b> (Fraunhofer Institute for Reliability and Microintegration)	Berlin, Germany (Headquarters)	<a href="http://www.izm.fhg.de">www.izm.fhg.de</a> <a href="http://www.iwmh.fraunhofer.de">www.iwmh.fraunhofer.de</a>
<b>HDPUG</b> (High Density Packaging Users Group)	Arizona	<a href="http://www.hdpug.org">www.hdpug.org</a>
<b>IEEC</b>	Binghamton University, NY	<a href="http://www.ieec.binghamton.edu/ieec/">www.ieec.binghamton.edu/ieec/</a>
<b>IFC</b> (Interconnect Focus Center)	Atlanta, Georgia	<a href="http://www.ifc.gatech.edu">www.ifc.gatech.edu</a>
<b>IME</b>	Singapore	<a href="http://www.ime.a-star.edu.sg">www.ime.a-star.edu.sg</a>
<b>IMEC</b> (Interuniversity Microelectronics Centre)	Leuven, Belgium	<a href="http://www.imec.be">www.imec.be</a>
<b>ITRI</b> (Industrial Technology Research Institute)	Hsin Chu, Taiwan	<a href="http://www.itri.org.tw">www.itri.org.tw</a>
<b>JIEP</b> (Japan Institute of Electronics Packaging)	Japan	<a href="http://www.e-jisso.jp">www.e-jisso.jp</a>
<b>KAIST</b> (Korea Advanced Institute of Science and Technology)	South Korea	<a href="http://www.kaist.edu">www.kaist.edu</a>
<b>LETI</b> (Laboratoire d'électronique et de technologie de l'information)	Grenoble, France	<a href="http://www-leti.cea.fr">www-leti.cea.fr</a>
<b>PRC</b>	Atlanta, GA	<a href="http://www.prc.gatech.edu">www.prc.gatech.edu</a>

See 2007 ITRS

System in Package

White Paper

for more Detail