ITRS Public Conference

Emerging Research Devices

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Emerging Research Devices Working Group

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Highlights of Changes

- Scope of ERD Chapter
  - Invent the new "switch" – Emerging information processing* devices to eventually replace CMOS Boolean logic
  - Supplement Si CMOS – Use the physics of emerging research devices to realize complex typically nonlinear functions in an accelerator-like fashion
    - ✓ Perform certain functions more efficiently than digital CMOS
    - ✓ Eventually extend CMOS and nanoelectronics to address new applications
- Spin off a new chapter on Emerging Research Materials
- Expand the Emerging Architecture Section
- Expand scope of the Emerging Logic Section – supplement CMOS
  - Example: Image Processing using emerging research devices integrated on a CMOS Platform.
- Update the Emerging Memory Section

*ERD Chapter includes the following elements of Information Processing: Data processing, storage and communication.

Evolution of Extended CMOS

Elements

Existing technologies

More Than Moore Elements

More Than Moore

More Moore

Top-down

Bottom-up

Beyond CMOS

Extended CMOS

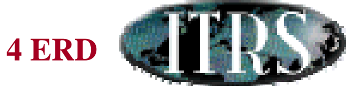
Beyond CMOS Elements

New technologies

Beyond CMOS

ERD-WG in Japan

year



2005 ITRS ERD Chapter

Emerging Research Memory Devices

	Nano-floating Gate Memory	Engineered tunnel barrier Memory	Ferroelectric FET Memory	Insulator Resistance Change Memory	Polymer Memory	Molecular Memories
Storage Mechanism	Charge on floating gate	Charge on floating gate	Remanent polarization on a ferroelectric gate dielectric	Multiple mechanisms	Not known	Not known
Cell Elements	1T	1T	1T	…R or 1R	1T1R or 1R	1T1R or 1R
Device Types	1Nanocrystal 2 Direct tunneling	Graded insulator	FET with FE gate insulator	1 M-I-M 2 Solid Electrolyte 3 FE tunneling 4 FE Schottky diode 5 FE-I-FE	M-I-M (nc)-I-M	Bi-stable switch

OUT

Expand

Capacitance-based

Resistance-based

2007 ITRS ERD Chapter

Transition Table for Emerging Memory Devices

	IN/OUT	*Reason for IN/OUT*	*Comment*
Nanofloating gate memory	OUT	Natural evolution of FG FLASH. No outstanding research issues -became a prototypical technology	ERD recommends to include NFLG memory in PIDS (Not included in 2007PIDS chapter)
Insulator Resistance Change Memory	OUT	Replaced by three new memory categories (see below)	This memory category included several different memory types based on different mechanisms of operation
Fuse/Antifuse Memory	IN	Replacement for the Insulator resistance change memory	
Ionic Memory	IN	Replacement for the Insulator resistance change memory	
Electronic Effects Memory	IN	Replacement for the Insulator resistance change memory	
Nano-mechanical memory	IN	New device concept, promising characteristics, several recent publications	

2007 ITRS ERD Chapter

Capacitance-based memory technologies

	Engineered tunnel barrier Memory	Ferroelectric FET Memory
Storage Mechanism	Charge on floating gate	Remnant polarization on a ferroelectric gate dielectric
Cell Elements	1T	1T
Device Types	Graded insulator	FET with FE gate insulator

2007 ITRS ERD Chapter

Resistance-based memory technologies

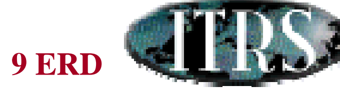
	Nanomechanical memory	Fuse/Anti fuse Memory	Ionic Memory	Electronic effects Memory	Polymer Memory	Molecular Memories
Storage Mechanism	Electrostatically-controlled bi-stable mechanical switch	Multiple mechanis ms	Ion transport in solids	Multiple mechanisms	Not known	Not known
Cell Elements	1T1R or 1D1R	1T1R or 1D1R	1T1R or 1D1R	1T1R or 1D1R	1T1R or 1D1R	1T1R or 1D1R
Device Types	CNT bridge CNT cantilever Si cantilever Nanoparticle	M -I-M e.g. Pt/NiO/Pt	1) Solid Electrolyte 2) RedOx reaction	1) Charge trapping 2) Mott transition 3) FE Barrier effects	M-I-M (nc)-I-M	Bi-stable switch

> 20	>16 - 18
>18 - 20	≤ 16

Critical Evaluation Memory

For each Technology Entry (e.g. 1D Structures), sum horizontally over the 8 Criteria
Max Sum = 24
Min Sum = 8

	Scalability	Performance	Energy Efficiency	Off/On ratio	Operational Reliability	Operate Temperature	CMOS Technological Compatibility	CMOS Architectural Compatibility
Engineered Tunnel Barrier Memory	2.4	2.3	2.2	2.0	2.2	2.7	2.7	2.5
Fuse/Anti-fuse Memory	2.6	1.9	2.0	2.2	1.8	2.8	2.7	2.5
Nano Mechanical Memory	1.7	1.9	2.4	2.5	1.9	2.9	2.2	2.2
Electron Injection Memory	2.3	2.2	2.3	2.1	2.0	2.4	2.3	2.4



> 20	>16 - 18
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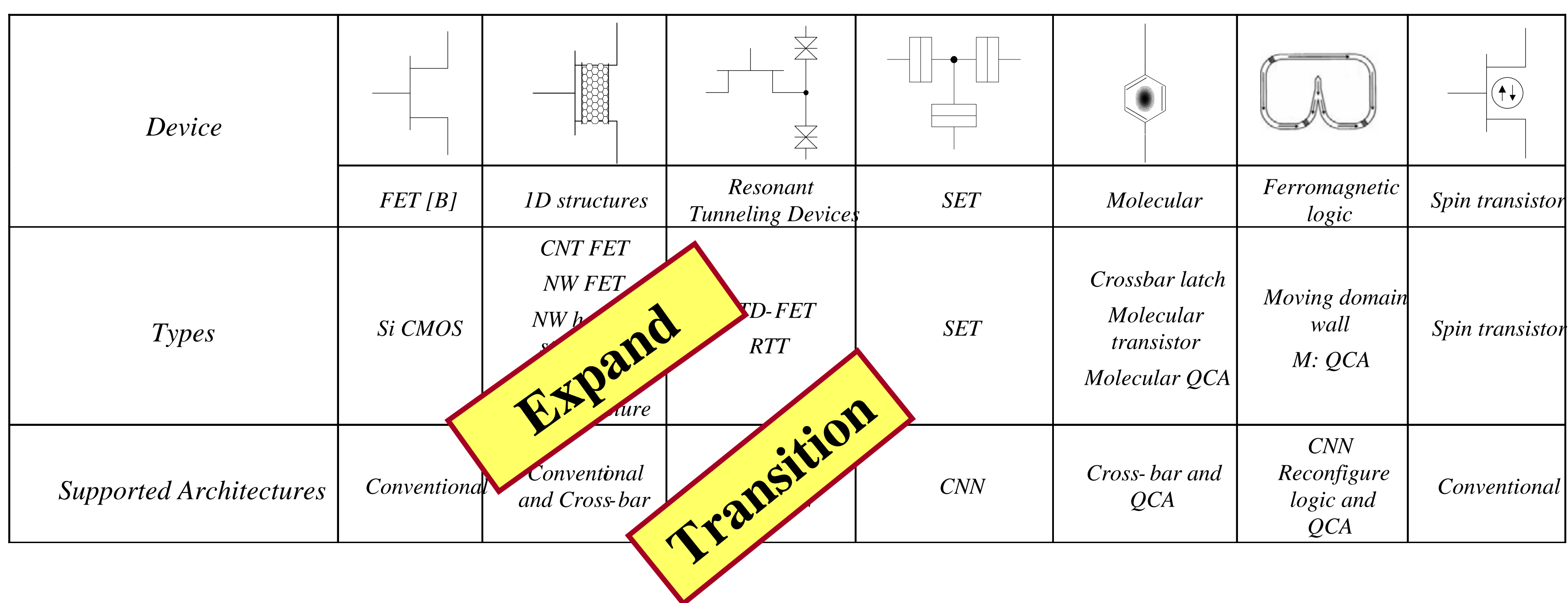
Critical Evaluation Memory

For each Technology Entry (e.g. 1D Structures), sum horizontally over the 8 Criteria
Max Sum = 24
Min Sum = 8

	Scalability	Performance	Energy Efficiency	Off/On ratio	Operational Reliability	Operate Temperature	CMOS Technological Compatibility	CMOS Architectural Compatibility
Ionic Memory	2.6	2.0	2.4	2.1	1.7	2.5	2.1	2.5
Ferroelectric FET Memory	1.8	2.0	1.9	2.1	1.7	2.6	2.3	2.3
Macromolecular Memory	2.1	1.8	2.1	1.8	1.4	2.2	1.9	2.3
Molecular Memory	2.4	1.7	2.4	1.4	1.3	2.2	1.8	1.9

2005 ITRS ERD

Emerging Research Logic Devices



Device	FET [B]	1D structures	Resonant Tunneling Devices	SET	Molecular	Ferromagnetic logic	Spin transistor
Types	Si CMOS	CNT FET NW FET NW [illegible] [illegible]ure	[illegible]D-FET RTT	SET	Crossbar latch Molecular transistor Molecular QCA	Moving domain wall M: QCA	Spin transistor
Supported Architectures	Conventional	Conventional and Cross-bar	[illegible]	CNN	Cross- bar and QCA	CNN Reconfigure logic and QCA	Conventional

Transition Table for Emerging Logic Devices

	IN/OUT	Reason for IN/OUT	Comment
Rapid Single Flux Quanta	OUT	RSFQ devices, systems and circuits have been developed, prototyped, and fabricated. They could become an important technology if the correct market driver emerges	Design and fabrication lines for RSFQ systems exist. Cryogenic operation, cost and material integration issues limit application space
CMOS extension-	IN	Low bandgap, compound III-V materials can potentially improve transistor performance	Research on compound III –V materials on SI substrates has increased significantly over the last 2 years
Impact Ionization MOS	IN (pending)	Simulation results showing very low sub threshold slopes indicate potential for low power operation	**May be included in future editions**
Lateral interband tunneling transistor	IN (pending)	Potential to utilize gate modulated interband tunneling to reduce subthreshold slope	**May be included in future editions**
Floating gate MOS devices	IN (pending)	Devices with nanocrystals embedded in gate allow circuits with tuneable thresholds. Potential for low power circuits	**May be included in future editions**
Nano Electro Mechanical Systems	IN (pending)	Potential for ultra low leakage device based on nano relay operation	**May be included in future editions**

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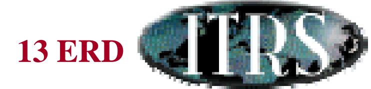
CMOS Scaling & Replacement Devices (1st)

Device	FET	CMOS Extension Low dimensional structures	CMOS Extension III-V channel replacement	SET	Molecular	Ferromagnetic logic	Spin transistor
Types	Si CMOS	•CNT FET •NW FET •NW hetero-structures •Nanoribbon transistors	•III-V compound semiconductor channel replacement	SET	•2-terminal •3-terminal FET •3-terminal bipolar transistor •NEMS •Molecular QCA	•Moving domain wall •Hybrid Hall effect •Magnetic Resistive Element •M: QCA	•Spin Gain transistor •HMF Spin MOSFET •Spin Torque Transistor
Supported Architectures	Conventional	Conventional	Conventional	Threshold logic	Memory-based QCA	Lithographically defined	conventional



Critical Evaluation Logic

> 20	>16 - 18
>18 - 20	≤ 16

For each Technology Entry (e.g. 1D Structures), sum horizontally over the 8 Criteria
Max Sum = 24
Min Sum = 8

	Scalability	Performance	Energy Efficiency	Gain	Operational Reliability	Operate Temperature	CMOS Technological Compatibility	CMOS Architectural Compatibility
1D Structure	2.4	2.2	2.5	2.3	2.0	2.5	1.8	2.3
Channel Replacement Materials	2.0	2.9	2.3	2.4	1.9	2.3	1.8	2.5
Single Electron Transistors	2.4	1.1	2.3	1.2	1.3	1.4	1.6	1.5
Molecular Devices	2.5	1.5	2.2	1.5	1.3	1.8	1.6	1.7

(Scale in each row: 3, 2, 1)

> 20	>16 - 18
>18 - 20	≤ 16

Critical Evaluation Logic

For each Technology Entry (e.g. 1D Structures), sum horizontally over the 8 Criteria
Max Sum = 24
Min Sum = 8

	Scalability	Performance	Energy Efficiency	Gain	Operational Reliability	Operate Temperature	CMOS Technological Compatibility	CMOS Architectural Compatibility
Ferromagnetic Devices	1.2	1.3	1.7	1.5	2.0	2.1	1.2	1.3
3 2 1								
Spin Transistor	1.7	1.4	2.3	1.7	1.4	1.3	1.3	1.3
3 2 1								

Logic Device Conclusions

- Continued analysis of alternative technology entries likely will continue to yield the same result:
  - **Nothing beats MOSFETs overall for performing Boolean logic operations at comparable risk levels**
- Certain functions, e.g. image recognition (associative processing), may be more efficiently done in networks of non-linear devices rather than Boolean logic gates

Supplementing CMOS

Basis of Existing Assessments of Logic Devices

A possible ultimate evolution of **on-chip** architectures is Asynchronous ***Heterogeneous*** Multi-Core with Hierarchical Processors Organization

General Purpose Processor

SOC-PE Architecture

Main Proc.

Main Memory

Peripherals

PE PE PE PE PE PE PE PE PE PE PE PE PE PE

Function A Function B Function C Function D Function E

Multi-Core/Accelerator Engine Platform (SOC-MC/AE Architecture)

Multi-Cores

L2 Cache L2 Cache L2 Cache L2 Cache

Multi-Core Multi-Core Multi-Core Multi-Core

On-Demand Acceleration

Accelerator Engine

Accelerator Engine

Accelerator Engine

Accelerator Engine

Non-Blocking Switch Fabric

System Functions

Memory Control

L3 Cache

Connectivity

Hi Speed Hi Speed Hi Speed

Courtesy Fawzi Behmann - Freescale

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CMOS Supplement Devices (2nd)

Device	Resonant tunneling diodes	Muti ferroic tunnel junctions	Single Electron Transistors	Molecular devices	Ferro-magnetic devices	Frequency coherent spin devices
State variable	Charge	Dielectric and magnetic domain polarization	Charge	Molecular Conformation	Ferromagnetic polarization	Precession frequency
Response function	Negative differential resistance	Four resistive states	Coulomb blockade	Hysteritic	Non-linear	Nonlinear

Emerging Research Architectures

Architecture	Implementation	Computational Elements	Network	Application	Research Activity
Homogeneous Many-Core	Symmetric cores	CMOS	Irregular/ Fixed	Synthesis/GPP	
Heterogeneous	Asymmetric cores	CMOS	Irregular/ Fixed	Synthesis/GPP	
	CMOL	CMOS+Molecular Switches	Irregular/ Fixed	Synthesis/GPP	
	Molecular Cross-bar	Molecular Switches	Regular/ Flexible	Synthesis/GPP	
	Check-point	CMOS+ Ferromagnetic logic	Irregular/ Fixed	Synthesis/GPP	
Morphic	CNN	CMOS+Sensors	Regular/ Flexible	Recognition/Vision	
	AMP	FG-FET, SET	Irregular/ Fixed	Recognition/Vision	
	Bio-inspired	MFDT, Spin-gain transistor	Mixed	Recognition Mining Synthesis	

CMOL – 'Molecule on CMOS' architecture
CNN – Cellular Nonlinear Network
AMP – Associative Memory Processor

GPP – General Purpose Processor
FG-MOS – Floating Gate MOS devices
SET – single electron transistor

MFTD – multiferroic tunnel diode

Potential Supplemental Applications

- Image recognition
- Speech recognition
- DSP (cross correlation)
- Data Mining
- Optimization
- Physical simulation
- Sensory data processing (biological, physical)
- Image creation
- Cryptographic analysis

Illustrative Example

Top down information processing Image Recognition

Saliency detector
Capturing moving objects in the complicated background

Stereo-vision chip
Real-time range detection

Visual pre-processor
Feature vector generation for image recognition

Memory of Past Experience

Template Memory

Matching Circuitry

Recalling maximum-likelihood event

Analog Associative Processor

Digital Associative Processor

Ferroelectric Associative Processor

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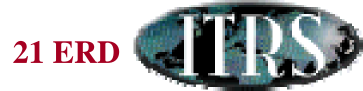


Specialized devices for image recognition

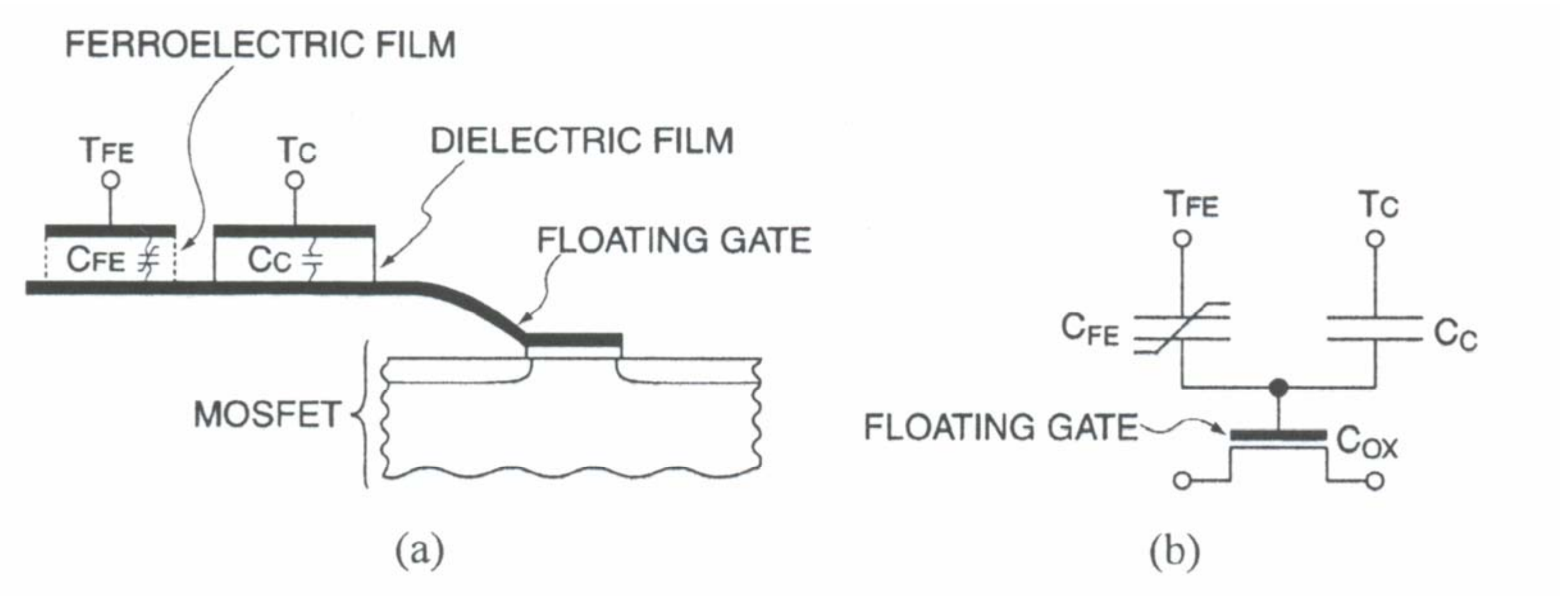


Fig. 1. (a) Conceptual drawing of the basic structure of the heterogate FGMOS. (b) Symbol representing the device.

Heterogate ferroelectric FGMOS FET

Tadashi Shibata, University of Tokyo

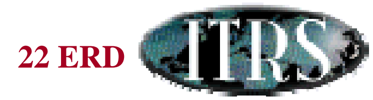


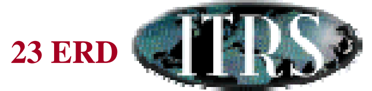
Image recognition

TABLE I
PERFORMANCES COMPARISON OF IMAGE RECOGNITION SYSTEMS

Search target: Sella (a pituitary gland)
Number of templates (generated by learning algorithm): 15
Search Area: 75x100-pel area

	Power(W)	Computational time (Second)	Total energy(J)
Pentium 4 1.5GHz Optimized in an assembly language level	54.7	5	273.5
Mobile Pentium 3 500MHz/1.1V Optimized in an assembly language level	3.5	15	52
Our digital vector generator & neural analog associative processor	0.152	1.2	0.182

Tadashi Shibata, University of Tokyo



Summary

- **Scope:** Broaden scope to encourage emerging technologies both to supplement CMOS as well as eventually to invent the new "switch".
- **Materials Section**: Spin out a new cross-cut chapter on Emerging Research Materials.
- **Memory Section**: Added NEMS mechanical memory to section.
  - Divide Emerging Memory Tables into Resistive and Capacitive subcategories
  - Updated section in 2007.
- **Logic Section**: Reformulated Logic Device Section to encourage high potential, but high risk approaches while maintaining Technology Entry evaluation function.
  - Re-considered status of candidate Technology Entries.
  - Re-structured Logic Section.
- **Architecture Section**: Revised section to focus on encouraging research to explore optimal organization of emerging non-linear devices to efficiently realize accelerator-like functions to supplement the CMOS platform technology.