



Results and Issues for 2007 ITRS

Process Integration, Developments, and Structures (PIDS) Working Group

ITRS Public Conference
Makuhari-Messe, Japan
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PIDS Roster

Taiwan

- R. Liu (Chair)
- Y. J. Mii
- C. Diaz
- M. Ma (Co-chair)
- M. J. Tsai
- E. Po

Korea

- I. S. Yeo
- K. H. Lee

Europe

- T. Skotnicki (Chair)
- K. Schrufer
- S DeLeonibus
- K. De Meyer
- R. Lander
- M. Jurczak

Japan

- K. Imai (Chair)
- T. Sugii
- S. Sawada
- S. Oda
- T. Hiramoto
- S. Takagi
- K. Shibahara
- A. Hori
- D. Hisamoto
- T. Nakamura
- Y. Tadaki
- Y. Tagawa
- Y. Takeda
- N. Kasai
- Y. Akasaka
- H. Inoue
- M. Yoshimi
- M. Mifuji
- M. Ogura
- J. Ida

Japan (con't)

- T. Tanaka
- Y. Kiyota
- M. Fujisawa
- T. Eimori

• US

- P. Zeitzoff (Chair)
- J. Chung
- J. Brewer
- A. Lochtefeld
- M. Rodder
- W. Maszara
- T. Ning
- G. Yeap
- M. Duane
- T. Dellin
- W. Tsai
- J. Hutchby
- K. Sprall



PIDS Subcategories

■ Logic

- High-performance
- Low operation power
- Low standby power

■ Memory

- DRAM
- Non-volatile memory (NVM)

■ Reliability

International Technology Roadmap for Semiconductors

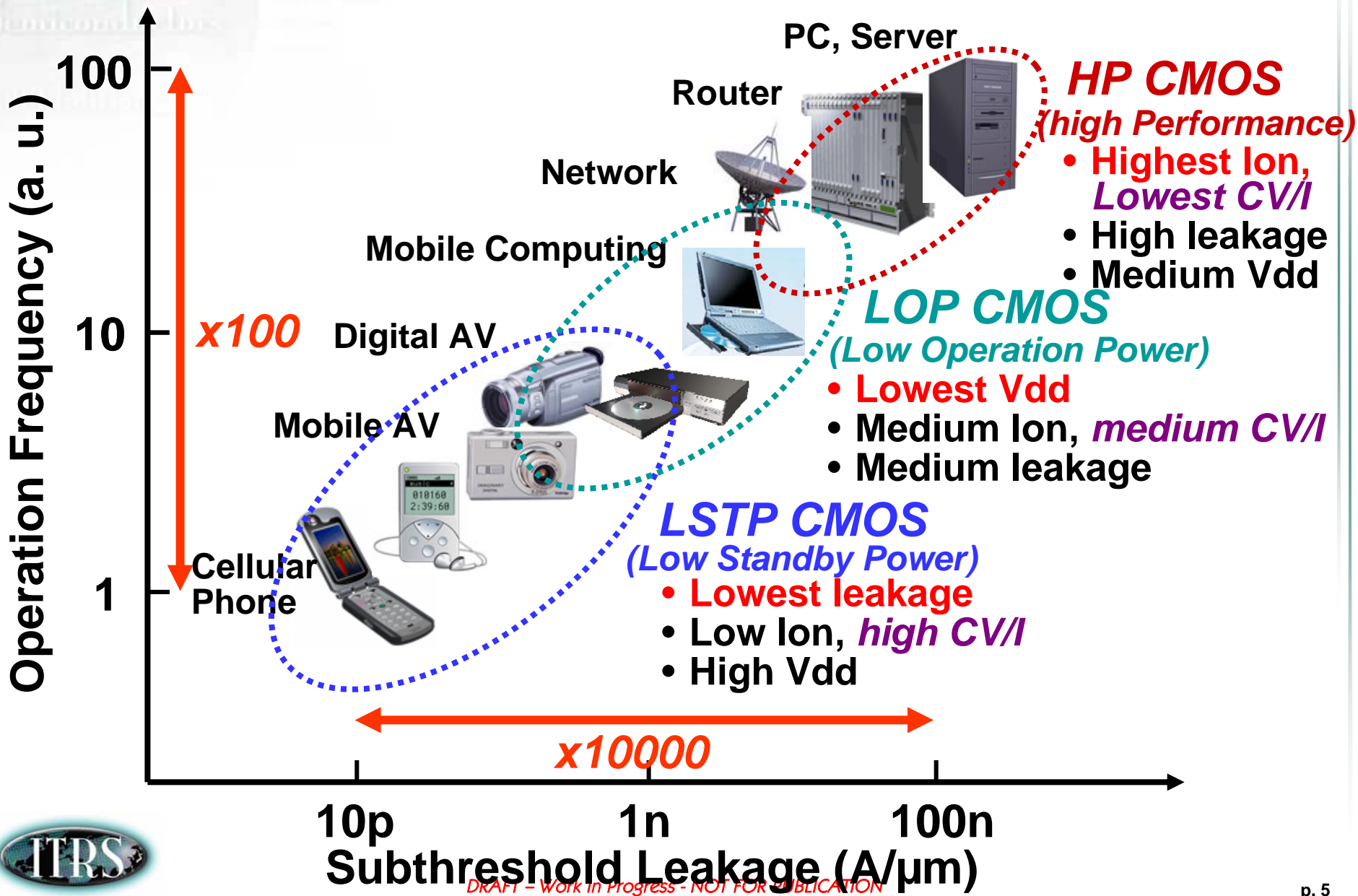
Outline

■ *Logic*

■ Memory



Logic CMOS Device Categories



Scaling Scenario in ITRS2007

MASTAR (detailed analytic device model from STM) is used to examine tradeoffs while generating technology requirements tables for logic devices.

■ HP CMOS

- Switching speed ($f_i = 1/[CV/I]$) improvement target is 17% per year.
- Metal gate/high-k will be introduced in 2008 (2 years ahead of ITRS06 projection).

■ LSTP CMOS

- Switching speed ($f_i = 1/[CV/I]$) improvement target is 14% per year
- Upper limitation of subthreshold leakage current will be relaxed from 10 pA/um to 30 pA/um.
- Supply voltage will be lowered to 1.0V with metal gate/high-k introduction in 2008.

■ Both

- Multiple parallel path (Bulk, UTB-FDSOI, FinFET) scenario is proposed.
- Variability of SRAM will become a critical issue for planar FET



High Performance Logic Technology Requirements Table

Year of Production			2007	2008	2009	2010	2011	2012	2013
Metal 1 ½ Pitch (nm)		IS	68	59	52	45	40	36	32
Lg: Gate Length (nm)		IS	25	22	20	18	16	14	13
Vdd: Supply Voltage (V)		IS	1.1	1.0	1.0	1.0	0.95	0.9	0.9
Tinv (nm)	Planer Bulk	WAS	1.84	1.70	1.6	0.92	0.75	0.75	
		IS	1.84	1.21	1.04	0.93	0.82	0.76	
	UTB-FDSOI	IS				1.1	1.0	0.95	0.9
	Double Gate	IS					1.2	1.1	1.0
Rsd ($\Omega\text{-}\mu\text{m}$)	Planar Bulk	IS	200	200	200	180	180	180	
Isd, leak ($\mu\text{A}/\mu\text{m}$)	Planar Bulk	IS	0.34	0.71	0.70	0.64	0.74	0.68	
	UTB-FDSOI	IS				0.33	0.52	0.62	0.56
	Double Gate	IS					0.2	0.34	0.37
Id, sat ($\mu\text{A}/\mu\text{m}$)	Planar Bulk	IS	1211	1513	1639	1807	1824	1762	
	UTB-FDSOI	IS				1948	2000	1944	2109
	Double Gate	IS					1917	1943	2204



Low Standby Power Logic Technology Requirements Tables

Year of Production			2007	2008	2009	2010	2011	2012	2013
Metal 1 ½ Pitch (nm)		IS	68	59	52	45	40	36	32
Lg: Gate Length (nm)		IS	45	37	32	28	25	22	20
Vdd: Supply Voltage (V)		WAS	1.2	1.1	1.1	1.1	1.0	1.0	1.0
		IS	1.1	1.0	1.0	1.0	1.0	1.0	1.0
T _{inv}	Planar Bulk	WAS	2.3	1.9	1.8	1.7	1.6	1.5	1.4
		IS	2.52	1.93	1.84	1.73	1.62	1.51	1.41
	UTB-FDSOI	IS						1.7	1.6
	Double Gate	IS						1.8	1.7
R _{sd} (Ω-μm)	Planar Bulk	IS	180	180	180	180	165	160	160
I _{sd, leak} (pA/μm)	Bulk Planer	WAS	10	10	10	10	12	16	21
		IS	30.3	30.3	30.5	30.7	30.2	30.2	30.3
	UTB-FDSOI	IS						31.4	30.9
	Double Gate	IS						11.5	24.4
I _{d, sat} (μA/μm)	Planar Bulk	IS	465	569	501	528	542	560	519
	UTB-FDSOI	IS						608	669
	Double Gate	IS						550	612



Major Technology Innovations Required Over the Next Few Years

In order to maintain scaling trend of $f_i = 1/[CV/I]$, **equivalent scaling with material and structural innovations** are required

		2005	2010	2015	2020		
MPU/ASIC M1 1/2 Pitch (nm)		90	68	45	32	22	16
Gate Stack	HP	PolySi / SiON	Metal gate / High-k				
	LSTP	PolySi / SiON	Metal gate / High-k				
Transistor Structure	HP	Planar Bulk	UTB-FDSOI				
		Parallel paths	Double Gate (FinFET)				
	LSTP	Planar Bulk	UTB-FDSOI				
		Parallel paths	Double Gate (FinFET)				



Requirement for Quasi-ballistic Transport

1. Gate length (L_g) scaling
 $L_g \sim$ Mean free path (λ)
→ Aggressive L_g scaling to 20nm or less
2. Suppression of carrier scattering in intrinsic (=channel) region
→ Undoped channel (=fully depleted)
3. Reduction of parasitic resistance in extrinsic (=source/drain) region
→ Potentially, Schottky S/D

K. Natori

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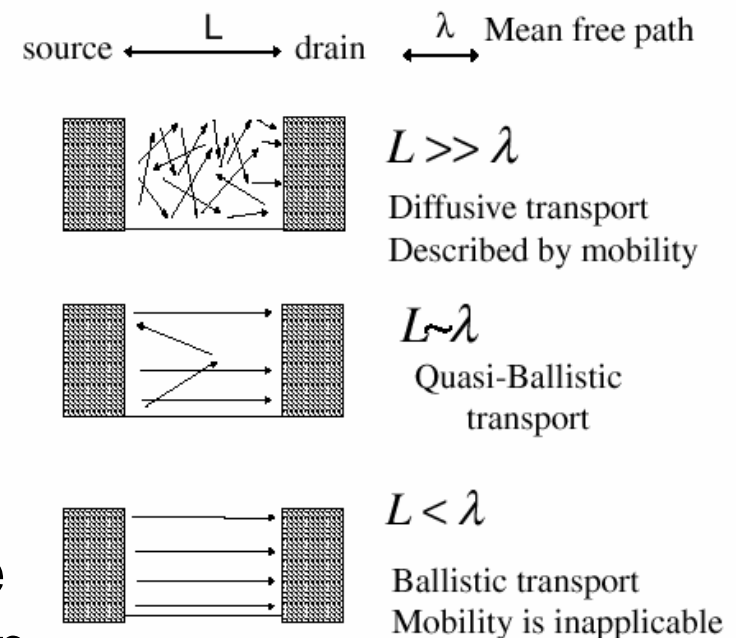
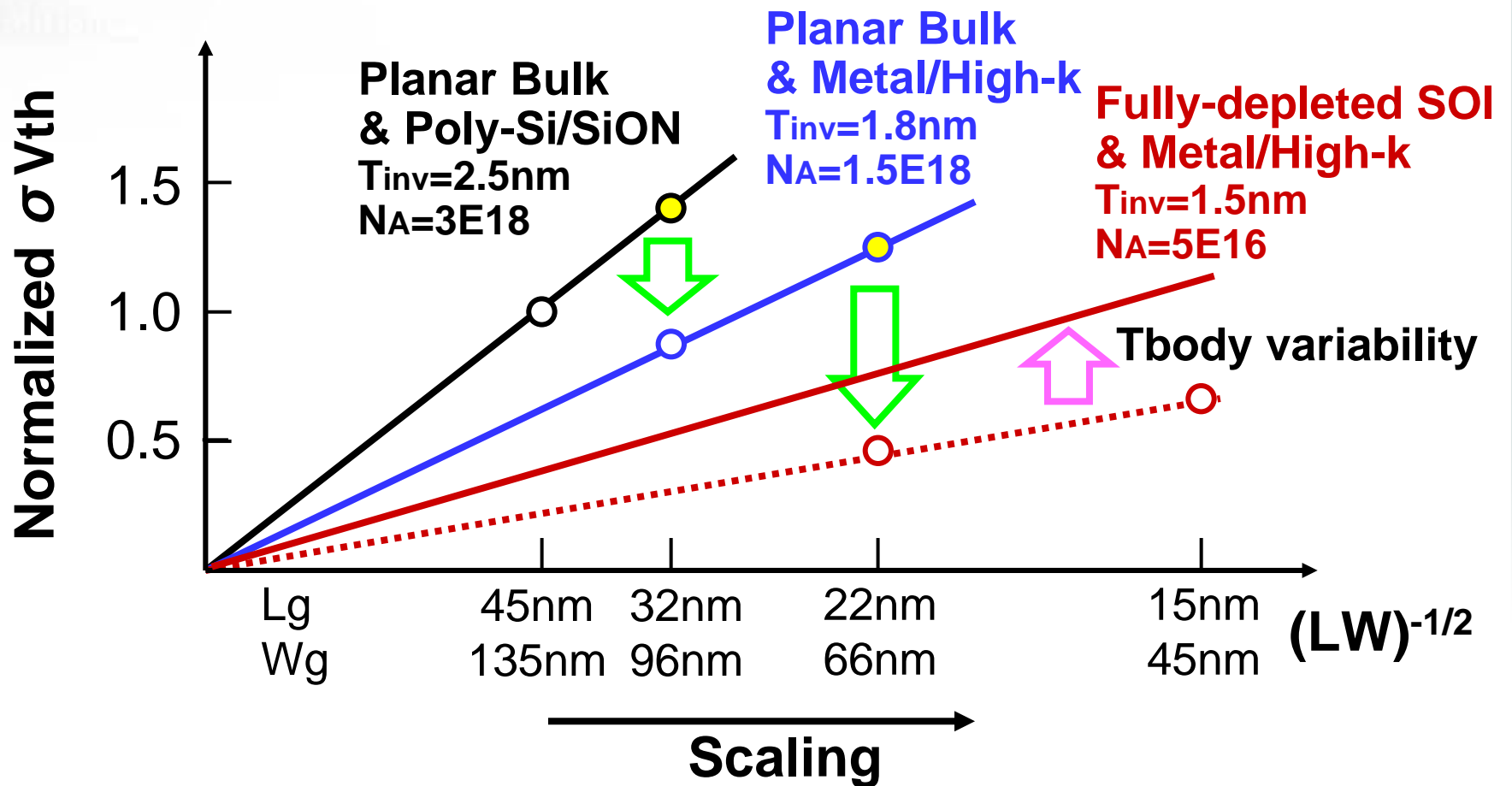


Fig. 1. Classification of carrier transport in MOSFETs.

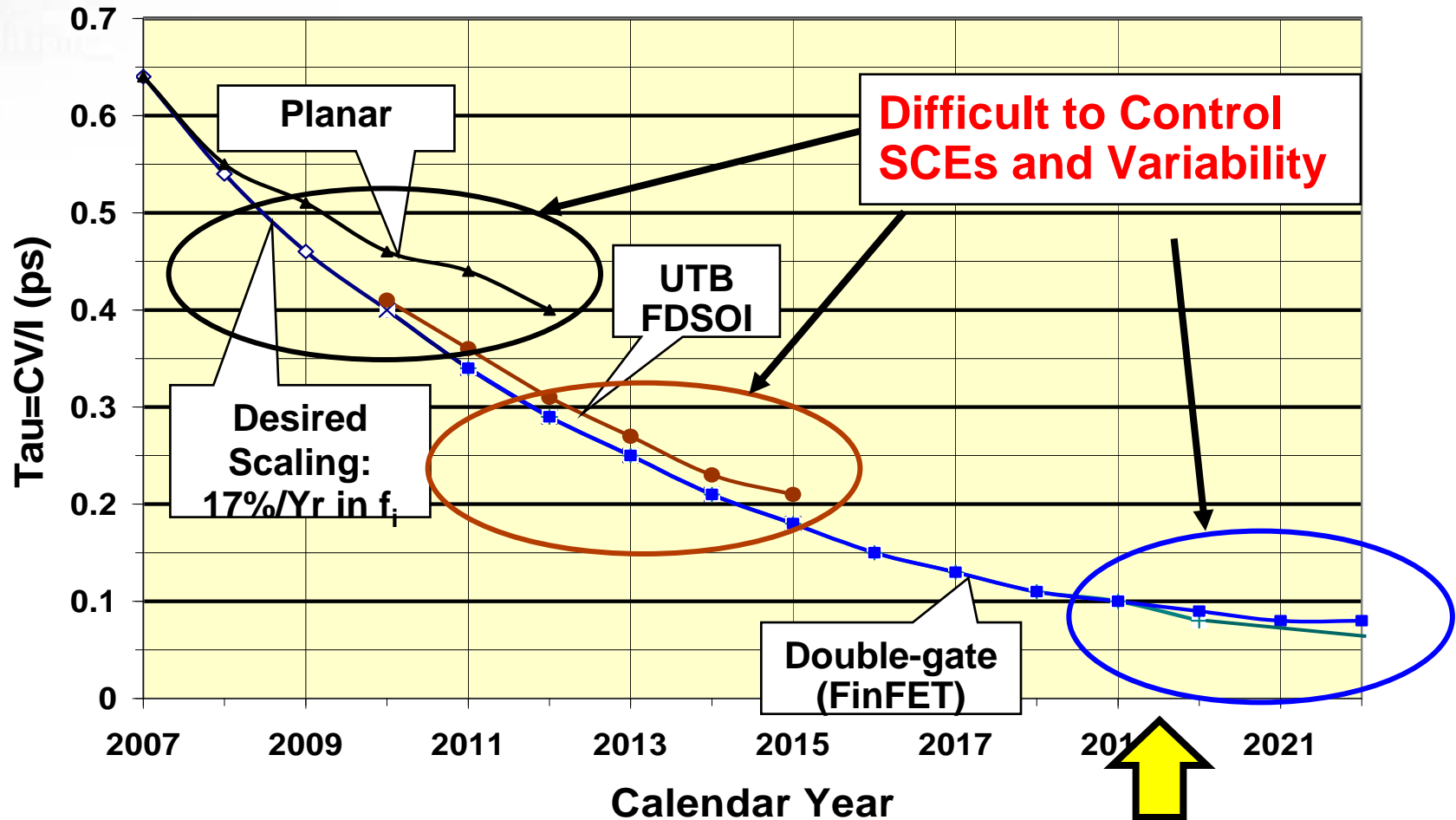
Random Variability Reduction Scenario



Assumption: Random dopant fluctuation is Main source of Random Variability: Line width roughness of Lg and Wg is not considered in this estimation.



High-Performance Logic: Scaling of Transistor Speed Metric, $f_i=1/[CV/I]$



Alternative material (Ge, III-V) and structure (Nanowire) in channel region.



Key issues to 2008

- **Gate length (L_g) scaling for HP in the 2007 ITRS is too aggressive, especially in 2007-2010 time frame → We will survey L_g trend.**
- **We need to consider SRAM transistor issues (leakage, mismatch, SNM, power dissipation).**
- **We need to consider introduction of alternative channel material (Ge, III-V) as well as alternative channel structure (Si nanowire) in year of 2019 time frame.**



International Technology Roadmap for Semiconductors

Outline

■ Logic

■ *Memory*



NAND Flash: Key Directions for 2007 ITRS based on Survey Results

- **Fundamental survey has been completed and summarized.**
- **NAND Flash Scaling is accelerated in 2007 ITRS.**
 - **One year pull from ITRS 2005. As a result, NAND Flash scaling has pulled 2years ahead of DRAM scaling.**
(NAND Flash F is pitch of NAND cell (uncontacted), DRAM is M1(Bit line) pitch)
- **Technology**
 - **3bit/cell technology will be released, after 2bit/cell technology. (before 4bit/cell technology)**
 - **NAND cell technology will migrate from FG type cell to CTF (Charge Trap Cell) type cell**
 - **In consequence, NAND cell structure will migrate over to CTF + 3D structure in 2013.**



NAND Flash Technology over view

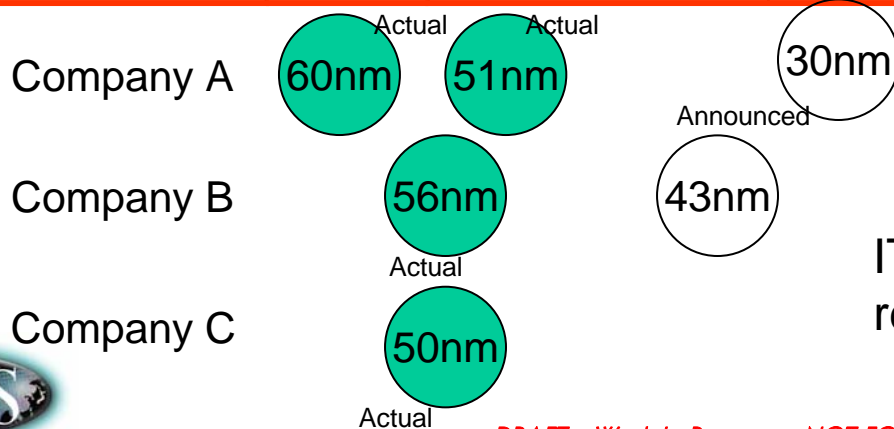
Year of Production	2007	2008	2009	2010	2011	2012	2013
DRAM ½ Pitch (nm) (contacted)	65	57	50	45	40	35	32
NAND Flash							
NAND Flash technology node – F (nm) [1]	51	45	40	36	32	28	25
Number of word lines in one NAND string [2]	32	32	64	64	64	64	64
Cell type (FG, CT, 3D, etc.) [3]	FG	FG	FG	FG/CT	CT	CT	CT-3D
A. Floating Gate NAND Flash							
Maximum number of bits per cell (MLC) [12]	2	2	3	4	4	4	4
B. Charge trapping NAND Flash (MANOS or Barrier Engineering) [13]							
Maximum number of bits per cell (MLC)				4	4	4	4



ITRS 2007 vs public information

ITRS 2005									
2004	2005	2006	2007	2008	2009	2010	2011	2012	2013
90nm	76nm	64nm	57nm	51nm	45nm	40nm	36nm	32nm	28nm
ITRS 2005	$x1/\sqrt{2}$ ($x0.71$)	←	$x0.794$	←	←	$x0.794$	←	←	←
Cell Size	Half in 2years		Half in 3years			Half in 3years			

ITRS 2007								
ITRS 2007	2006	2007	2008	2009	2010	2011	2012	2013
	64nm	54nm	45nm	40nm	36nm	32nm	29nm	25nm
Cell size	Half in 2years		Half in 3years			Half in 3years		



ITRS 2007 is more likely to trace the real products.



December 2007 ITRS PIDS NVM

- **Major revisions for 2007 NVM section**
 - Separate NOR and NAND applications.
 - NOR and NAND subsections include floating gate and nitride storage (charge trapping, or CT) devices.
 - NAND subsection includes 3-D and MLC devices.
 - Emerging NVM renamed “Non-charge-storage memories”. It contains FeRAM, MRAM and PCRAM.
- **NAND and NOR updates based on surveys of major suppliers conducted in 2007.**
 - Thanks to Japan PIDS group for the NAND survey.
- **FeRAM, PCRAM entries updated, but MRAM not changed significantly due to slow advances in 2006/2007**
 - Thanks to Japan FEP and PIDS groups.
 - Included spin transfer torque approach for MRAM cell size reduction.



2008 Plans for ITRS PIDS NVM

- **New issues for 2008**
 - **Address NAND as a technology driver issue**
 - **Work between PIDS and Litho iTWGs**
 - **CT (charge trapping) and 3-D NAND introduction time**
 - **How far can floating gate NAND scale?**
 - **How many bits per cell can MLC achieve?**
 - **Random telegraph noise limitation and ECC area overhead**
 - **Whether PCRAM products will be introduced in 2008/2009?**
- **Will not do a new NOR survey since change is relatively slow.**
- **Will do a new NAND survey due to rapid changes in NAND technology and market, as well as NAND being one of the technology drivers.**



DRAM Survey Carried Out in Mid-to-Late 2006, Analysis Completed

- ● ● 1. DRAM half pitch (minimum feature size : F)
- ● ● 2. Cell size : A_{cell}
- ● ● 3. Cell size factor : a [$A_{cell} = a F^2$]
- ● ● 4. DRAM Product (bit) : b
- ● ● 5. Chip size : A_{chip}
- ● ● 6. Area factor [= $A_{cell} \times b / A_{chip}$]
- ● ● 7. Retention time
- ● ● 8. Storage Capacitance : C_s
- ● ● 9. Voltage of capacitor
- ● ● 10. Gate oxide thickness of cell transistor
- ● ● 11. Maximum word-line level
- ● ● 12. Effective electric field of gate insulator
- ● ● 13. Negative word-line use
- ● ● 14. Capacitor structure
- ● ● 15. Capacitor insulator material
- ● ● 16. Effective capacitor insulator thickness
- ● ● 17. Physical capacitor insulator thickness
- ● ● 18. Support FET (EOT, Ion, V_t)
- ● ● 19. Array FET structure

- Overall Table
- PIDS Table
- FEP Table

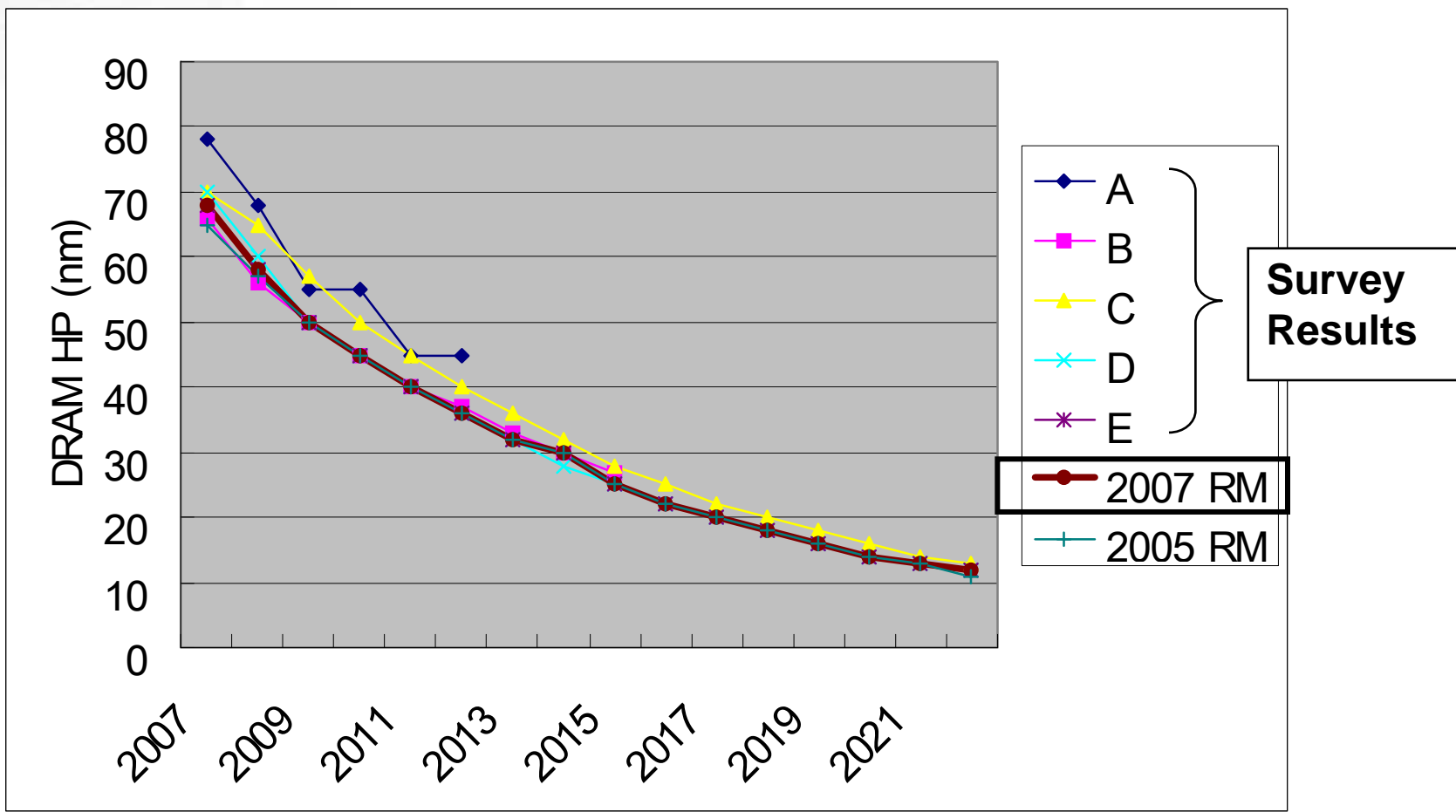


DRAM: Key Directions for 2007 ITRS, per Survey Results

- **Feature size scaling unchanged from 2005 ITRS**
 - **F = half-pitch of contacted M1 : 3 year cycle**
 - 65nm in 2007, 45 nm in 2010
- **Other results**
 - **Cell size factor, $a=(\text{cell area})/F^2$**
 - $a=8$ through 2005, $a=6$ in 2006 and thereafter
 - 2-years pull-in from 2005 ITRS
 - **DRAM product generation: 1 year delay from 2005 ITRS**
 - 4Gb delayed from 2009 until 2010
 - **Capacitor equivalent oxide thickness, T_{eq}**
 - T_{eq} is unchanged from 2005 ITRS up to 2010
 - Ultra-high-k dielectric (new material) needed beyond 2010



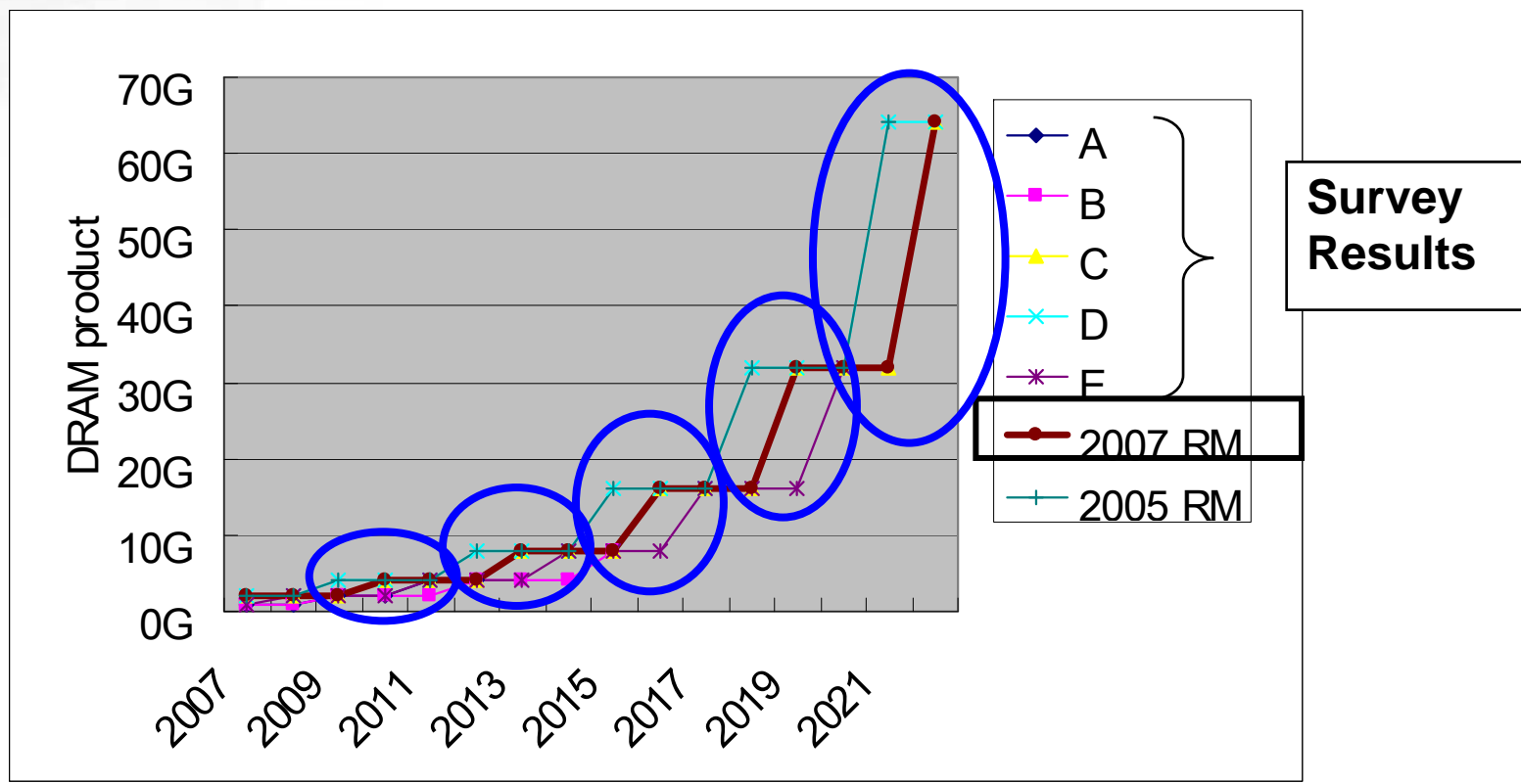
Scaling of DRAM Half Pitch (F)



The same as in 2005 version



DRAM Product Generation (in Gb)

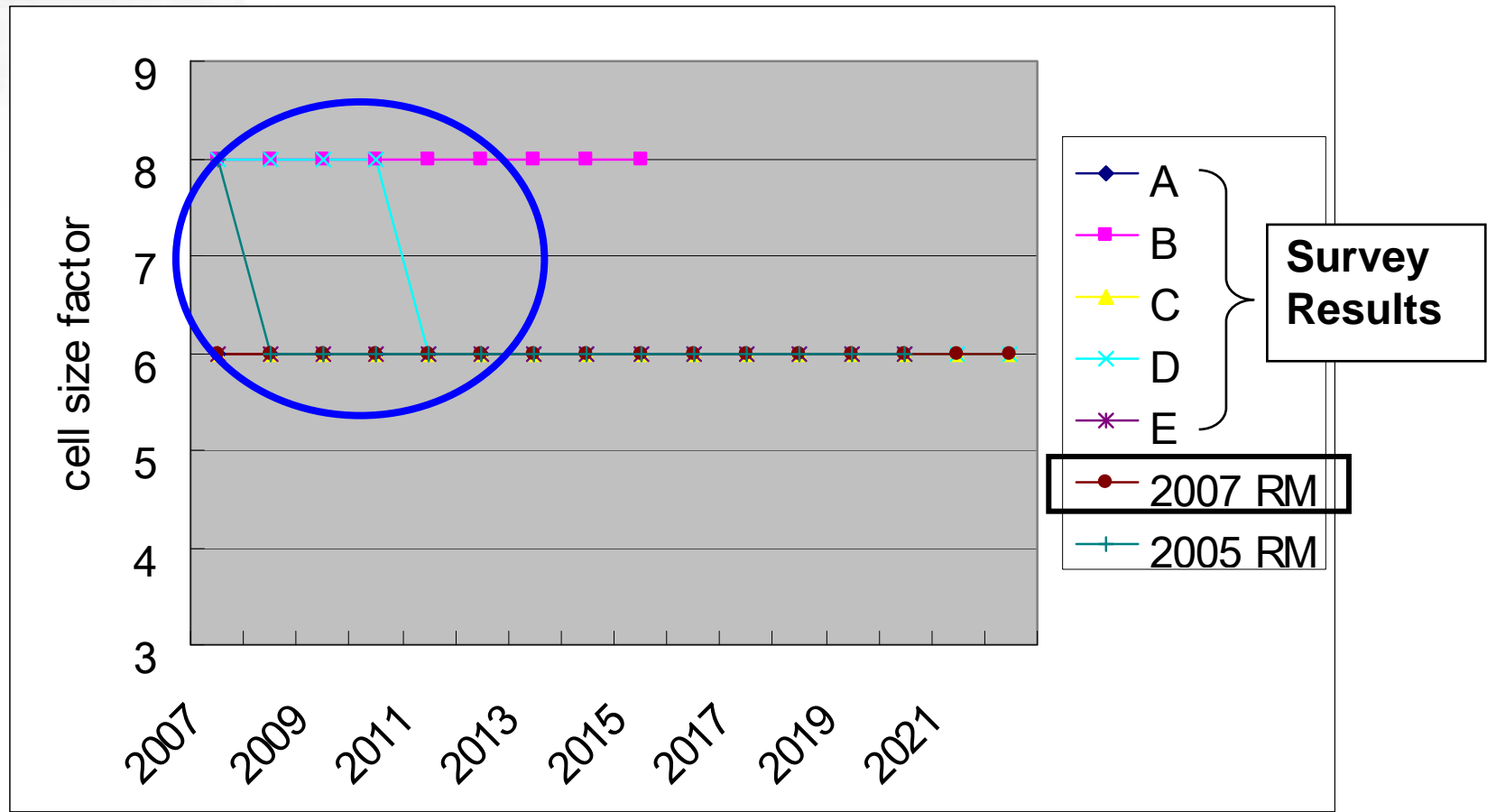


	2007	2008	2009	2010	2011	2012	2013	2014	2015	2016
2007 RM	2	2	2	4	4	4	8	8	8	16

1 year delay against 2005 version



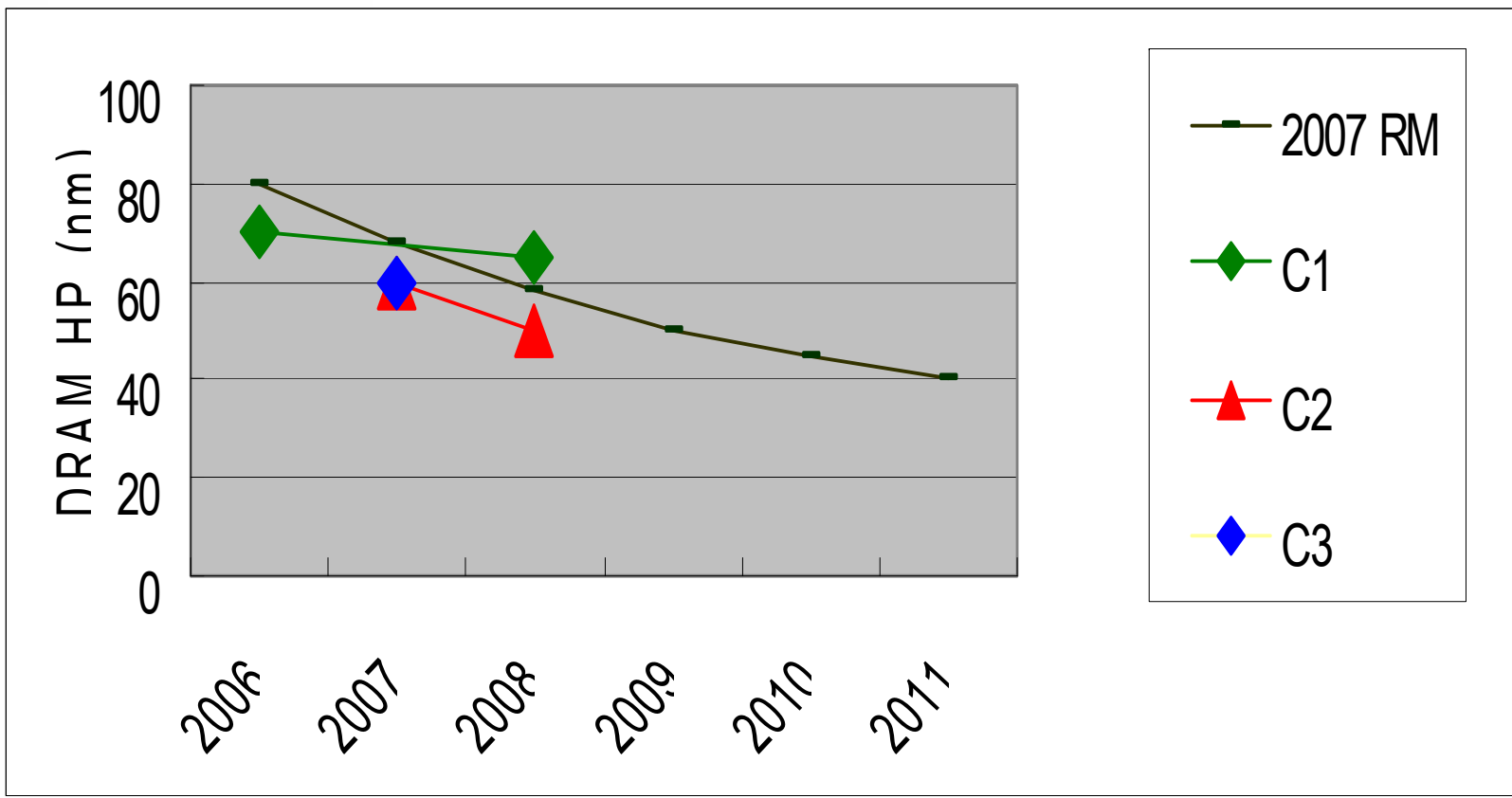
Scaling of Cell Size Factor, a



6F² starts in 2006 (two year pull-in)



Press release for DRAM HP



Summary

■ Logic

- Equivalent scaling with material and structural innovations will be required.
- Metal gate and high-k projected for 2008
- High Performance: great difficulty in scaling planar bulk MOSFETs to 2009 and beyond
→ Double-gate MOSFETs

■ Memory

- DRAM: scaling continuing
- NAND: Accelerate 1year
- Numerous different types of NVM, with unique attributes and scaling scenarios

