Assembly and Packaging

July 18, 2007

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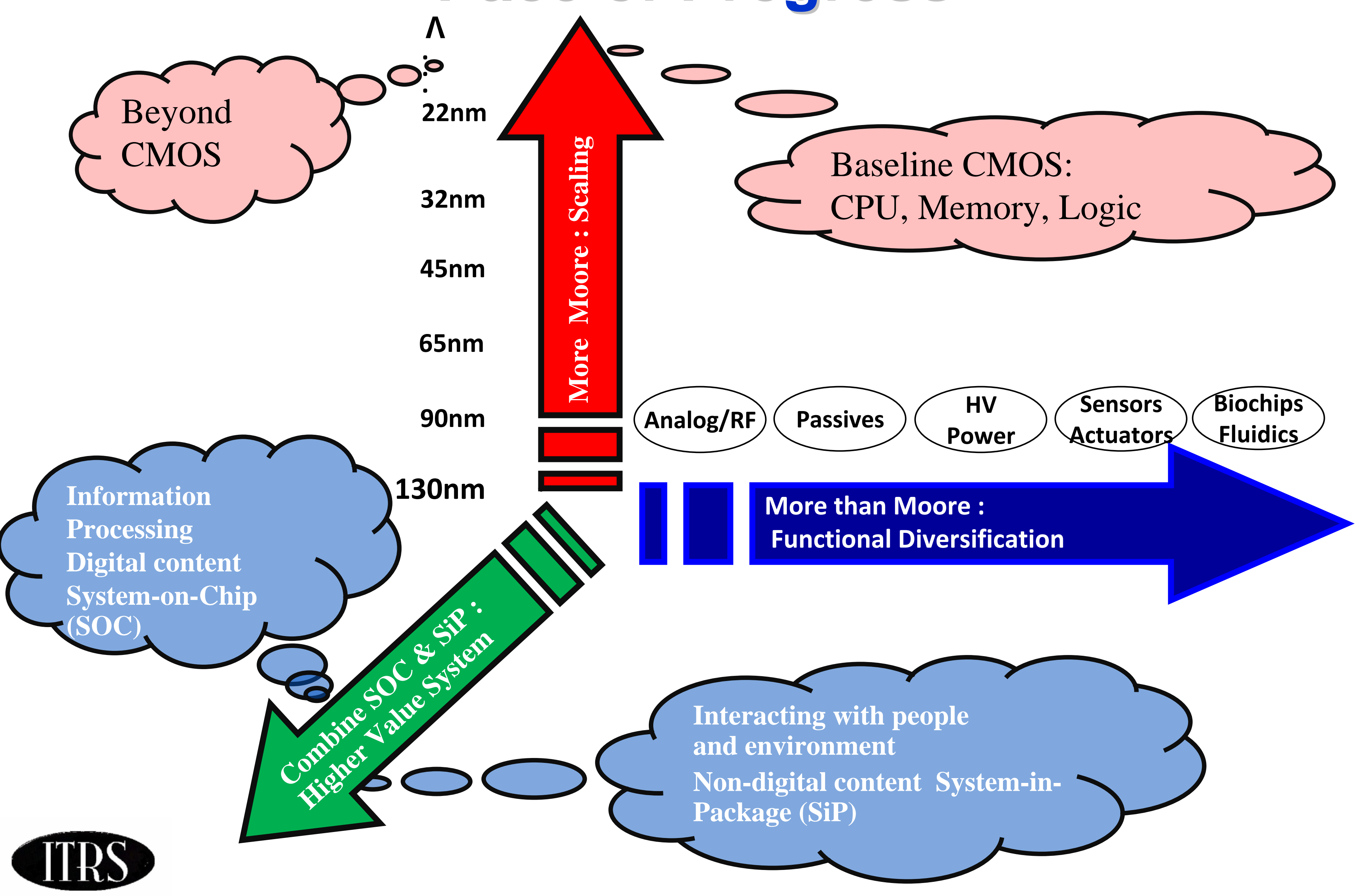
Moore's Law Scaling can not maintain the Pace of Progress



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Packaging is now a limiting factor but it is enabling for More than Moore

- Packaging has become the limiting element in system cost and performance
- The Assembly and packaging role is expanding to include system level integration functions.
- As traditional Moore's law scaling become more difficult innovation in assembly and packaging can take up the slack.

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System Level Integration

System
on Chip

Cost / function
Time to market

Bio-Interface

Power supply

MEMS

SiP and 3D Packaging

System complexity

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The Pace of Change in Packaging is Accelerating

- As traditional CMOS scaling nears it natural limits other technologies are needed to continue progress
- This has resulted in an increase in the pace of innovation.
- Many areas has outpaced ITRS Roadmap forecasts. Among these are:
  - Wafer thinning
  - Wafer level packaging
  - Incorporation of new materials
  - 3D integration

The consumerization of electronics is the primary driving force.

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Wafer Thinning

It was easier than we thought.

Table 102a&b Thinned Silicon Wafer Thickness 200 mm/300 mm

Year of Production	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*	*2014*	*2015*
Min. thickness of thinned wafer (microns) (general product)	50	50	50	50	45	40	40	40	40
Min. thickness of thinned wafer (microns) (For extreme thin package ex. Smart card)*	20	20	15	15	10	10	10	10	8

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New Materials

- In this decade most if not all packaging materials will change due to changing functional and regulatory requirements
  - Bonding wire
  - Molding compounds
  - Underfill
  - Thermal interface materials
  - Die attach materials
  - Substrates
  - Solder

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3D Integration

Table 101 System-in-a-Package Requirements

Year of Production	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*	*2014*	*2015*
Number of terminals—low cost handheld	700	800	800	800	800	800	800	800	800
Number of terminals—high performance (digital)	3050	3190	3350	3509	3684	3860	4053	4246	4458
Number of terminals—maximum RF	200	200	200	200	200	200	200	200	200
Low cost handheld / #die / stack*	7	8	9	10	11	12	13	14	14
high performance / die / stack	3	3	3	4	4	4	5	5	5
Low cost handheld / #die / SiP	8	8	9	11	12	13	14	14	14
high performance / #die / SiP	6	6	6	7	7	7	8	8	8
Minimum TSV pitch	10.0	8.0	6.0	5.0	4.0	3.8	3.6	3.4	3.3
TSV maximum aspect ratio**	10.0	10.0	10.0	10.0	10.0	10.0	10.0	10.0	10.0
TSV exit diameter(um)	4.0	4.0	3.0	2.5	2.0	1.9	1.8	1.7	1.6
TSV layer thickness for minimum pitch	50	20	15	15	10	10	10	10	8
Minimum component size (micron)	1005	600x300	600x300	400x200	400x200	400x200	200x100	200x100	200x100

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The Pace of Change is Accelerating and introducing new challenges

- New failure mechanisms
- Slow rate of innovation in low cost, high density package substrates
- Limited tool availability for Co-design and modeling 3D electronic structures

Assembly and Packaging Technical working Group 2007 Focus

We are giving special focus to preparation of a white paper titled:

"The next step in Assembly and Packaging:

Systems Level Integration"

Objectives of this white paper

- Catalyze a new SiP chapter ITRS
- Identify needs and gaps
- Identify new technology trends for future SiP

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System-in Package definition

System in Package (SiP) is a combination of multiple active electronic components of different functionality, assembled in a single unit, that provides multiple functions associated with a system or sub-system. An SiP may optionally contain passives, MEMS, optical components and other packages and devices.

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SiP - Situation Analysis

- Market: In 2004, 1.89 Billion SiPs were assembled. By 2008, this number is expected to reach 3.25 Billion, growing at an average rate of about 12% per year.
- Technology: SiP applications have become the technology driver for small components, packaging, assembly processes and for high density substrates.
- Growth: System in Package (SiP) has emerged as the fastest growing packaging technology segment although still representing a relatively small percentage of the unit volume.

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Categories of SiP

<table>
<tr><td colspan="2">Horizontal Placement</td><td>Wire Bonding Type
Flip Chip Type</td></tr>
<tr><td rowspan="2">Stacked Structure</td><td>Interposer Type</td><td>Wire Bonding Type
Wire Bonding + Flip Chip Type
Flip Chip Type</td></tr>
<tr><td>Interposer-less Type</td><td>Terminal Through Via Type</td></tr>
<tr><td colspan="2">Embedded Structure</td><td>Chip(WLP) Embedded + Chip on Surface Type
3D Chip Embedded Type
WLP Embedded + Chip on Surface Type</td></tr>
</table>

Source: 20030710 K. Nishi, Hitachi, JEITA, Revised by H. Utsunomiya

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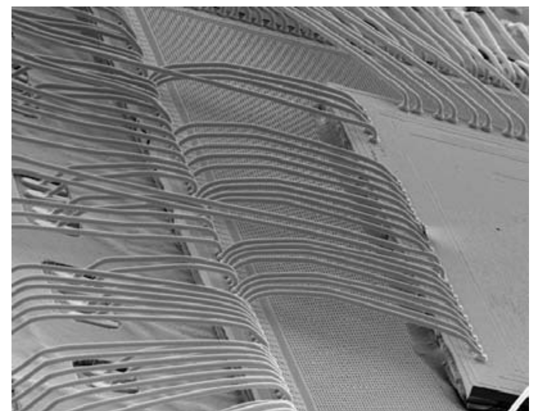
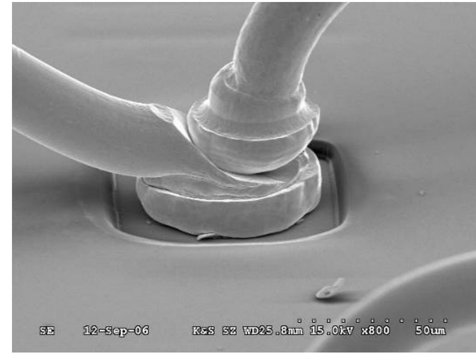
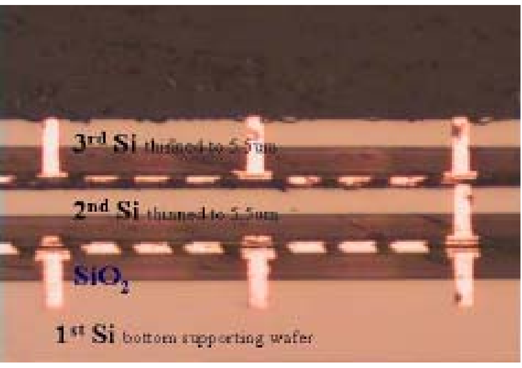
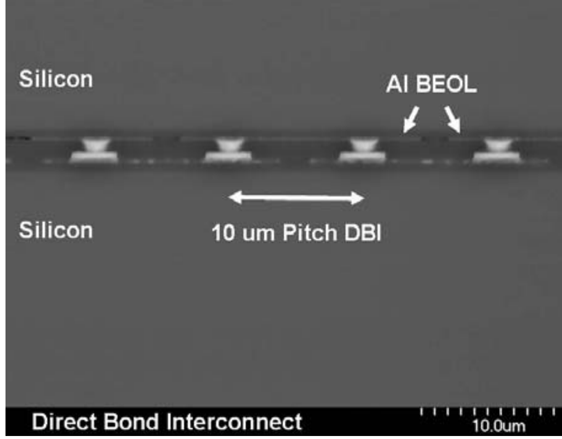
3D Stacked Die Package

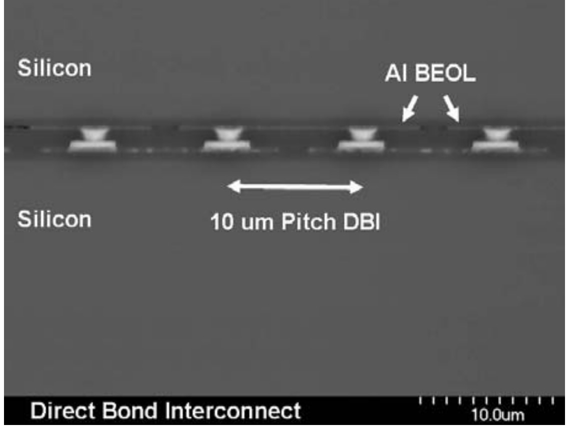




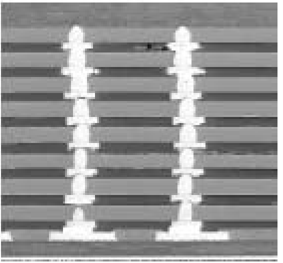


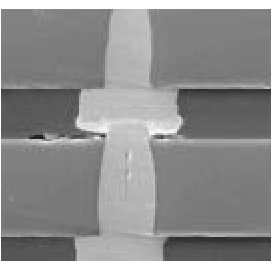
TSV of Tezzaron

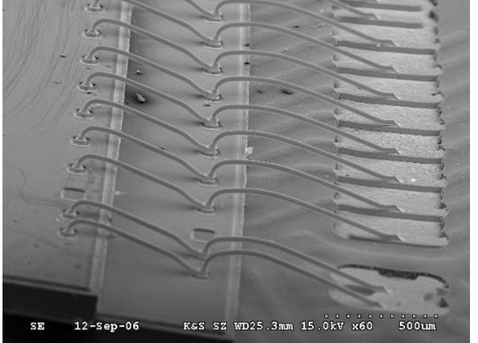




TSV of Ziptronix







Samsung TSV
Laser drill, plating,
50 micron thick

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Typical SiP in 2010

TSV

0.025mm

Mold resin thickness on
top of die: 0.10 mm

1.0

Substrate
thickness: 0.16

Ball pitch: 0.8 mm
Ball diameter: 0.4 mm

Die attach thickness
0.015

Embedded

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Wafer Level SiP - Vision

Energy source

MEMS

ASIC
+
memories

Cooling

Source: LETI

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ITRS projection for stacked die SiP packages

2014 through 2020

Table 101 System-in-a-Package Requirements

Year of Production	*2015*	*2016*	*2017*	*2018*	*2019*	*2020*	*2021*	*2022*
Low cost handheld / #die / stack*	14	15	15	16	16	17	17	18
high performance / #die / stack	5	6	6	6	7	7	7	8
Low cost handheld / #die / SiP	14	15	15	16	16	17	17	18
high performance / #die / SiP	8	9	9	9	10	10	10	11

Limited by thermal density

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SiP presents new Design Challenges for signal integrity, power integrity and shielding

- Signal integrity for high density interconnect
  - Cross talk
  - Impedance discontinuities (reflections)
  - Timing skew
  - Parasitic capacitance, resistance and inductance in long traces (inductance change for each layer for wire bonded stacked die)
- Power integrity
  - Voltage drop for high speed signals (lead and trace inductance limits power delivery)
  - Ground noise due to high frequency current variations
- Shielding
  - Radiated noise within the package at high frequency
  - External electromagnetic noise sources

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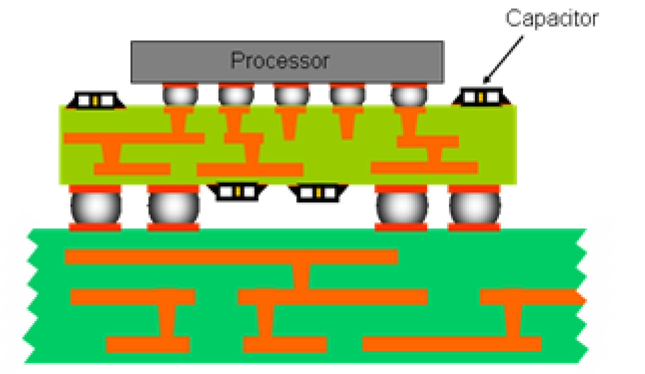
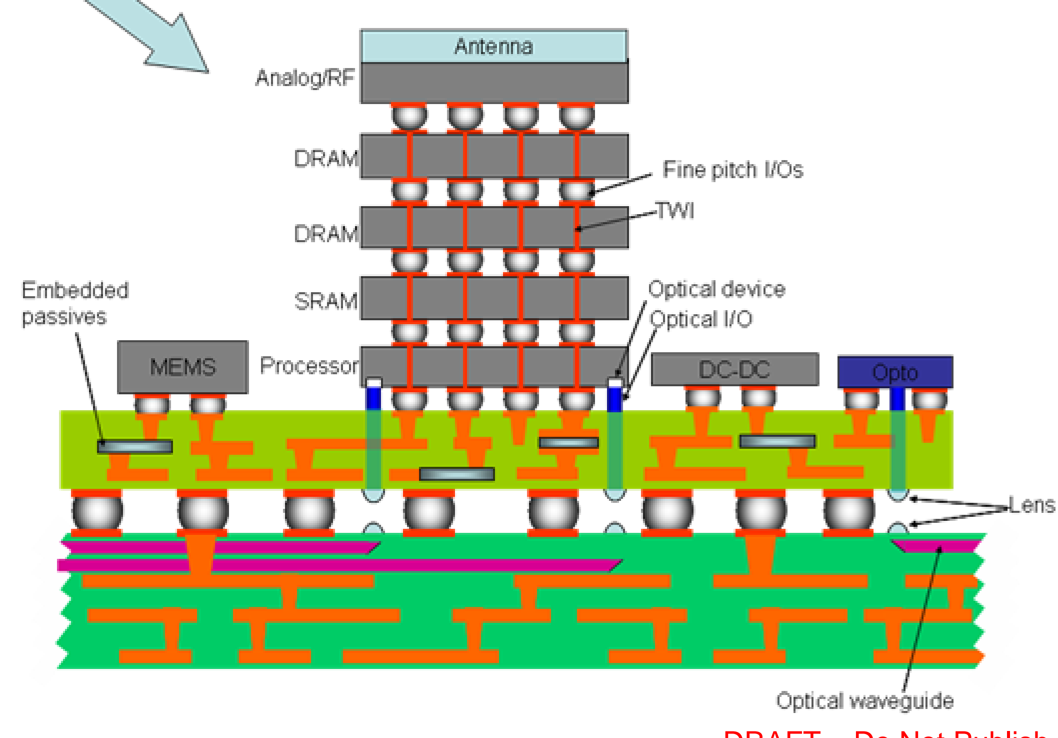
Interconnect Challenges for Complex SiPs



New circuit elements and components place expanded demands on the environment provided by the package

Evolutionary and revolutionary interconnect technologies are needed to enable the migration of microsystems from conventional state-of-art to 3D SiP.



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Potential Solutions for Interconnect Challenges

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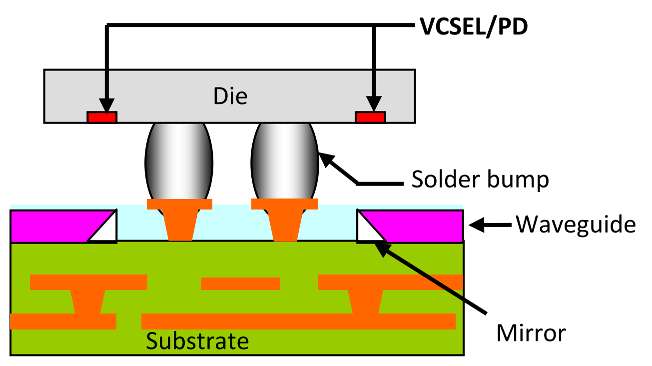
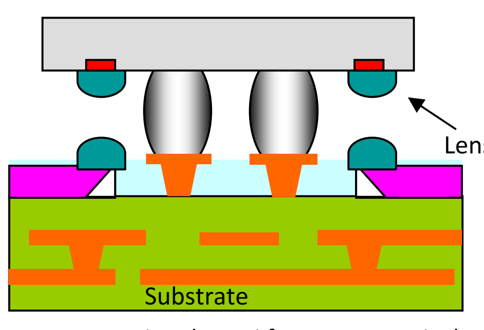
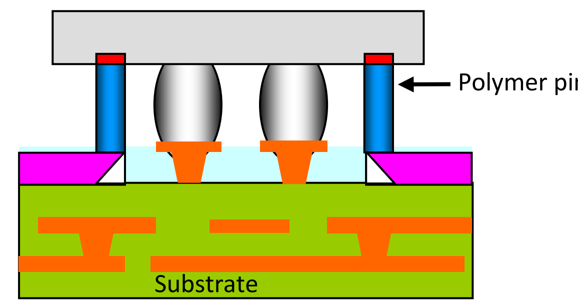
Interconnect Requirements may be satisfied by Wave Guide Optical Solutions



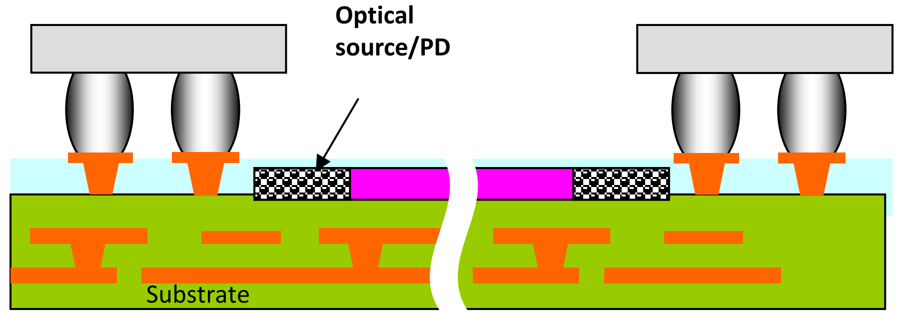
Quasi free-space optical I/O



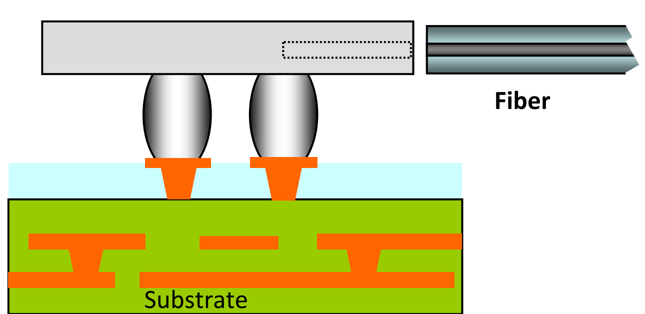
Lens assisted quasi free-space optical I/O



Surface-normal optical waveguide I/O



Board-level integrated optical devices



Fiber-to-the-chip

Examples of guided wave optical interconnects for chip-to-chip interconnection.

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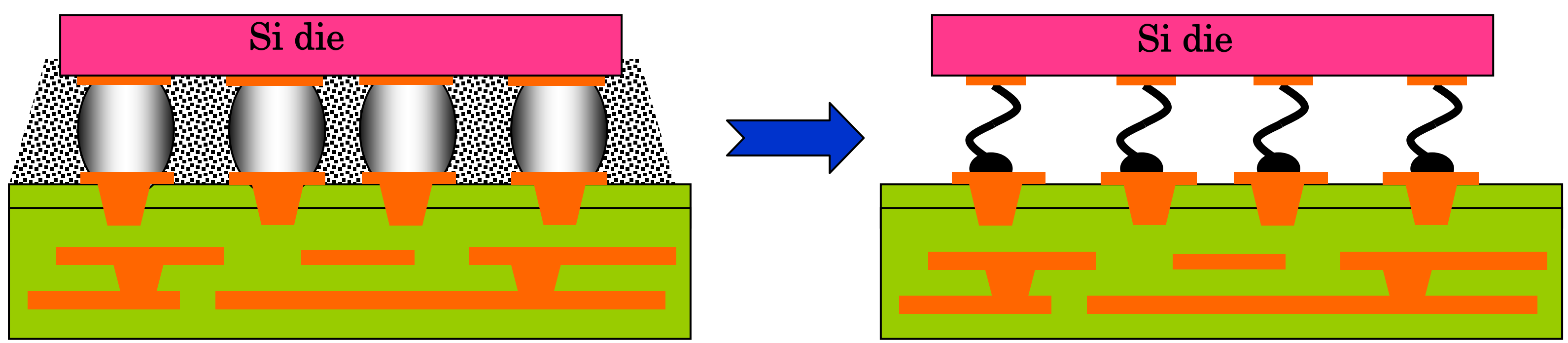
Low k ILD may Require Improved Underfill or Compliant I/O connections



The use of compliant electrical I/O can potentially eliminate the need for underfill reducing cost and processing complexity as I/O density rises.

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SiP presents new challenges for Thermal management

- High performance generates high thermal density
- Heat removal requires much greater volume than the semiconductor
  - Increased volume means increased wiring length causing higher interconnect latency, higher power dissipation, lower bandwidth, and higher interconnect losses
  - These consequences of increased volume generates more heat to restore the same performance
- ITRS projection for 14nm node
  - Power density >100W/cm2
  - Junction to ambient thermal resistance <0.2degrees C/W

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Thermofluidic Heat Sinks may be the Solution

Conventional thermal Interconnects

Die

Back-side integrated fluidic heat sink using TIM and inlets/outlets

Thermal interface Material

Back-side integrated fluidic heat sink and Back and front-side inlets/outlets

tube

fluidic I/O

Examples of thermofluidic heat-sink integration with CMOS technology.

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Test Challenges of SiP

- Test cost
- BIST and other Embedded test approaches
- Thermal management
- Test access
- Contactor/ Connection issues
- Single chip testing in SiP configurations
- Time to market

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Environmental Issues

2003 2004 2005 2006 2007

WEEE(Aug. 2005)
Recycle System set up

Mar. 2007
China
version
RoHS

ELV(2003/07)
Non-use of Lead (Pb)
Mercury (Hg)
Cadmium (Cd)
Hexavalent Chromium (Cr6+)

RoHS(Jul. 2006)
Non-use of Lead (Pb)
Mercury (Hg)
Cadmium (Cd)
Hexavalent Chromium (Cr6+)
Polybrominated biphenyls (PBB)
Polybrominated diphenyl ethers (PBDE)

REACH
(Under discussion)
Risk Assessment, and registration of Chemicals

There are several regulatory activities resulting from environmental considerations that will impact the future SiP technology as well as all other parts of the electronics industry. These include:

ELV: Directive on end-of life vehicles

RoHS: Directive on the restriction of the use of certain hazardous substances in electrical and electric equipment

WEEE: Directive on waste electrical and electronic equipment

EuP: Directive on the eco-design of Energy-using Products

REACH: Registration, Evaluation and Authorization of Chemicals

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Major Challenges

- Handling for ultrathin die
- Cost targets for new package types
- Co-Design tools for SiP, 3D packaging, TSV, etc.
- Handling increasing thermal density (particularly for 3D packaging)
- Incorporation of new materials
- Signal integrity for complex SiP

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Cross TWG "More than Moore" Cooperation

Product Optimization methodology

This is a long term project which is in its early definition phase. The current objective is to have a joint vision for this project in the 2009 Roadmap.

A number of the issues addressed in the *SiP White Paper* and the *Design Chapter of the ITRS Roadmap* provide a foundation for this project.

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Thank You