

# Front End Processes 2007 ITRS

**ITRS Public Conference  
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San Francisco**

**FEP ITWG Membership:**

**US: J. Butterbaugh (presenter), R. Jammy, L. Larson**

**Japan: I. Mizushima, M. Niwa, H. Kitajima, S. Kawamura, M. Watanabe**

**Europe: M. Alessandri, W. Mueller, C. Stapelmann**

**Korea: J.S. Roh, H.S. Rhee**

**Taiwan: H.H. Tsai**



# 2007 FEP Sub-TWGs and Chairs

- **Starting Materials**
  - Mike Walden(US), Mike Goldstein(US)
- **Surface Preparation**
  - Joel Barnett(US)
- **Thermal/Thin Films/Doping**
  - Carl Osburn(US), Hsing-Huang Tseng(US)
- **Etch**
  - Greg Smith(US), Gabe Gebara(US)
- **Stacked DRAM**
  - Jae-Sung Roh(KR)
- **Trench DRAM**
  - Wolfgang Mueller(EU)
- **Flash**
  - Mauro Alessandri(EU)
- **PCM**
  - Mauro Alessandri(EU)
- **FeRAM**
  - Jeffrey Cross(JP)



# 2007 FEP - Highlights

- **Starting Materials:**
  - FDSOI metrics start in 2010 – **colored yellow for thickness control for 2 years**
  - 450mm transition from research to development pushed to 2009
- **Surface Prep:**
  - Particle control capability unknown for particle size <27nm
  - Material loss metrics focused on post-gate formation cleaning steps
- **Thermal/Thin Films/Doping:**
  - High-k/metal gate production moved back to 2008 for HP logic (LP already there)
  - $X_j/L_{gate} \approx 0.5$ ; LSTP leakage limit increased to 30 pA/um; other model constraints
- **Etch:**
  - No change in metrics; color changes to reflect use of design restrictions
  - Physical Gate Length scaling is too aggressive – needs to be corrected in 2008
- **Stacked DRAM:**
  - Capacitor dielectric  $t_{eq}$  **red in 2012** (36nm); Cap. **aspect ratio red in 2014** (28nm)
- **Trench DRAM:**
  - Capacitor dielectric  $t_{eq}$  **red in 2014** (28nm)
- **Non-volatile memories**
  - Flash – updated STI aspect ratio metrics; discuss end of FG scaling
  - PCRAM – table metrics enhanced: heater stability, reset current density
  - FeRAM – significant changes in metrics and timing to reflect current production



# Starting Materials

## 2007 Highlights

- Updated reported front surface particle size metrics (from 90nm to 65nm in 2007 & 2008)
- Removed Fully Depleted (FD) SOI film and BOX thickness parameters through 2009 – reflecting PIDS push to 2010 – **colored yellow** due to thickness variation requirements
- Set edge exclusion to 2mm through 2008, then to 1.5mm for consistency with Factory Integration
- Revised supplier and metrology colorization to reflect updated industry capabilities
- Simplified Table notes to improve reader comprehension
- Reassessed Potential Solutions – 450mm transition from research to development pushed out to 2009
- Revised Emerging Materials details document to reflect changes since the 2005 publication
- Created two supplementary “detailed needs” documents accessible via chapter hyperlinks (Si and Metrology Reference)



# Starting Materials Ongoing Activities

- **Continue to follow industry developments related to productivity enhancements and assess relevance to Starting Materials Tables, Text and Potential Solutions**
  - 300mm “Prime” initiative
  - “More than Moore” impact
  - Potential next diameter migration (450mm)
- **Assessment of Emerging Materials for potential Table line item inclusion**
- **Revisit edge roll-off for possible Table insertion**



# Surface Preparation 2007 Highlights

- Particle metrics updated for changes in DRAM models
- Implemented “rule” to eliminate upward movement in particle metrics
- Particles **red cell** pulled into 2009 to reflect unknown capability under 27nm size
- Added indication that material loss metrics are most important after gate formation
- Watermarks metric removed from table



# Surface Preparation Ongoing Activities

- **Lack of forward-looking models**
  - impact/sensitivity of high-k/metal gates (C, O, metals, mobile ions)
  - impact/sensitivity of FDSOI, MuGFET
  - mobility-enhanced channel materials (SiGe, III-V)
- **Questions remain around particle model**
- **Lack adequate metrology for vertical surfaces**
- **High aspect ratio contact/via drying**
- **Material loss metrics controversial**
- **Backside and Bevel/Edge contamination metrics need model-based approach**



# Thermal/Thin Films/Doping

## 2007 Highlights - 1

- High-k/Metal gate pulled back to 2008 for HP and LSTP (LP already there)
- FDSOI pushed out to 2010, MuGFET pulled into 2011
- Metal gate work function tradeoffs identified
- Long term scaling of EOT to 5Å still challenging
- $X_j$  extension “Reset” to Reflect Best Value of About 13 nm in 2007, Making  $X_j/L_{gate} \approx 0.5$
- Offset Spacer (Prior to Extension Implant) is Needed to Minimize Degradation to  $I_{on}$  and CV/I Performance Requirements
- Interfacial Contact Resistivity was Assumed to “Staircase” from  $1E-7 \Omega\text{-cm}^2$  (2007-2009), to  $5E-8$  (for non-equilibrium doping from 2010-2012), to  $2E-8$  (for dual metal gates from 2013-2017), to  $1E-8$  (for even lower-barrier metals after 2018)



# Thermal/Thin Films/Doping 2007 Highlights - 2

- LSTP Leakage Allowance Increased from 10 to 30 pA/um
- FDSOI Thicknesses and Fin Widths Reduced Somewhat by PIDS to Obtain Higher Performance
- Requirement for  $V_T$  Shifts Due to Charge in the High k Dielectric Charge Changed From 10 mV to 1/3 of the Allowable Threshold Voltage Variability (ATVV), Which is 3% of  $V_{dd}$  to be Consistent with Starting Materials



# Thermal/Thin Films/Doping Ongoing Activities

- **Continue close cooperation with PIDS to monitor consistency of model projections**
- **Monitor results of gate length study for impact on model projections for 2008 ITRS update**



# Etch

## 2007 Highlights

- No changes in the metrics for gate etch bias and gate CD control
- Gate CD control color changed to **white** for 2007/2008 and to **yellow** for 2009 reflecting the implementation of design restrictions
- Atomic Layer Etching adding to potential solutions table



# Etch

## Ongoing Activities

- Complete and summarize gate length survey in order to update physical gate length roadmap in 2008 update
- Continue to monitor gate CD control issues
- Continue discussions with Design and Litho on how to reduce and share this metric
- Continue to review resist trimming and hard mask requirements with respect to pattern collapse issues



# Stacked DRAM 2007 Highlights

- 2007 Cell size factor changed from 8 to 6 according to the ORTC table
- Both of cylinder and pedestal MIM as a capacitor structure are extended until the year 2012 (36nm).
- Cylinder factor of 1.5 is applied only until the year 2008 because the pedestal structure will be more favored by the most of companies from 2009 onward.
- Capacitor details are calculated based on the PIDS projection of equivalent oxide thickness for the storage node dielectric. teq is colored red starting in 2012 (36nm)
- Storage node aspect ratio is used to give an indication of structural stability. SN A/R colored red starting in 2014 (28nm)



# Trench DRAM 2007 Highlights

- 2007 is SIS with NO dielectric – MIM with high-k dielectric starts in 2008 (1 year delay from the ITRS 2006 update)
- teq of 0.7nm changed from **yellow** to **red** in the years 2014 and 2015
- trench depth adjusted starting in 2010 - shallower



# DRAM

## Ongoing Activities

- Try to get closer coordination between Stacked and Trench roadmaps
- Add projections related to the transistors in the array and periphery



# Flash

## 2007 Highlights

- updated and separated STI aspect ratio projections for NAND and NOR
- updated dielectric requirements for tunnel and interpoly
- discuss end of floating gate structure



# PCRAM

## 2007 Highlights

- updated conformality requirements
- added row for heater stability
- added row for maximum reset current density



# FeRAM

## 2007 Highlights

- 2 year technology roll back to reflect status of industry (from conference presentation level to mass production)
- changed technology cycle from 1 to 3 years
- mixed signal devices introduced in 2007
- endurance changed to 1e14
- corresponding adjustments in specifications, materials, processing
- Table revised to reflect mass production of 0.18um FeRAM with 0.13um CMOS in 2007
- table covers both embedded and standalone



# 2007 FEP - Summary

- 450mm transition from research to development pushed to 2009
- High-k/metal gate production moved back to 2008
- FDSOI metrics start in 2010
- Multi-gate metrics start in 2011
- $X_j/L_{\text{gate}} \approx 0.5$ ; LSTP leakage limit increased to 30 pA/um; other model constraints
- design restriction implementation assumed for gate CD control
- DRAM stacked capacitor dielectric **teq red in 2012** (36nm)
- DRAM stacked capacitor **aspect ratio red in 2014** (28nm)
- DRAM trench capacitor dielectric **teq red in 2014** (28nm)
- Several updates and adjustments to non-volatile memory tables

