Interconnect Working Group

2007 Edition - draft
18 July 2007
San Francisco

Christopher Case
Linde

ITWG Regional Chairs

Japan
- Hiroshi Miyazaki
- Masayuki Hiroi

US
- Christopher Case
- Robert Geffken

Taiwan
- Douglas CH Yu

Europe
- Hans-Joachim Barth
- Alexis Farcy

Korea
- Hyeon-Deok Lee
- Sibum Kim

Partial List of Contributors

- Robert Geffken
- Hans-Joachim Barth
- Alexis Farcy
- Harold Hosack
- Paul Feeney
- Ken Monnig
- Rick Reidy
- Mauro Kobrinsky
- Hideki Shibata
- Kazuyoshi Ueno
- Michele Stucchi
- Susan Vitkavage
- Eiichi Nishimura
- Mandeep Bamal
- Quingyuan Han
- Robin Cheung
- Didier Louis
- Katsuhito Tokushige
- Masayoshi Imai
- Greg Smith
- Detlef Weber
- Scott Pozder
- Osamu Yamazaki
- Hiroshi Miyazaki
- Masayuli Hiroi
- Manabu Tsujimura
- Nohjung Kwak
- Hyeon Deok Lee
- Yuji Awano
- Kenichi Nishi
- Sibaim Kim
- Lucile Arnaud
- JD Luttmer
- Sitaram Arkalgud
- Azad Naeemi
- Dirk Gravesteijn
- NS Nagaraj
- Mike Mills
- Skip Berry
- Gunther Schindler
- Chung-Liang Chang
- Tomoji Nakamura
- Christopher Case

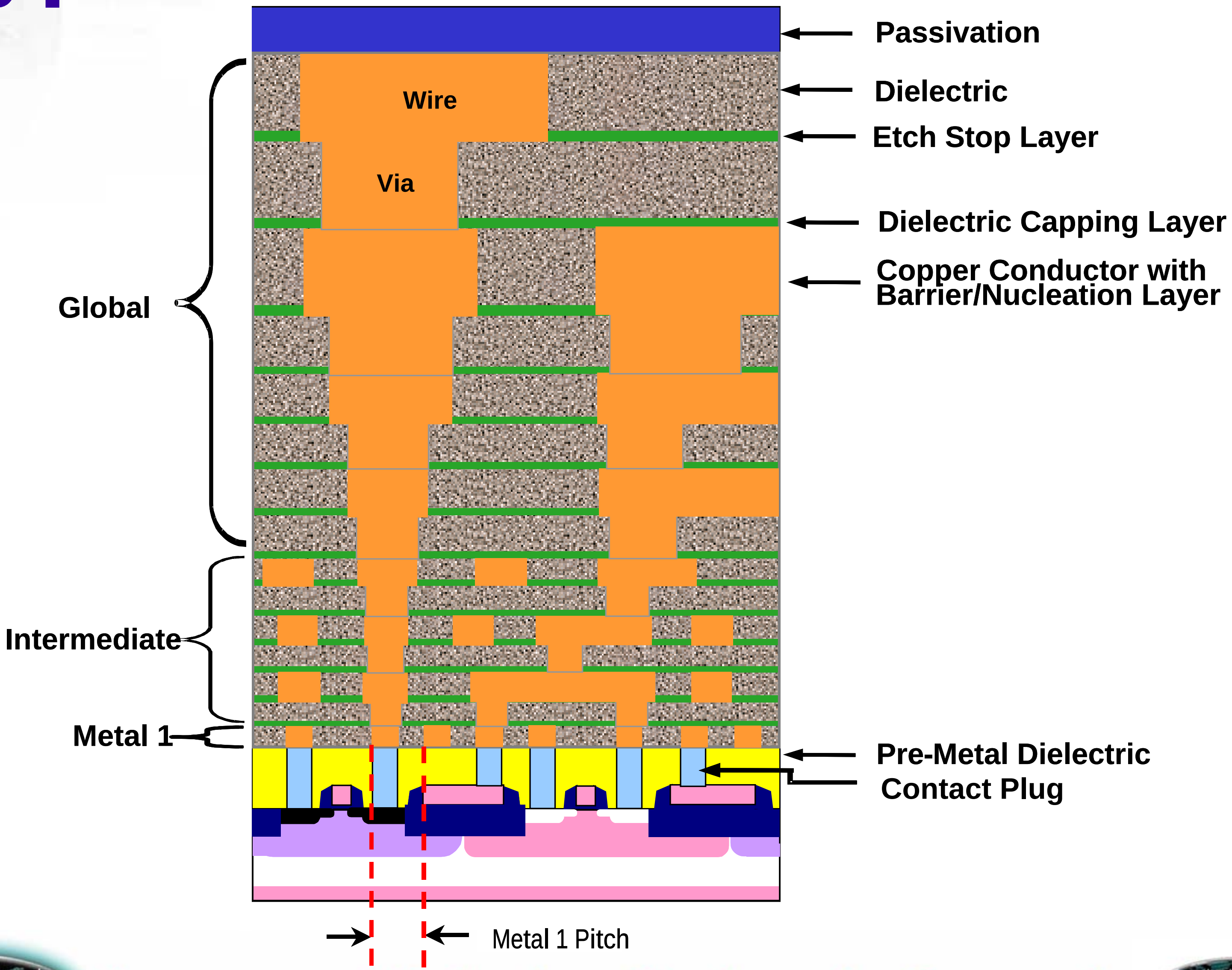
Agenda

- Scope, structure and 10 year synopsis
- Technology requirements
- Difficult challenges
- Cu resistivity effects
- Energy and performance
- Low κ roadmap
- Interconnect for memory
  - DRAM wiring roadmap
  - Non-volatile interconnect requirements
- Beyond metal/dielectric systems
  - 3D, optical and carbon nanotubes (CNT)
  - 3D roadmap proposal
- Last words

Interconnect scope

- Conductors and dielectrics
  - Starts at contact
  - Metal 1 through global levels
  - Includes the pre-metal dielectric (PMD)
- Associated planarization
- Necessary etch, strip and cleans
- Embedded passives
- Reliability and system and performance issues
- Ends at the top wiring bond pads
- “Needs” based replaced by – scaled, equivalently scaled or functional diversity drivers

Typical MPU cross section



Passivation

Dielectric

Etch Stop Layer

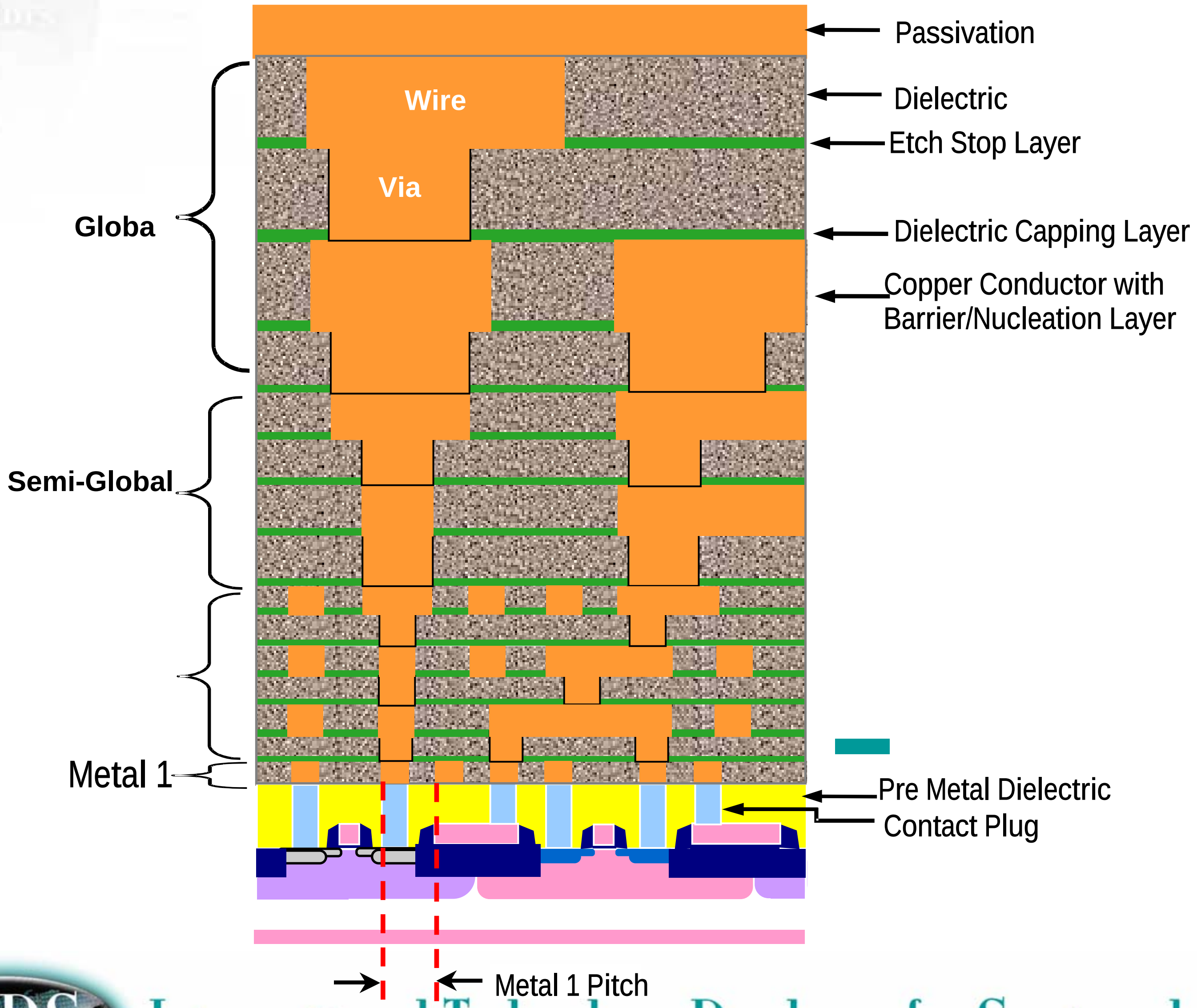
Dielectric Capping Layer

Copper Conductor with Barrier/Nucleation Layer

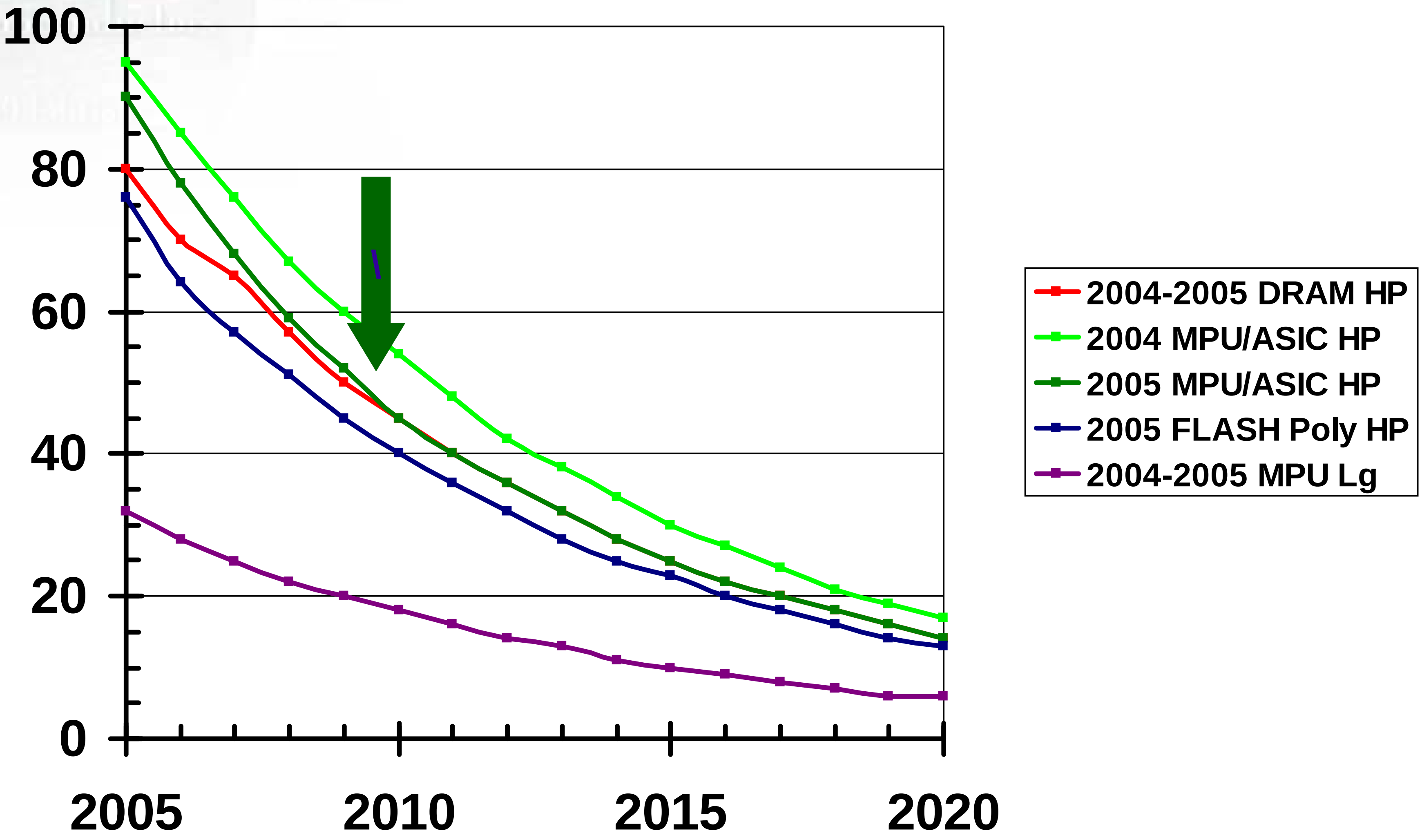
Pre-Metal Dielectric

Contact Plug

Typical ASIC Chip Cross Section



M1 Half Pitch Trends



Whose linewidth is it anyway?

- Metal 1 design rule concerns
  - Staggered contacted pitch used for definition
    - 68 nm half pitch for 2007
    - High performance MPU pitches scaling at ~0.75/2 years until 2009
    - Returning to 0.7/3 years 2010

- Convergence of MPU/ASIC and DRAM pitch in 2010
  - Commonality in the backend (Cu based)

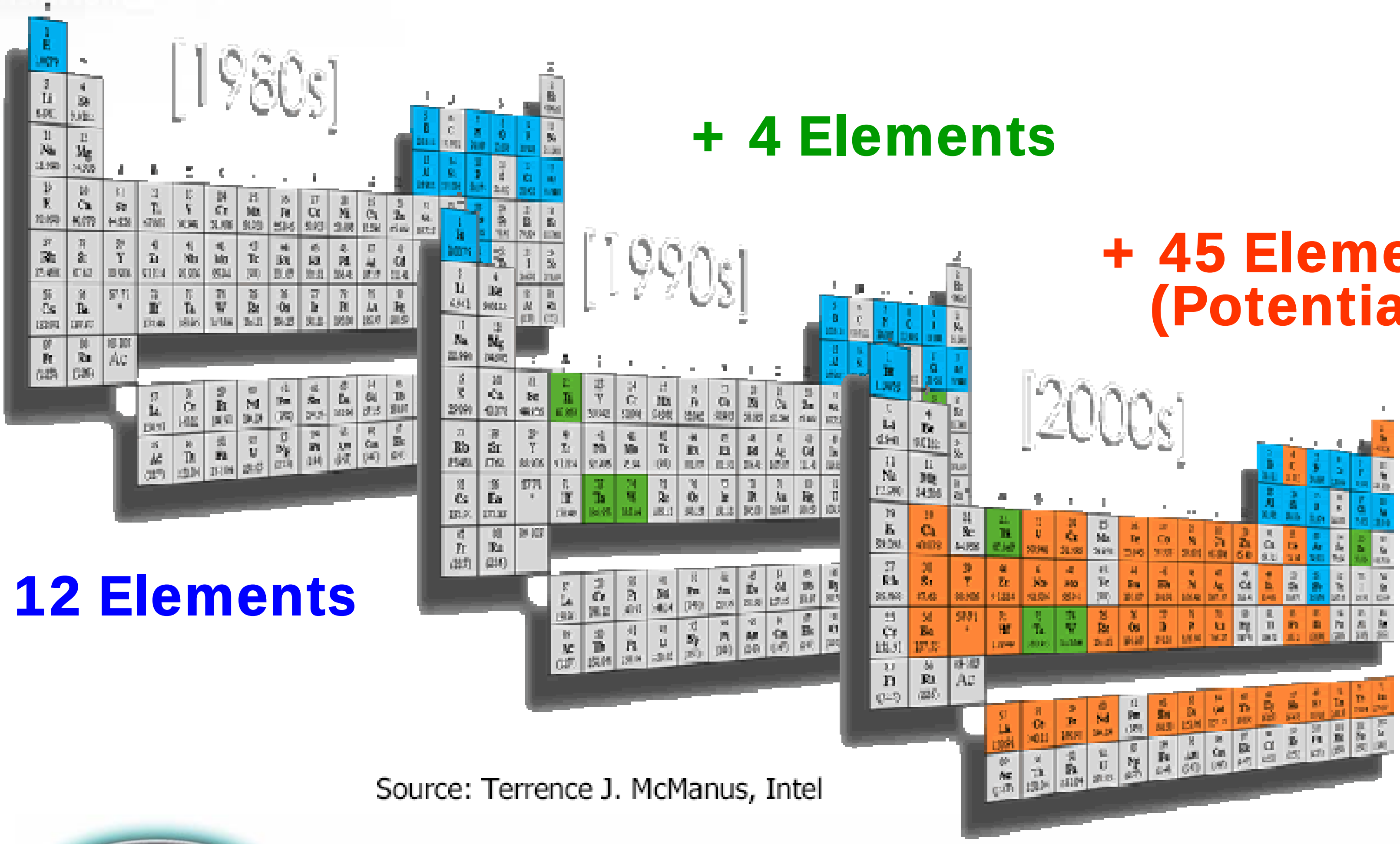
Technology Requirements

- Tables for HP MPU and ASIC plus DRAM
- Wiring levels including “optional levels”
- Reliability metrics
- Minimum wiring/via pitches by level
- Performance figure of merit and capacitance
- Planarization requirements
- Conductor resistivity with and without scattering
- Barrier thickness
- Dielectric metrics including effective k (UPDATED)
- Crosstalk metric
- Metal 1 variability due to CD and scattering
- Power Index

Technology Requirements

- HP MPU and DRAM tables now restated and organized as
  - **General requirements**
    - Resistivity
    - Dielectric constant
    - Metal levels
    - Reliability metrics
    - Power metric
  - **Level specific requirements** (M1, intermediate, global)
    - Geometrical
      - Via size and aspect ratio
      - Barrier/cladding thickness
      - Planarization specs
      - Variability
    - Materials requirements
      - Conductor effective resistivity and scattering effects
    - Electrical characteristics
      - Delay, capacitance, Jmax

The March of Materials



12 Elements

+ 4 Elements

+ 45 Elements
(Potential)

Source: Terrence J. McManus, Intel

Difficult challenges (1 of 3)

- *Meeting the requirements of **scaled** metal/dielectric systems*
  - Managing RC delay and power
    - New dielectrics (including air gap)
    - Controlling conductivity (liners and scattering)
  - Filling small features
    - Liners
    - Conductor deposition
  - Reliability
    - Electrical and thermo-mechanical
- Engineering a manufacturable interconnect stack compatible with new materials and processes
  - Defects
  - Metrology
  - Variability

Difficult challenges (2 of 3)

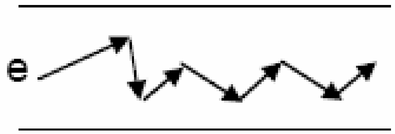
- *Meeting the requirements with **equivalent scaling***
  - Interconnect design and architecture (includes mulit-core benefits)
  - Alternative metal/dielectric assemblies
    - 3D with TSV
  - Interconnects beyond metal/dielectrics
    - 3D
    - Optical wiring
    - CNT
  - Reliability
    - Electrical and thermo-mechanical
- Engineering a CMOS-compatible manufacturable interconnect system
  - Non-traditional materials (for optical, CNT etc.)
  - Unique metrology (alignment, chirality measurements, turning radius etc)

Difficult challenges (3 of 3)

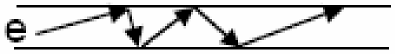
- *Adding **functional diversity***
  - Mixed technologies
    - Si, GaAs, HgCdTe together
  - Mixed signalling approaches
    - Rf
    - Passive devices
  - *Intelligent Interconnect* (active devices, sensors, MEMS, biochips, fluidics, etc. in interconnect)
    - Repeaters in interconnect, combined metallic/semiconducting CNT interconnects
    - Back-end memory
    - Variable resistor via
  - Reliability
    - Electrical and thermo-mechanical
- Engineering a CMOS-compatible manufacturable interconnect system
  - Non-traditional materials III/V, II/VI
  - Deposition (low temperature epi)
  - Unique metrology (composition)

Size matters

- 2003 – the impending impact of Cu resistivity increases at reduced feature sizes (due to scattering) - first noted
- 2004 – metrics introduced to highlight the impact of width dependent scattering on the effective resistivity and impact on RC delay
  - Models have been refined to more accurately predict the resistivity due to changes in aspect ratio, shape and metal thickness
- 2007 - Metrics updated – managed architecture
- Adapt the same methodology for DRAM when Cu is introduced (2007)



Bulk scattering



Surface scattering

Size matters

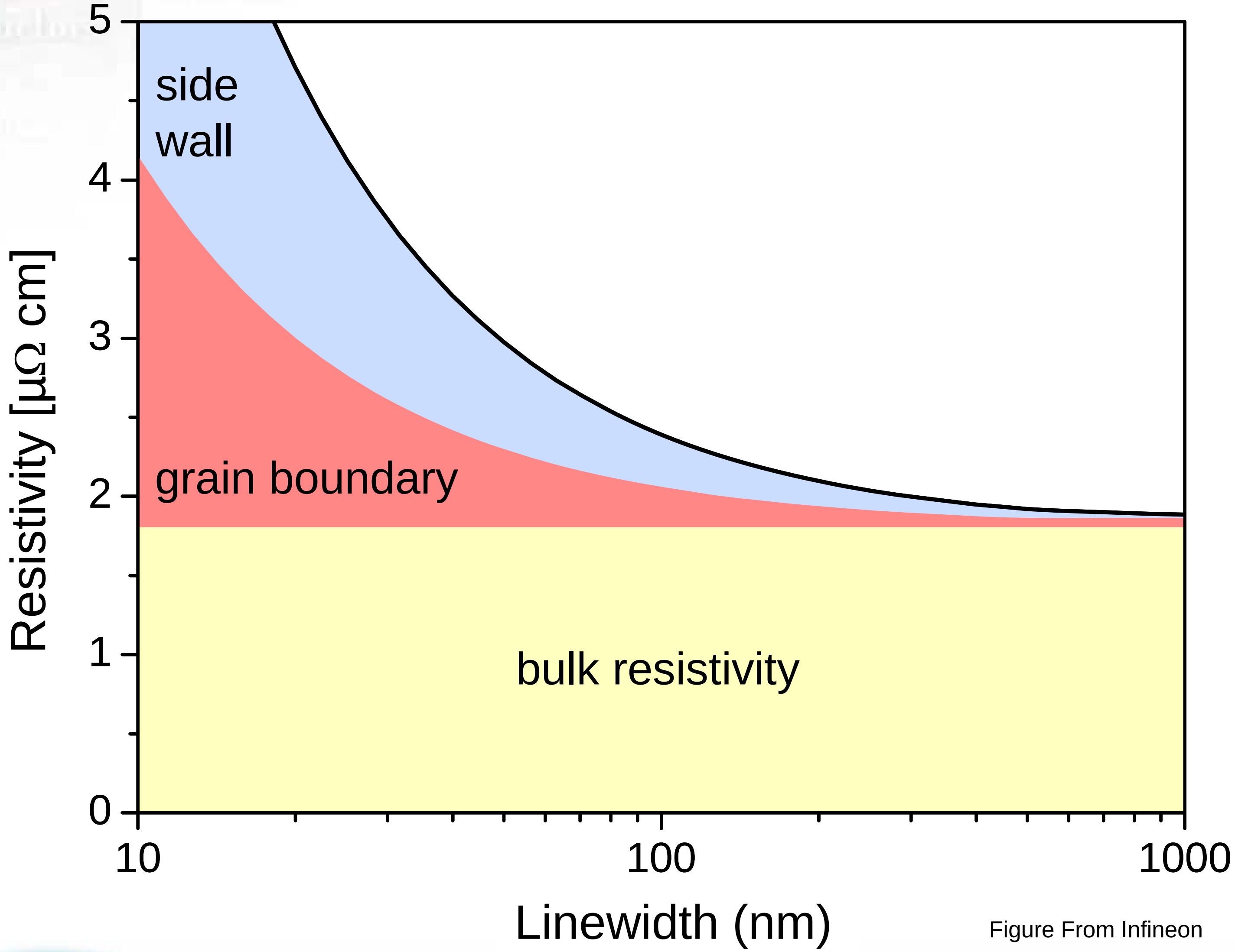
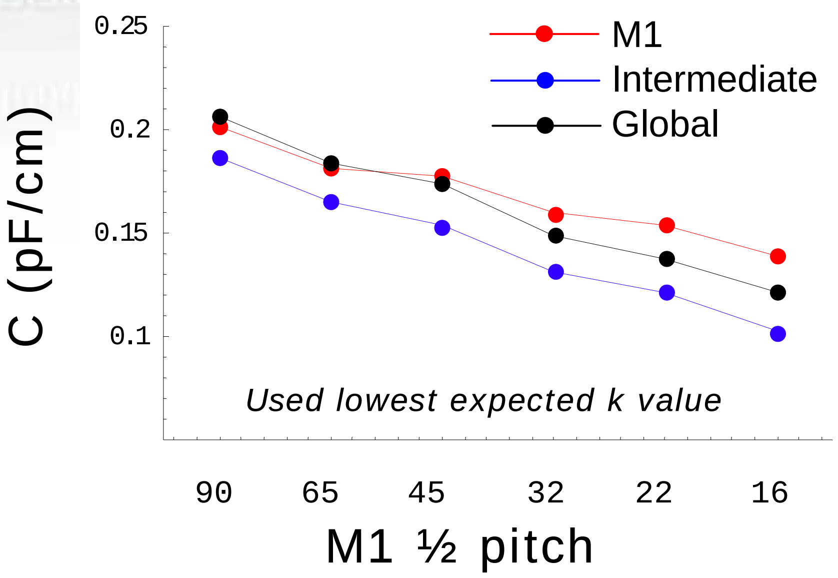


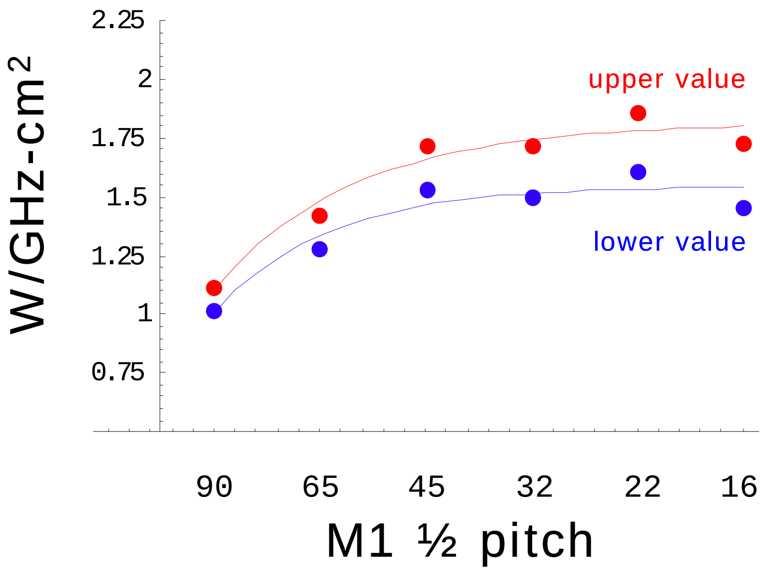
Figure From Infineon

Dynamic Power

- Increasing concern about rising dynamic power in the interconnect stack
  - Interconnects make a significant contribution to total dynamic power
- Impacts effective k roadmap
  - Drives reduction in parasitic capacitance
- Dynamic power is a key constraint for high performance MPUs
- Alternative interconnect technologies (optical, CNT, RF, etc.) should be performance competitive in terms of delay and power
- Influence of number of functions (N), activity (A) and frequency (F): $P = (NAF)CV^2$

Capacitance and Power Index



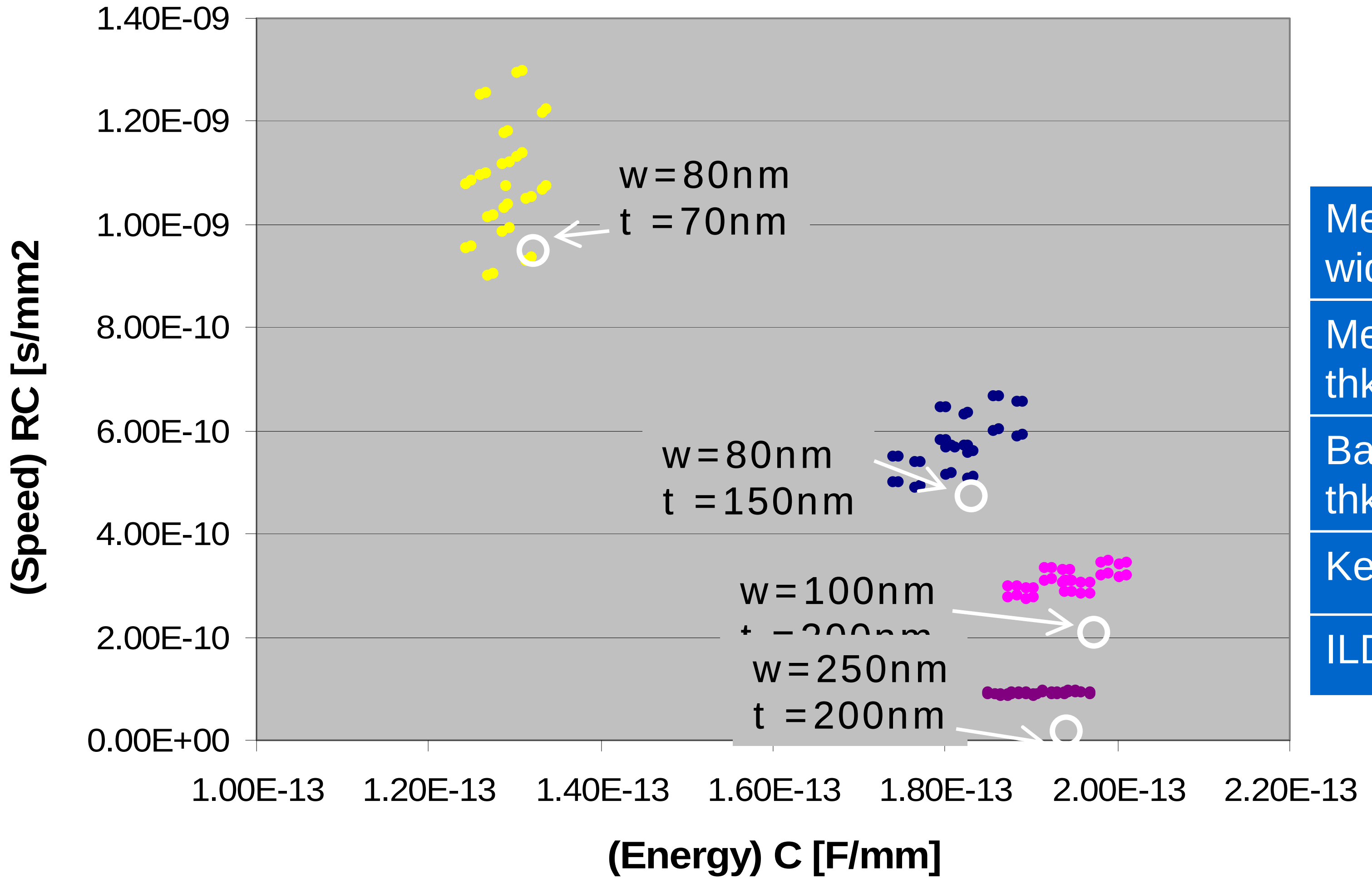


$$P_{layer}\left[\frac{W}{GHz-cm^2}\right] = C \cdot V^2 \cdot a \cdot (1\,GHz) \cdot \left(e_w \cdot \frac{1\,cm^2}{\mathrm{p}}\right) = \text{Power per GHz per cm}^2 \text{ of metal layer.}$$

C = capacitance per unit length.

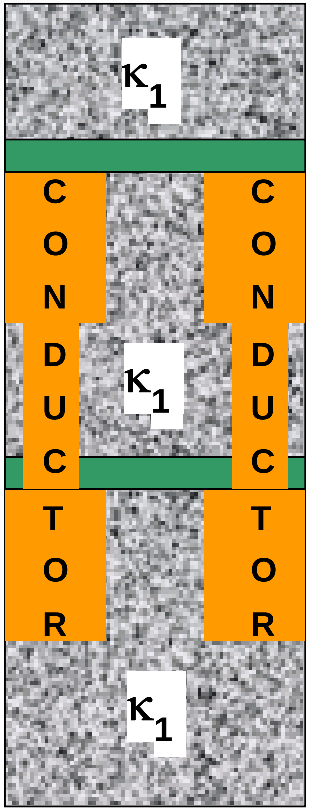
$V = V_{dd}$, p = pitch, e_w = wiring efficiency, a = average activity factor of interconnects.

R and C variability

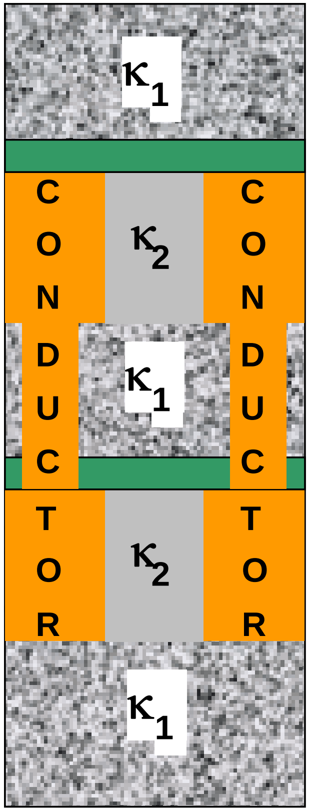


Metal width	± 6nm
Metal thk	± 4nm
Barrier thk	± 2nm
Keff	± 0.1
ILD thk	± 4nm

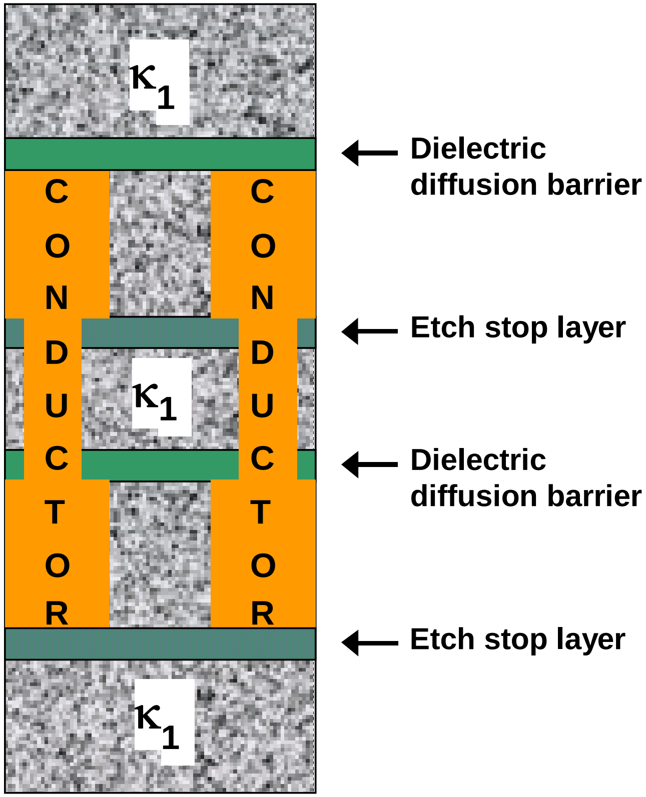
Integration Schemes



Homogeneous ILD
without trench etch stop



Embedded low κ ILD
($\kappa_1 > \kappa_2$)



Dielectric diffusion barrier

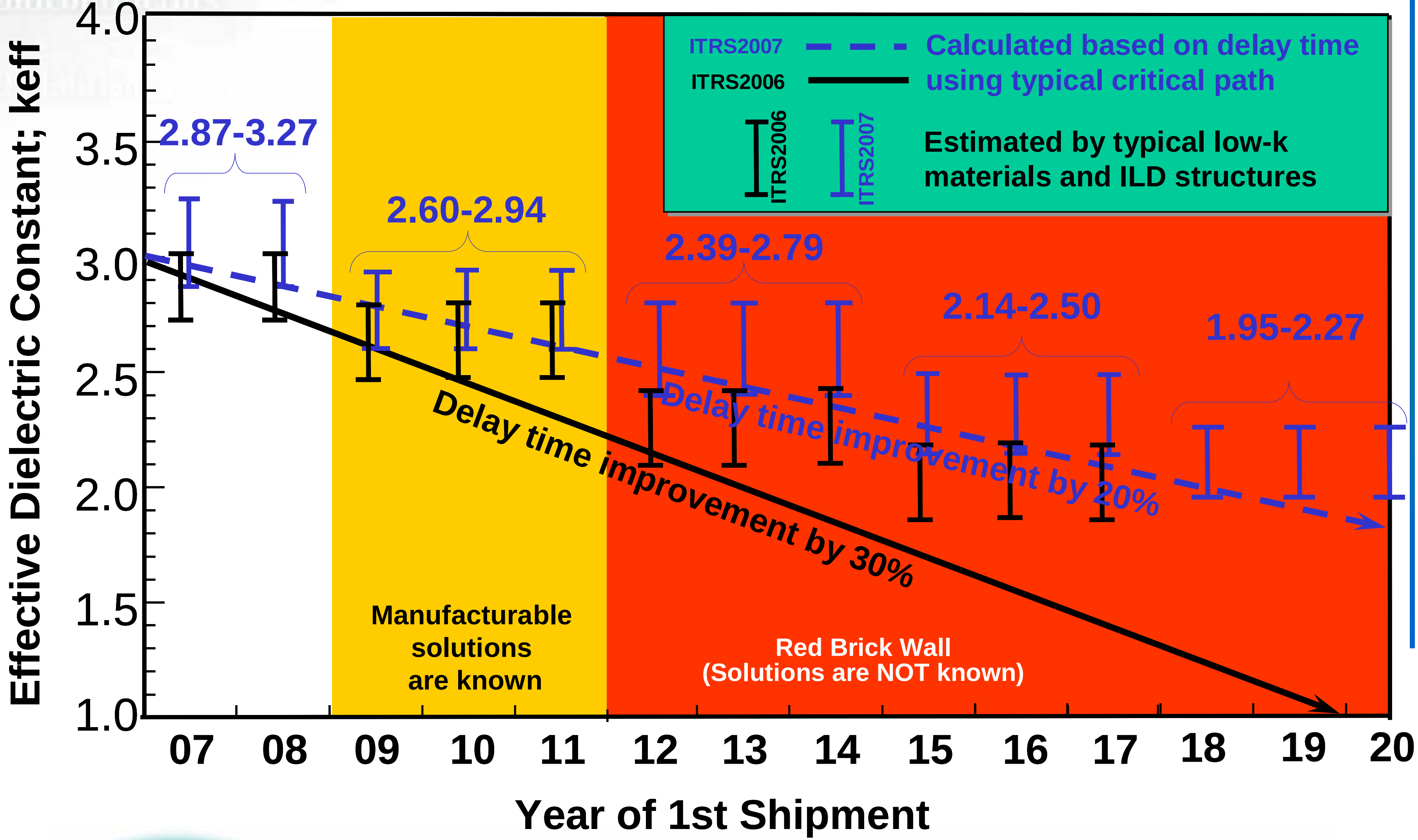
Etch stop layer

Dielectric diffusion barrier

Etch stop layer

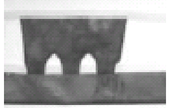
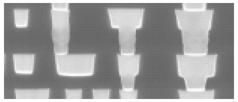
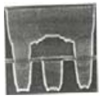
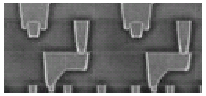
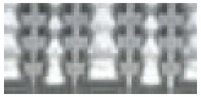
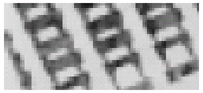
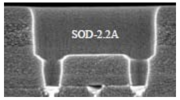
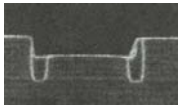
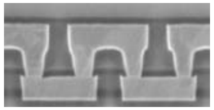
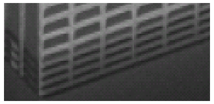
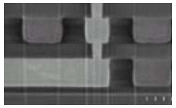
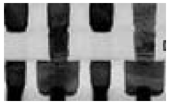
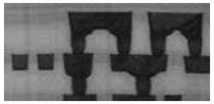
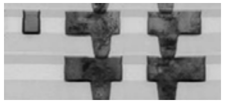
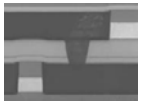
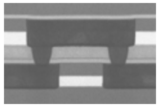
Homogeneous ILD
with trench etch stop

Low-k update



Effective Dielectric Constant; keff
4.0
3.5
3.0
2.5
2.0
1.5
1.0
07
08
09
10
11
12
13
14
15
16
17
18
19
20
Year of 1st Shipment
ITRS2007
ITRS2006
Calculated based on delay time using typical critical path
ITRS2006
ITRS2007
Estimated by typical low-k materials and ILD structures
2.87-3.27
2.60-2.94
2.39-2.79
2.14-2.50
1.95-2.27
Delay time improvement by 30%
Delay time improvement by 20%
Manufacturable solutions are known
Red Brick Wall (Solutions are NOT known)

Low-k Trend (2003-2006 IITC, IEDM, VL, AMC)

	90 nm(2005-)	65 nm(2007-)	45 nm(2010-)	32nm(2012-)
Intel	 CVD SiOC DD (k=2.9)	 CVD SiOC DD (k=2.9)	– CVD SiOC DD (k=2.6)?	– CVD SiOC DD (k=2.4)?
IBM	 CVD SiOC DD (k=3.0)	 CVD SiOC DD (k=2.75)	– CVD SiOC DD (k=2.45)	– CVD SiOC DD (k=2.2-2.4)?
TSMC	 CVD SiOC DD (k=3.0)	 CVD SiOC DD (k=2.5)	 CVD SiOC hybrid DD (k=2.2/2.5)	– CVD SiOC hybrid DD (k=2.2/2.5)?
Renesas	 CVD SiOC DD (k=2.9)	 CVD SiOC stack DD (k=2.6/3.0)	 CVD SiOC DD (k=2.65)	– CVD SiOC DD (k=2.4)?
Fujitsu	 CVD SiOC DD (k=2.9)	 NCS/CVD SiOC stack DD (k=2.25/2.9)	 NCS/NCS stack DD (k=2.25/2.25)	– NCS/NCS stack DD (k=2.25/2.25)?
TOSHIBA SONY NECEL	 CVD SiOC DD (k=2.9)	 PAr/SiOC hybrid DD (k=2.6/2.5)	 P-PAr/p-SiOC hybrid DD (k=2.3/2.3)	 ULK-PAr/SiOC hybrid DD (k=2.0/2.0)

Slow down of low-k technology development speed and large variation of k values among device companies

Low-k Roadmap Table Update

		Near-term						
	Year of Production	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*
Was	Interlevel metal insulator – effective dielectric constant (κ)	**2.7-3.0**	**2.7-3.0**	**2.5-2.8**	**2.5-2.8**	**2.5-2.8**	**2.1-2.4**	**2.1-2.4**
Is	Interlevel metal insulator – effective dielectric constant (κ)	**2.9-3.3**	**2.9-3.3**	**2.6-2.9**	**2.6-2.9**	**2.6-2.9**	**2.4-2.8**	**2.4-2.8**
Was	Interlevel metal insulator – bulk dielectric constant (κ)	**2.3-2.7**	**2.3-2.7**	**2.1-2.4**	**2.1-2.4**	**2.1-2.4**	**1.8-2.1**	**1.8-2.1**
Is	Interlevel metal insulator – bulk dielectric constant (κ)	**2.5-2.9**	**2.5-2.9**	**2.3-2.7**	**2.3-2.7**	**2.3-2.7**	**2.1-2.5**	**2.1-2.5**
New	Copper diffusion barrier and etch-stopper - bulk dielectric constant (κ)	**4.0-4.5**	**4.0-4.5**	**3.5-4.0**	**3.5-4.0**	**3.5-4.0**	**3.0-3.5**	**3.0-3.5**

Long-term									
2014	*2015*	*2016*	*2017*	*2018*	*2019*	*2020*	*2021*	*2022*	*2023*
2.1-2.4	**1.9-2.2**	**1.9-2.2**	**1.9-2.2**	**1.6-1.9**	**1.6-1.9**	**1.6-1.9**			
2.4-2.8	**2.1-2.5**	**2.1-2.5**	**2.1-2.5**	**2.0-2.3**	**2.0-2.3**	**2.0-2.3**	**1.7-2.0**	**1.7-2.0**	**1.7-2.0**
1.8-2.1	**1.6-1.9**	**1.6-1.9**	**1.6-1.9**	**1.4-1.7**	**1.4-1.7**	**1.4-1.7**			
2.1-2.5	**1.9-2.3**	**1.9-2.3**	**1.9-2.3**	**1.7-2.1**	**1.7-2.1**	**1.7-2.1**	**1.5-1.9**	**1.5-1.9**	**1.5-1.9**
3.0-3.5	**2.6-3.0**	**2.6-3.0**	**2.6-3.0**	**2.4-2.6**	**2.4-2.6**	**2.4-2.6**	**2.1-2.4**	**2.1-2.4**	**2.1-2.4**

Manufacturable solutions exist, and are being optimized	⬜
Manufacturable solutions are known	🟨
Interim solutions are known	◆
Manufacturable solutions are NOT known	🟥

DRAM

Small changes in specific via and contact resistivity

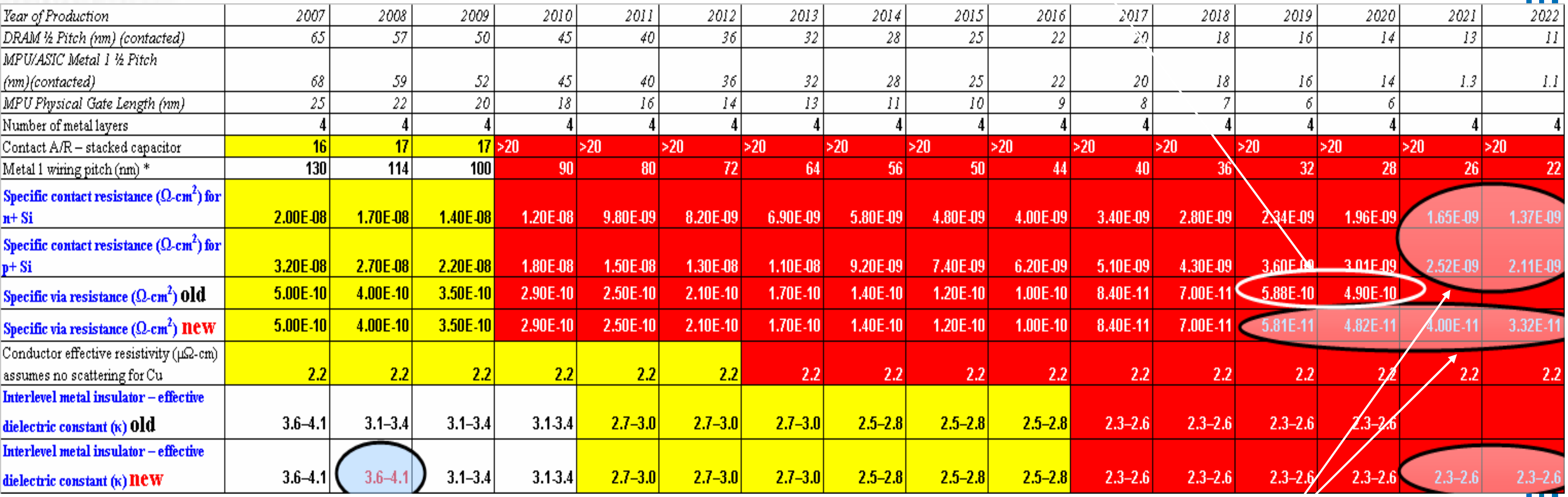
Contact A/R (stacked capacitor) rises to >20 in 2010 - a nearby red challenge - associated with the 45 nm DRAM half pitch

Cu implemented in 2007

Low k with an effective dielectric constant of 3.1 – 3.4 pushed back one year to 2009

Plan to distinguish embedded, flash, and traditional DRAM along with alternative memory in the interconnect in the future (2009)

2007 DRAM Table - n+Si, p+Si and Via

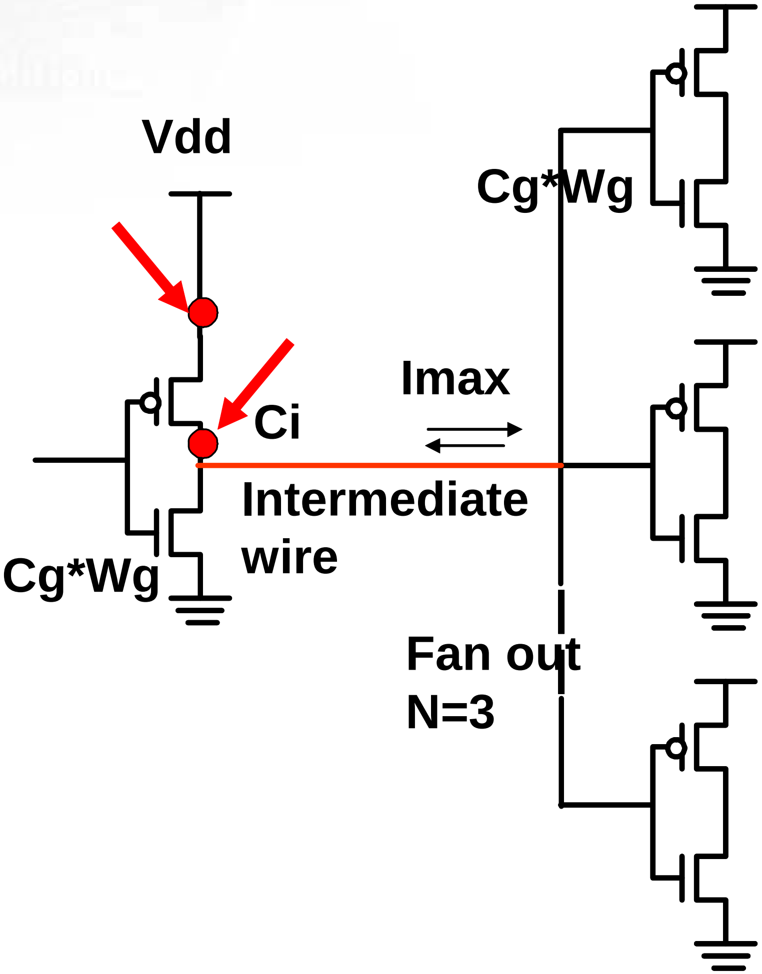


Year of Production	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*	*2014*	*2015*	*2016*	*2017*	*2018*	*2019*	*2020*	*2021*	*2022*
DRAM ½ Pitch (nm) (contacted)	65	57	50	45	40	36	32	28	25	22	20	18	16	14	13	11
MPU/ASIC Metal 1 ½ Pitch (nm)(contacted)	68	59	52	45	40	36	32	28	25	22	20	18	16	14	1.3	1.1
MPU Physical Gate Length (nm)	25	22	20	18	16	14	13	11	10	9	8	7	6	6		
Number of metal layers	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4
Contact A/R – stacked capacitor	16	17	17	>20	>20	>20	>20	>20	>20	>20	>20	>20	>20	>20	>20	>20
Metal 1 wiring pitch (nm) *	130	114	100	90	80	72	64	56	50	44	40	36	32	28	26	22
Specific contact resistance (Ω-cm^2) for n+ Si	2.00E-08	1.70E-08	1.40E-08	1.20E-08	9.80E-09	8.20E-09	6.90E-09	5.80E-09	4.80E-09	4.00E-09	3.40E-09	2.80E-09	2.34E-09	1.96E-09	1.65E-09	1.37E-09
Specific contact resistance (Ω-cm^2) for p+ Si	3.20E-08	2.70E-08	2.20E-08	1.80E-08	1.50E-08	1.30E-08	1.10E-08	9.20E-09	7.40E-09	6.20E-09	5.10E-09	4.30E-09	3.60E-09	3.01E-09	2.52E-09	2.11E-09
Specific via resistance (Ω-cm^2) **old**	5.00E-10	4.00E-10	3.50E-10	2.90E-10	2.50E-10	2.10E-10	1.70E-10	1.40E-10	1.20E-10	1.00E-10	8.40E-11	7.00E-11	5.88E-10	4.90E-10		
Specific via resistance (Ω-cm^2) **new**	5.00E-10	4.00E-10	3.50E-10	2.90E-10	2.50E-10	2.10E-10	1.70E-10	1.40E-10	1.20E-10	1.00E-10	8.40E-11	7.00E-11	5.81E-11	4.82E-11	4.00E-11	3.32E-11
Conductor effective resistivity (µΩ-cm) assumes no scattering for Cu	2.2	2.2	2.2	2.2	2.2	2.2	2.2	2.2	2.2	2.2	2.2	2.2	2.2	2.2	2.2	2.2
Interlevel metal insulator – effective dielectric constant (κ) **old**	3.6–4.1	3.1–3.4	3.1–3.4	3.1-3.4	2.7–3.0	2.7–3.0	2.7–3.0	2.5–2.8	2.5–2.8	2.5–2.8	2.3–2.6	2.3–2.6	2.3–2.6	2.3–2.6		
Interlevel metal insulator – effective dielectric constant (κ) **new**	3.6–4.1	3.6–4.1	3.1–3.4	3.1-3.4	2.7–3.0	2.7–3.0	2.7–3.0	2.5–2.8	2.5–2.8	2.5–2.8	2.3–2.6	2.3–2.6	2.3–2.6	2.3–2.6	2.3–2.6	2.3–2.6

Calculated values by using the scaling factor of 0.83

1. Values for Contact and Vias are basically consistent with measured data up to 2009
2. Beyond 2009 the values are extrapolated as proposed previously by Japan TWG:
Based on contact CD scaling assumption, 30 % every 2 years (factor = 0,83/year) is between compensation of width scaling (factor = 0,89/year) and area scaling (factor = 0,79/year); 30 % every 2 years is a good approach to keep the contact Rs below a certain limit.
3. Values 2010 to 2022 should stay in red

Jmax 2007 – small changes



Inverter circuit (F.O=3)

-Minimum Tr width (Wmin.):
  NMOS Gate width= (ASIC Half-pitch)x 4
  PMOS Gate width=(NMOS Gate-width) x 2

-Tr-width (Wg):
  Wg =Wmin.x 8

-Gate capacitance(Cg)

-Wiring length (Li): IM-Pitch x 200

-Wiring capacitance(Ci): Updated keff

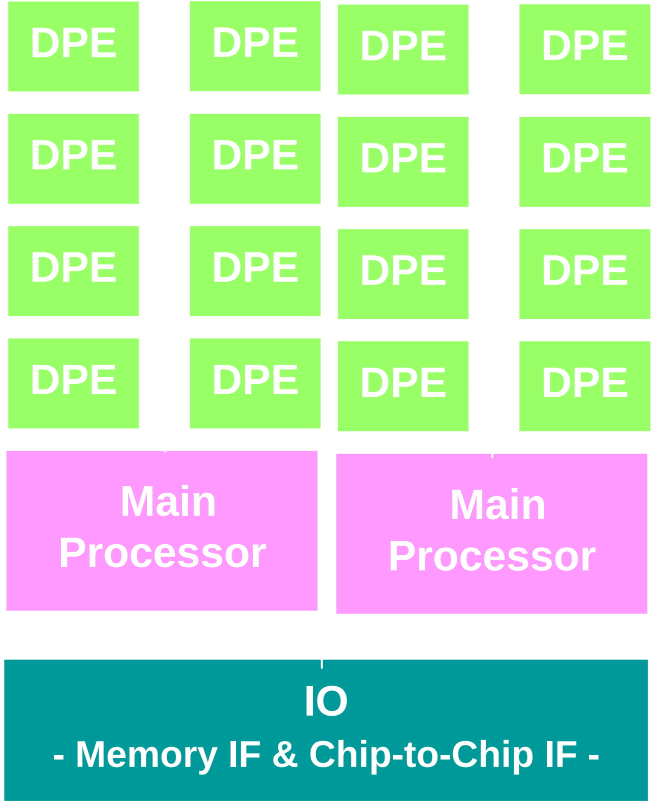
Average current density of IM-interconnect （J_{max}）

= f (Cg*Wg *N+Ci) *Vdd/(Wi*Ti)

Multi-core Impact on Interconnect

- Wiring lengths change
  - Critical path reduced (in core)
  - Mechanical integrity challenges will change
  - Jmax changes
  - Hierarchical structure may no longer be necessary
    - Converge to more fine pitch local/intermediate wires
    - Power and ground delivered through grid
  - Global delay challenge relaxed
  - 3D may include multi-core

- Need to consider splitting metrics into:
  - In-core (intra-tile) and Inter-core (inter-tile)
    - New bandwidth requirements



DPE DPE DPE DPE

DPE DPE DPE DPE

DPE DPE DPE DPE

DPE DPE DPE DPE

Main Processor

Main Processor

IO

- Memory IF & Chip-to-Chip IF -

Figure From ITRS 2006 Design TWG

Emerging Interconnect

- Use geometry
  - 3D
  - Air gap
- Use different signaling methods
  - Signal design
  - Signal coding techniques
- Use innovative design and package options
  - Interconnect - centric design
  - Package intermediated interconnect
  - Chip-package co-design

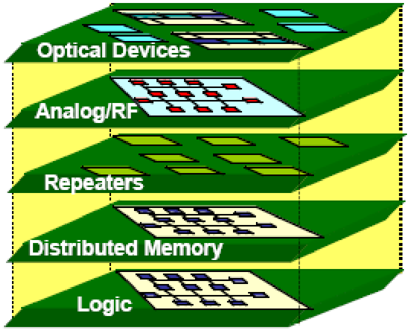
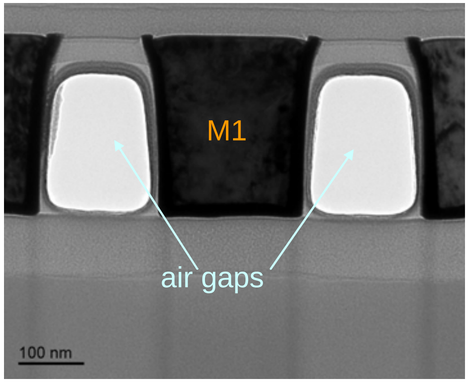
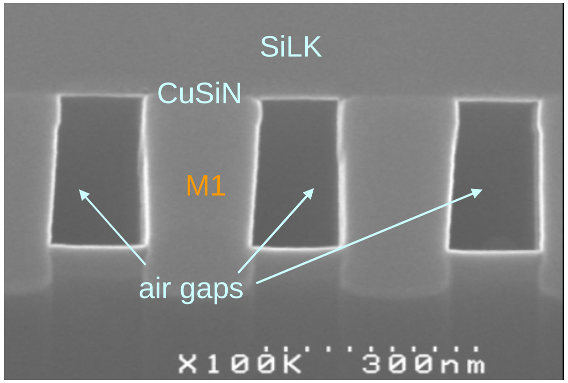


Figure From Stanford

From low κ to no κ - air gaps

- Introduction of air gap architectures
  - Creation of air gaps with non-conformal deposition
  - Removal of sacrificial materials after multi-level interconnects





⇒ Values of effective k-value down to 1.7 with low crosstalk levels

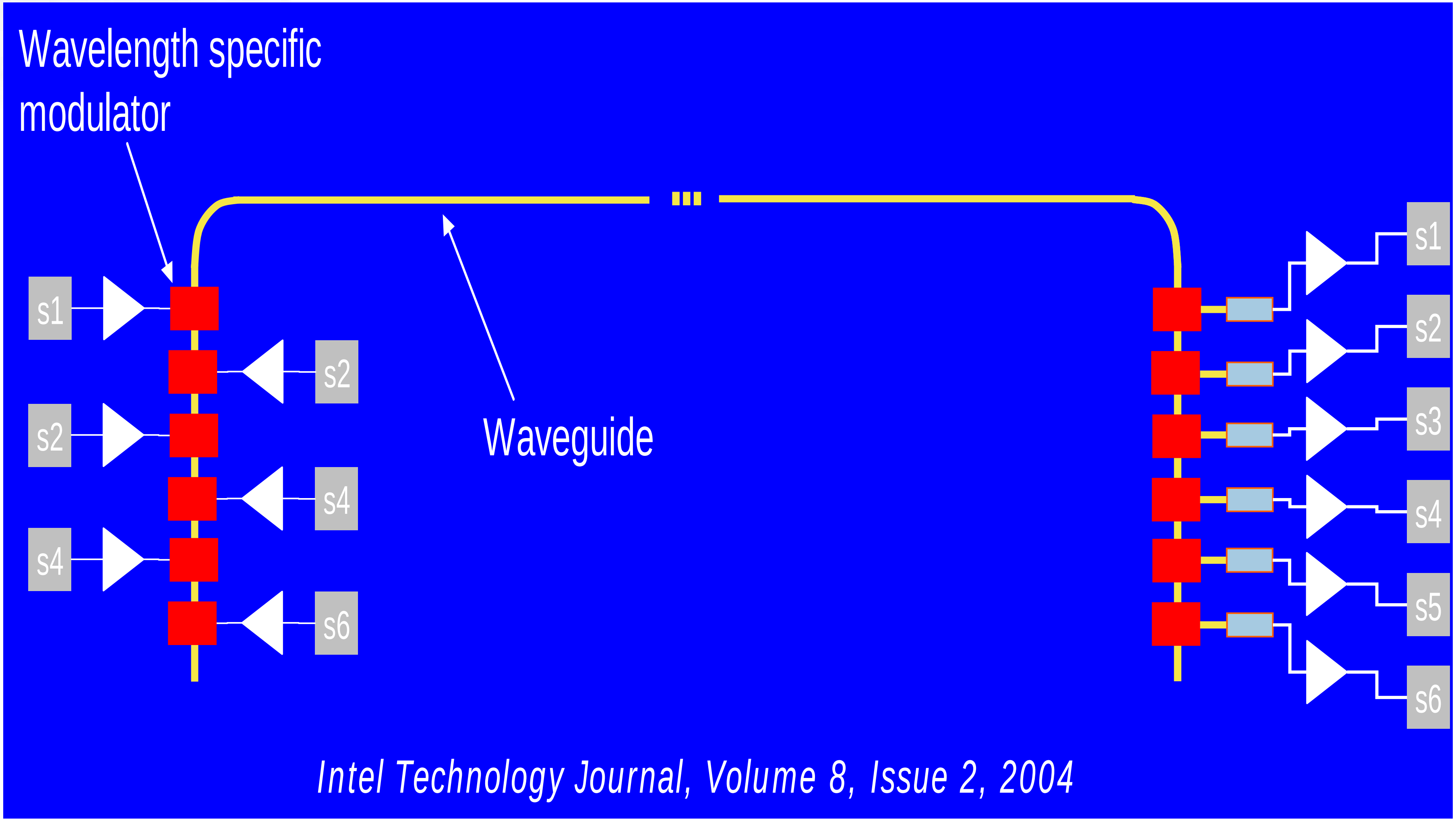
⇒ Localized air gaps to maintain good thermal and mechanical properties

Ultra-low κ and Air gap (κ<1.7) (CVD and Spin-on)

Emerging interconnect

- Use different physics
  - Optics (waveguides, emitters, detectors, free space, trans-impedance amps, modulators)
  - RF/microwaves (transmitters, receivers, free space, waveguides)
  - Terahertz photonics
- Radical solutions
  - Nanowires/nanotubes
  - Molecules
  - Spintronics
  - Quantum wave functions

Hypothetical On-die Optical Interconnects with WDM

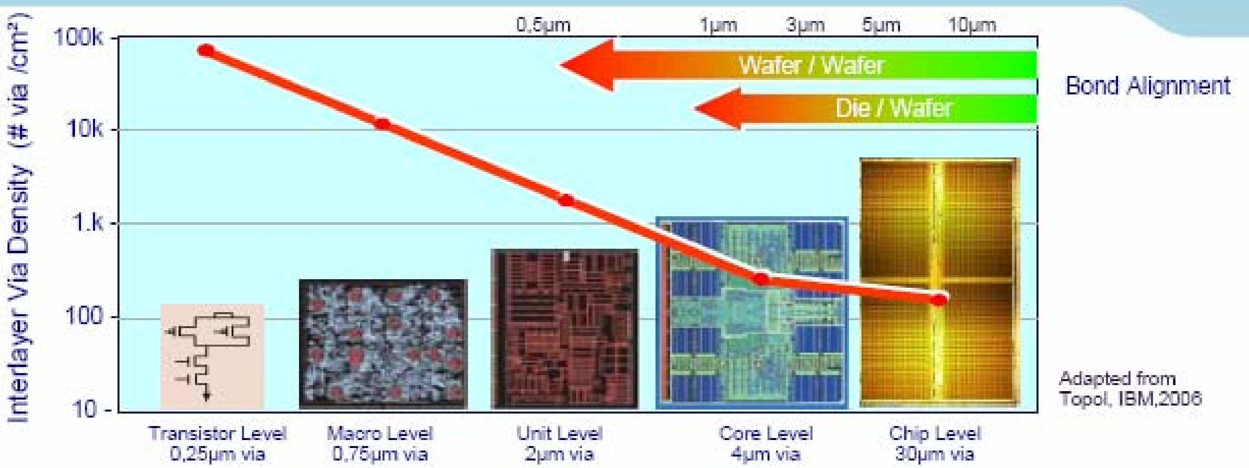


Intel Technology Journal, Volume 8, Issue 2, 2004

High Density 3D Integration

- Through silicon via (TSV)
  - Reliability
  - Physical metrics (pitch, diameter, density)
- Alignment tolerance
- Bond layer
  - Reliability
  - Interfacial defect density
  - Adhesion
- List of “Difficult Challenges”, e.g. TSV processes, alignment, low k impact on TSV, etc.

The Introduction of Thru-Si-Stacking (TSV)



Adapted from
Topol, IBM,2006

Architecture	Via Size	Via Process	Chip/Via Connection	Stacking Type	1st Application	
Standard Chip Architecture	Large,(~ 20µm) ~ 10...100/chip	Post Front-End	On Chip RDL	Die / Die Die / Wafer	Flash	Phase 1
First 3D Elements	Medium,(< 5µm) ~ 200...1000/chip	Pre /In /Post Front-End	Integrated in Me layers	Die / Wafer Wafer / Wafer	DRAM, Sensors	Phase 2
Complete 3D Design	Fine,(< 1µm) ~ 1k...100k/chip	Pre /In Front-End	Integrated In Me layers	Wafer / Wafer	???	Phase 3

The 3D Thru-Si-Via Stacking Technology will be introduced stepwise to be beneficial

Summary of Notable 2007 changes

- Low-k slowdown
  - New range for bulk k and k_{eff}
- New Technology Introduction
  - ALD barrier processes and metal capping layers for Cu are lagging in introduction.
- No solutions seen for Cu resistivity rise
- Power Metric
  - Capacitance per unit length decreases due to decreases of the dielectric constant.
  - However, the dynamic power is expected to increase because of the increased number of metallization layer, larger chip size and increased frequency.

Last words

- Must manage the power envelope
- Must continue to meet requirements of scaled metal/dielectric systems while developing CMOS-compatible equivalent scaling solutions
  - Cu resistivity impact real but manageable
  - materials solutions alone cannot deliver performance - end of traditional scaling
  - integrated system approach required
- Functional diversity enhances value