

# **ITRS Roadmap Design + System Drivers**

**San Francisco, July 2007**

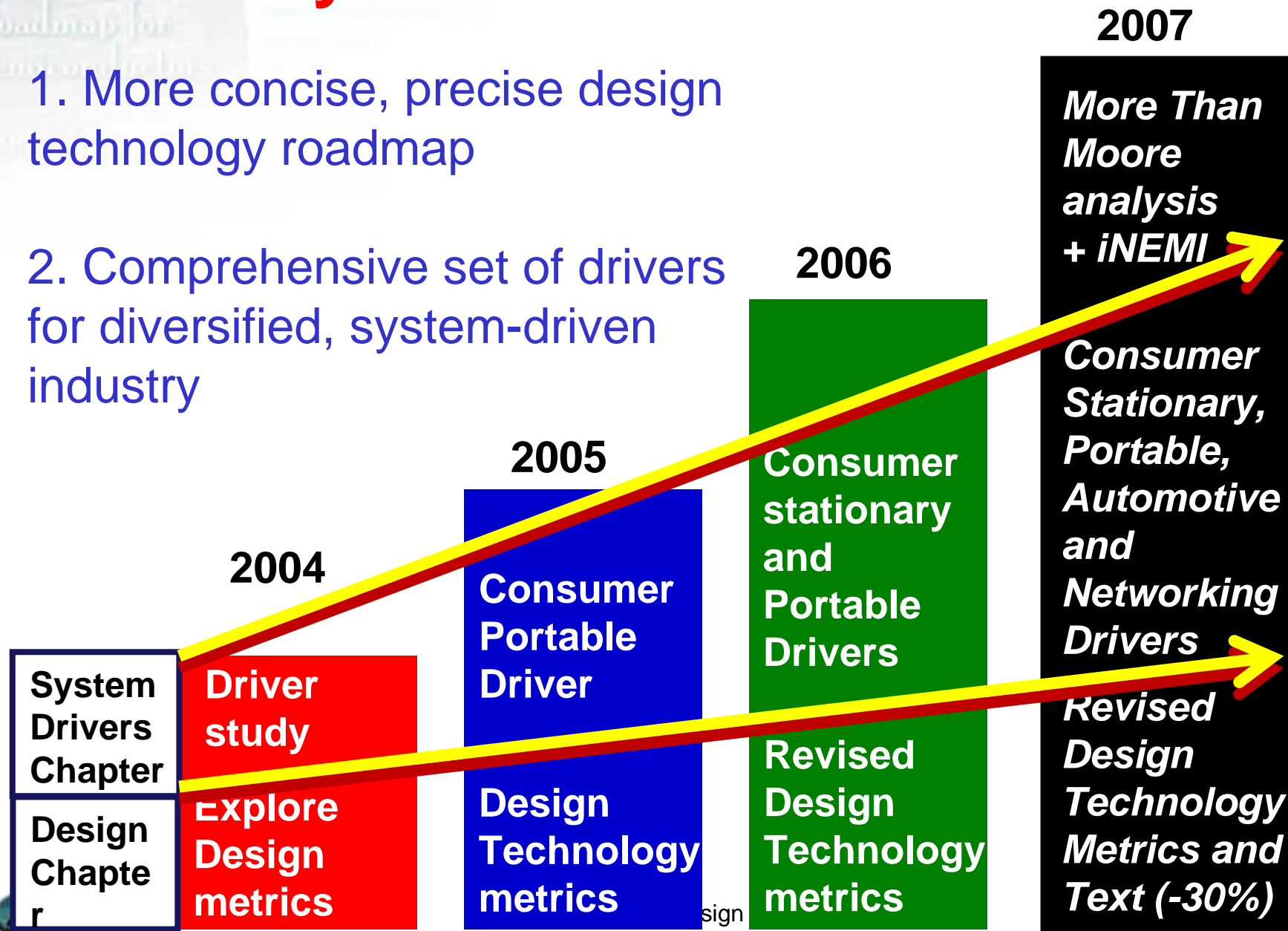
**Worldwide Design TWG**

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# Summary

1. More concise, precise design technology roadmap
2. Comprehensive set of drivers for diversified, system-driven industry



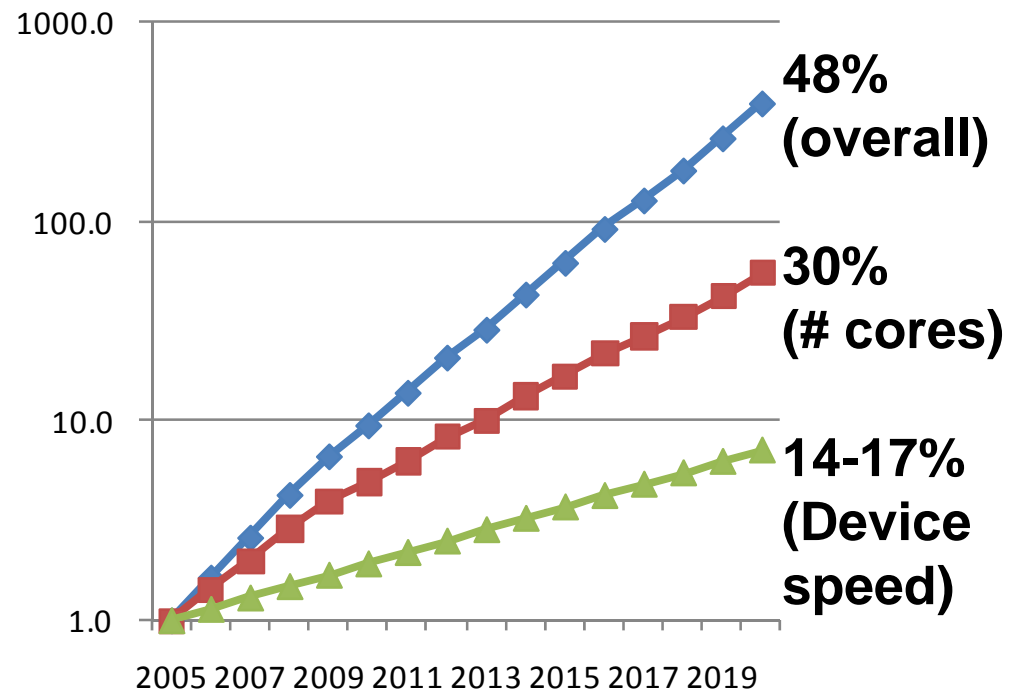
# Design-Driven Semiconductor Innovation (Moore+)

**Domain / market independent**  
*Inventory 50+ Design Solutions*

**Domain / market dependent**  
*(Consumer) driver architecture*



- Moore
- More Moore
- More Than Moore



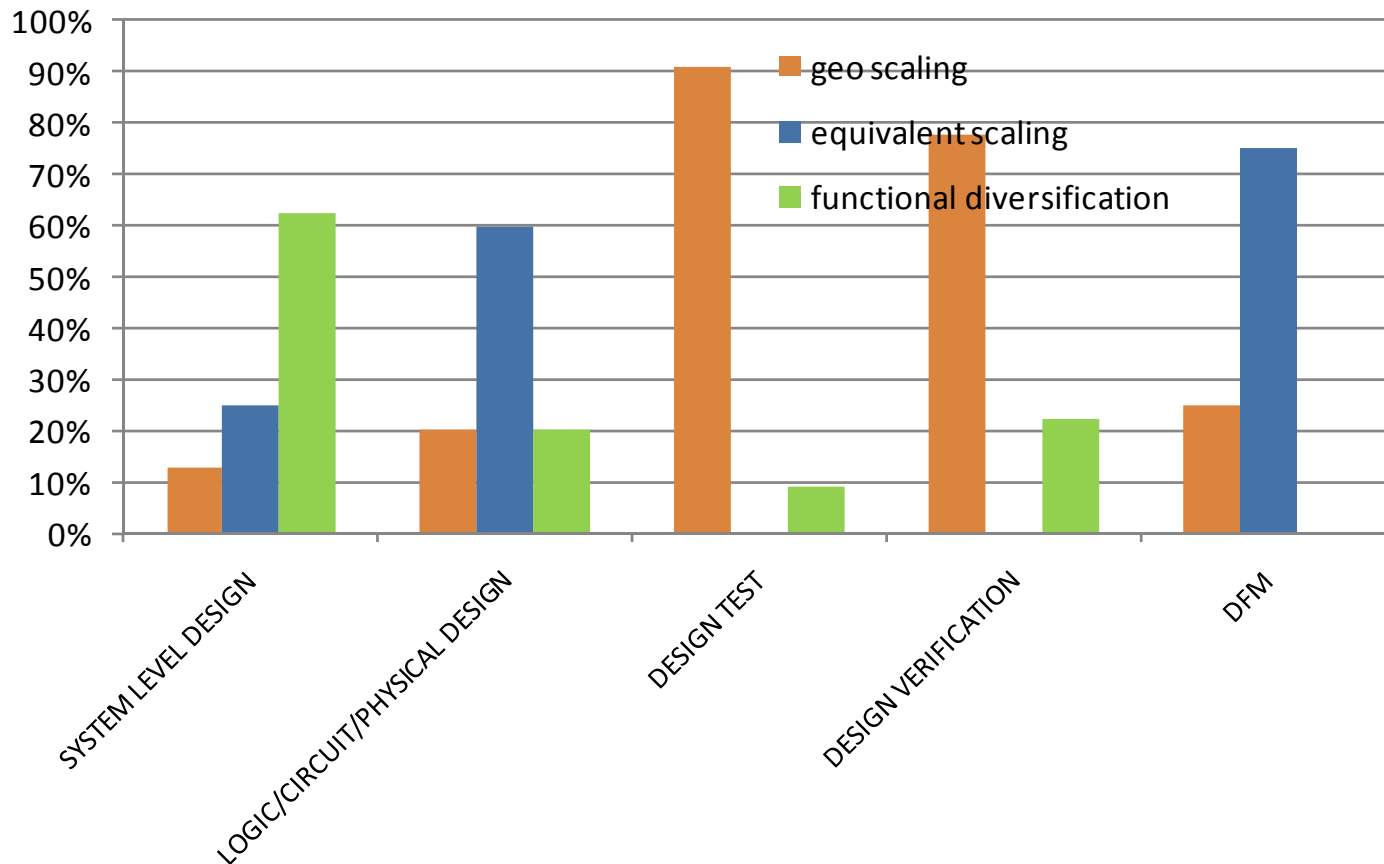
ITRS Design TWG 2007

**2007 ITRS DRAFT DO NOT PUBLISH**

# Design-Driven Semiconductor Innovation (Moore+)

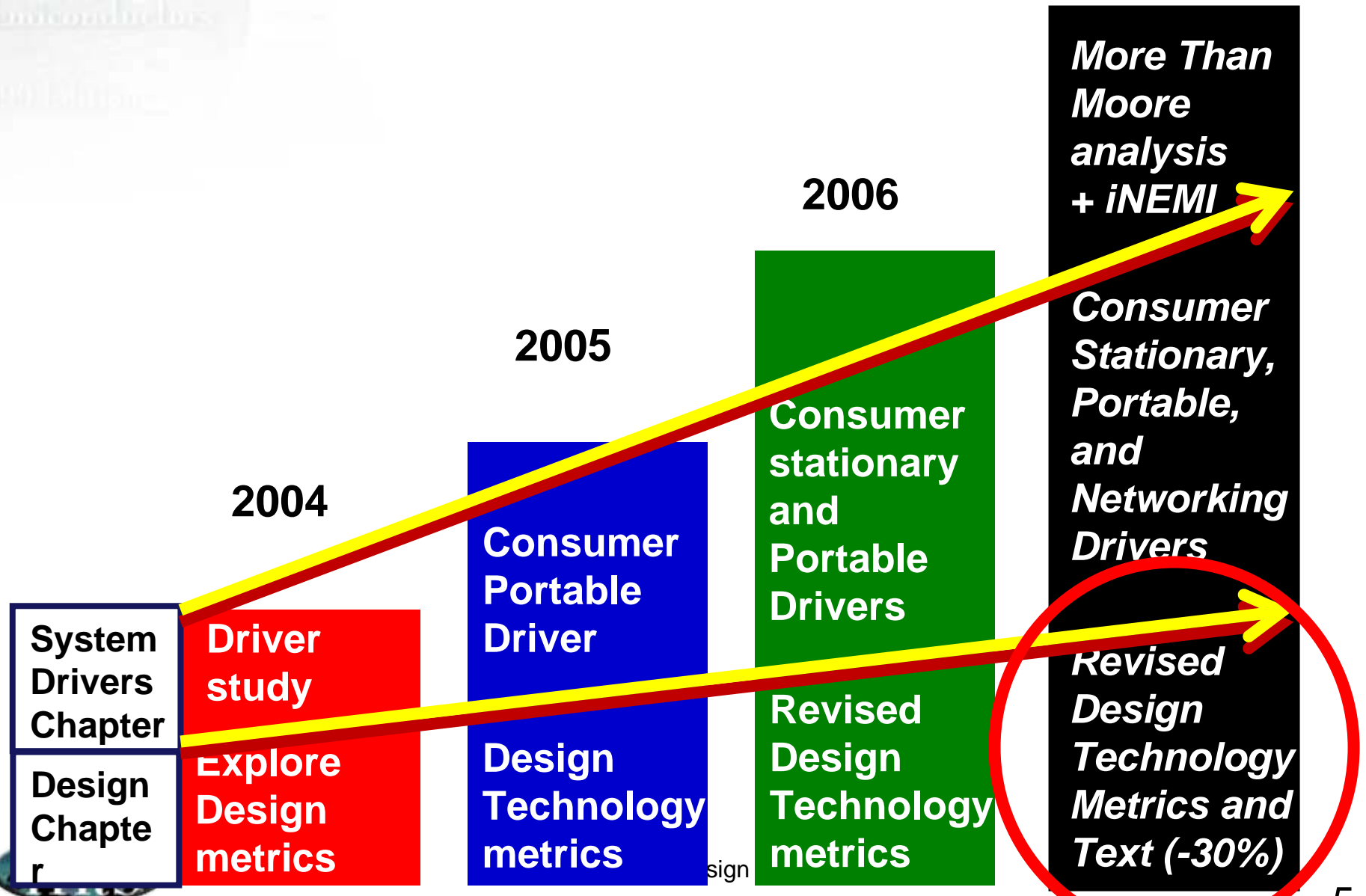
Domain / market independent *Inventory 50+ Design Solutions*

→ Reveals impact of More Than Moore on key design phases



# ITRS Design + System Drivers

2007



# Design Chapter Sections Improved, Reduced Format

Target of 1/4 to 1/3 page reduction. Three main portions:

## (a) Requirements table

- 1-2 pages. Includes subsection description, metric definitions, rationale for each number.
- Number of metrics: 10 max. (more subject to approval)

## (b) Solutions table

- 1 to 1.5 pages. Includes definitions for each solution, and rationale for each solution.
- Number of solutions: 10 max. (more subject to approval)

## (c) Mapping from challenges to solutions

- maps challenges to solutions. Not need to be 1-to-1. Explain requirements with no solutions.
- $\leq 1$  page.



# Design Technology Roadmap

## Improved Parameter Explanations

### Example: Logic / Circuit / Physical Design

Asynchronous global signaling  
% of a design driven by handshake clocking

(Requirement) This requirement refers to a design style where instead of using global clock, synchronization is performed through request, and acknowledge lines.

The need for the asynchronous global signaling will rise as the repeater insertion returns diminish with increasing die size, clock frequency and power consumption. (22k in 180nm processor, 1.5M projected in 65nm). By 2012 further progress in asynchronous clocking would depend on the provided tool support. Rapidly maturing arbitration schemes (e.g. crossbar of Fulcrum Microsystems, trees) are likely to evolve through 2014 improving latency of a design.

Parameter uncertainty  
%-effect (on sign-off delay)

(Prediction) Here %-effect is predicted as a function of parametric variation in shrinking devices. Accounting for parametric uncertainty can lead to 9% worst case delay improvement in a 16-bit multiplier at three sigma set to 20% of the mean ("Statistical timing based on incomplete probabilistic description of parameter uncertainty", M. Orshansky et al, 43rd DAC). As the technology scale, the uncertainty requirements are proportional. According to IBM (eetimes, 06.06.2005) statistical methods will become a mainstream at 45nm. (note: pls correct the req. tables to start yellow at 45nm, instead of 28)

Simultaneous analysis objectives  
# of objectives during optimization

(Requirement) Area, power (active or dynamic), timing, and noise immunity are currently main optimization objectives that are required to be optimized together (indirectly, or directly they effect each other). Currently developed statistical methods (e.g. IBM) are likely to integrate yield optimization into existing optimization process by 2008, and become mainstream in 2010 to improve development time and yield by 25% (see "Statistical analysis to yield better chips", eetimes, 03/27/03). Optimizations for reliable computing will extend existing techniques for robust computation (e.g. Razor), and have promise to be integrated in design flow by 2009. Productivity cost (development time) will be part of equation in 2013 as well. Productivity measures are only loosely defined these days, and no mature optimization techniques are known (hence requirement turns red in 2013.) However, the arising need for measuring chip productivity is emerging as one of the most important factors in chip design, and may need integration with other objectives by 2013.

# Design Technology Roadmap

## New Requirement-Solution Matching Tables

### Example: Logic / Circuit / Physical

Parameter uncertainty %-effect (on sign-off delay)	Synthesis and timing accounting for variability	These solution tools account for parametric uncertainty to improve chip
	Circuit/layout enhancement accounting for variability	Optimizations which consider parametric uncertainty
Simultaneous analysis objectives # of objectives during optimization	Power management analysis & logic insertion SOI SoC tools	Requires budgeting various area/power/timing constraints
	Cost-driven implementation flow	Cost is an engineering parameter effecting turn-around times. Silicon is no longer dominant factor. Test, manufacturing costs increase emphasis on adaptive, self-repairing circuits.
Circuit families # of circuit families in a single design	Non-static logic implementation	Non-static implementations help improving different chip parameters
Analog content synthesized % of a design	Analog synthesis (circuit/layout)	The solution allows for larger portions of a chip to be in analog
Leakage whole chip (normalized to current power dissipation of achip)	Macro block/chip leakage analysis	Right models are key enabler in accurate leakage predictions
	Power management analysis & logic insertion SOI SoC tools	Requires budgeting various area/power/timing constraints

# Design Technology Roadmap

## New Requirement-Solution Matching Tables

### Example: Design For Manufacturability

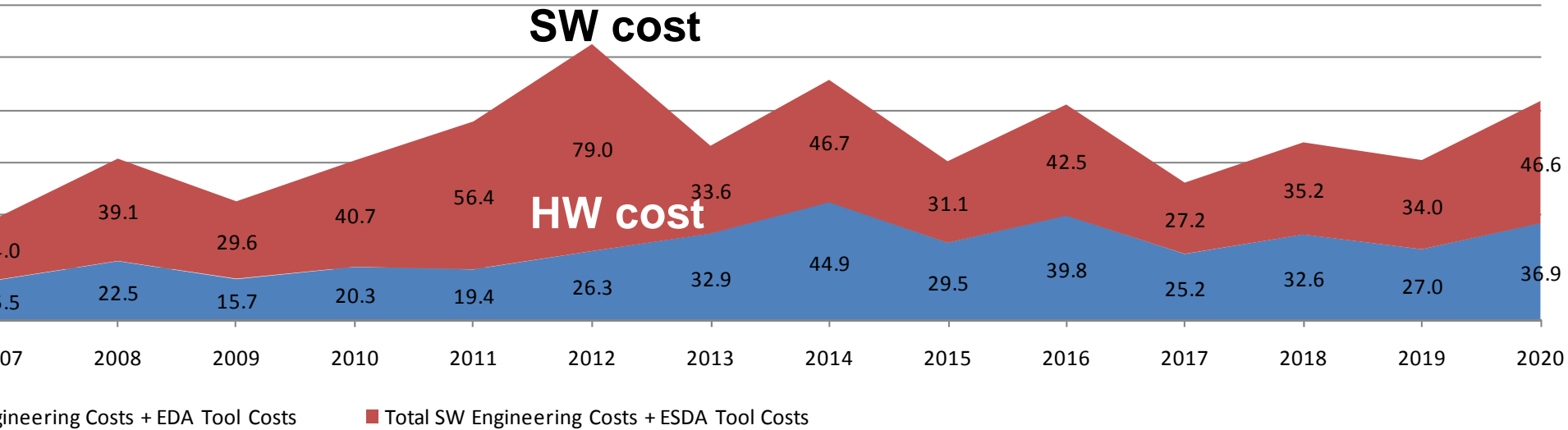
% $V_{dd}$ Variability % variability seen at on-chip circuits	Tools that account for mask cost in their algorithms	Obvious
	Radically-restricted rules (grid-like layouts, no diagonals, etc.)	This allows for better manufacturability by the design, reducing mask complexity, and improving yield.
	RET tools that are aware of circuit metrics (timing, power)	This allows for more effective optimization and reduction of design loops.
	Statistical leakage analysis and optimization tools	Leakage power variability will soar. Statistical leakage tools are critical to estimate and control it.
	Post-tapeout RET interacting with synthesis, timing, P&R	By interacting with earlier-in-the-flow EDA tools, we can address effectively litho issues.
	model-based physical verification	By using an explicit litho model-based physical design toolset, we can address litho issues with precision.
	model-based physical synthesis	The explicit litho model-based approach above will move to the physical synthesis toolset.
	manufacturing-friendly design rules (hard rules)	Manufacturing-friendly rules reduce mask and manufacturing cost and address printability.
% $V_{th}$ variability Doping Variability impact on VTH	Statistical analysis and opt. tools and flows (Vdd, T, Vth)	By providing a better estimate of the impact of variability, circuits don't need to be overdesigned.
% $V_{th}$ variability Includes all sources	Statistical analysis and opt. tools and flows (Vdd, T, Vth)	By providing a better estimate of the impact of variability, circuits don't need to be overdesigned.
	Adaptable and redundant circuits	These circuits resistant to variability allow an extra degree of freedom in addressing variability.
	Statistical leakage analysis and optimization tools	Leakage power variability will soar. Statistical leakage tools are critical to estimate and control it.



# New Software Design Roadmap Combined HW+SW Design Cost

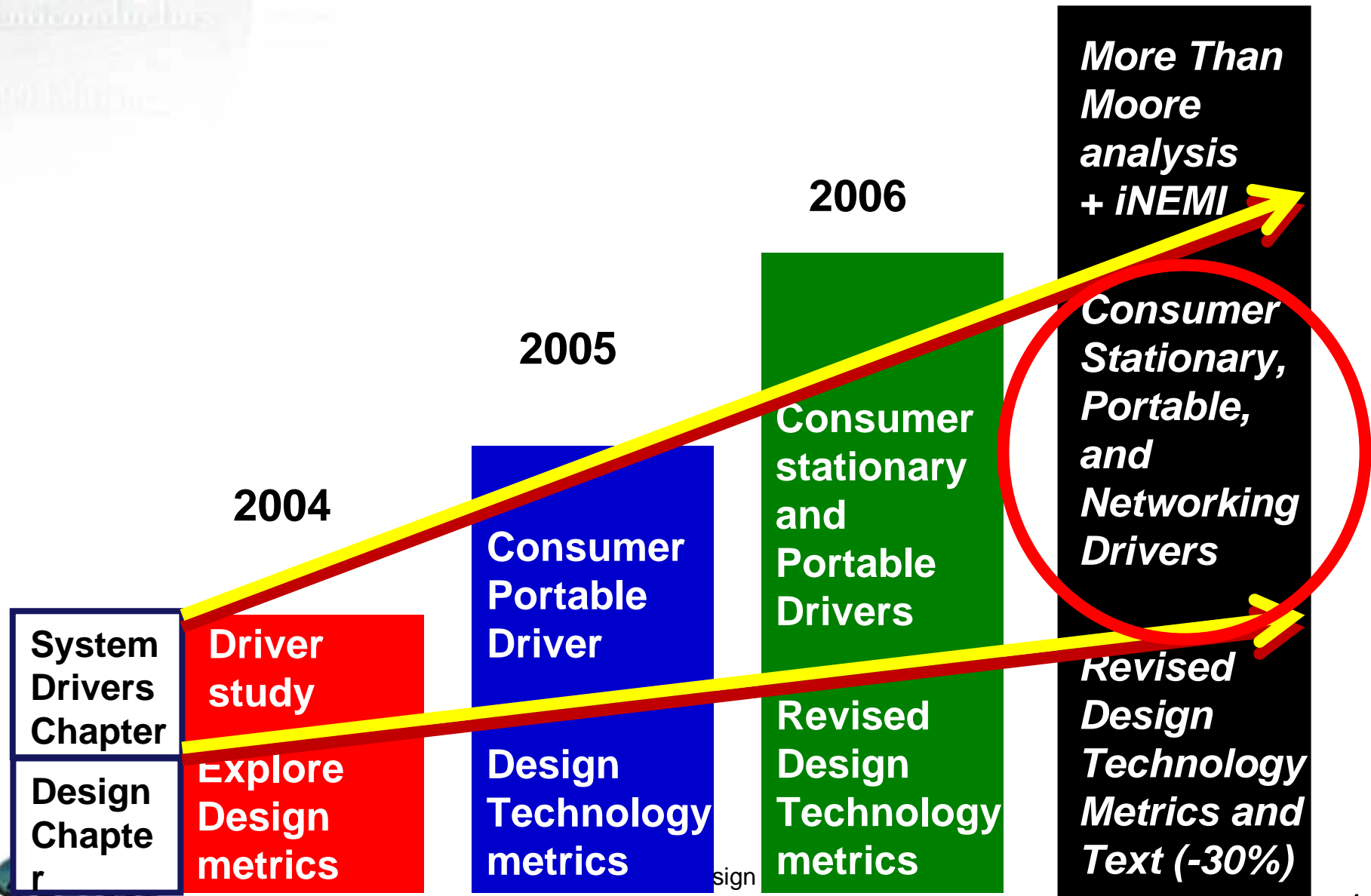
**NRE cost for SW design to equal HW design**

*→ until design technology for SW issues is addressed*

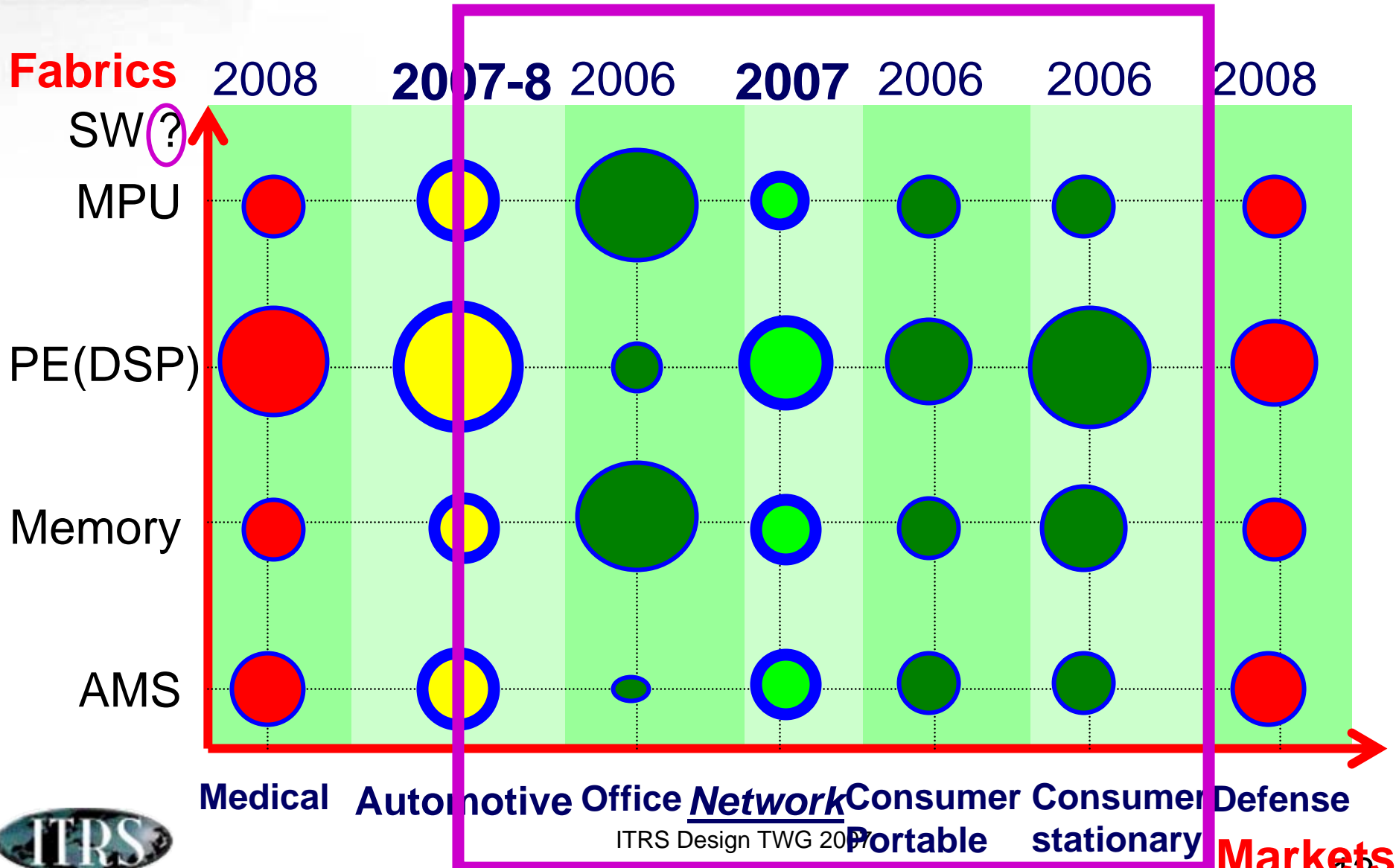


# ITRS Design + System Drivers

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# An Expanded Set of Drivers Will Direct An Increasingly Broad Industry



# New *Networking System Driver*

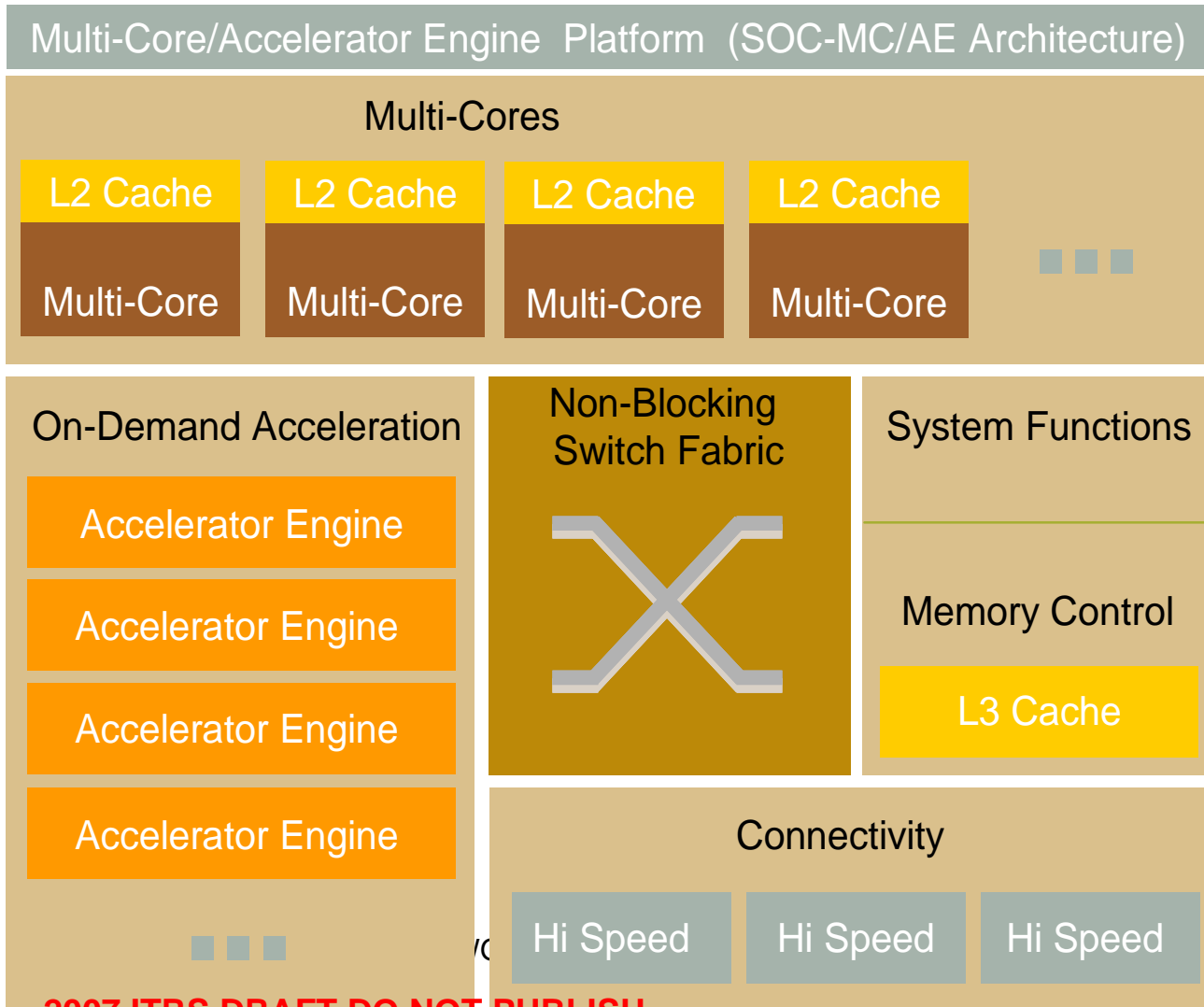
## Multi-Core/Accelerator Engine SoC - Architecture template

### Goals

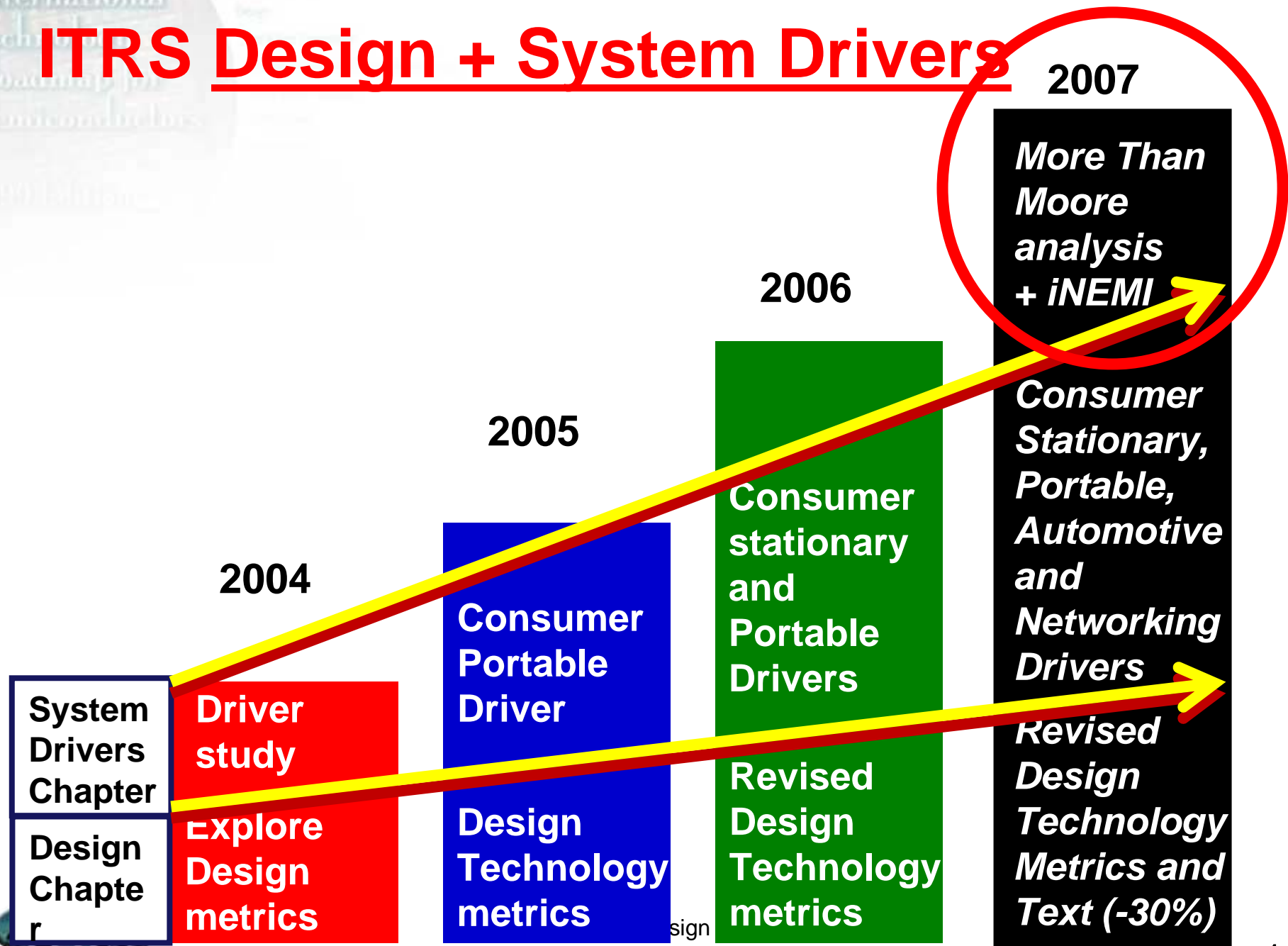
- Performance
- Ease of use

### Components

- On-chip fabric
- 32+ cores with private memory
- Accelerator engine app-specific



# ITRS Design + System Drivers



# Moore+ Parameter Inventory

## Classification of 50+ design technology solutions

1. Supporting Moore's Law – **More Moore (geo scaling)**
2. Extending Moore's Law – **More Moore (equivalent scaling)**
3. Beyond Moore's Law – **More Than Moore (architecture diversification)**

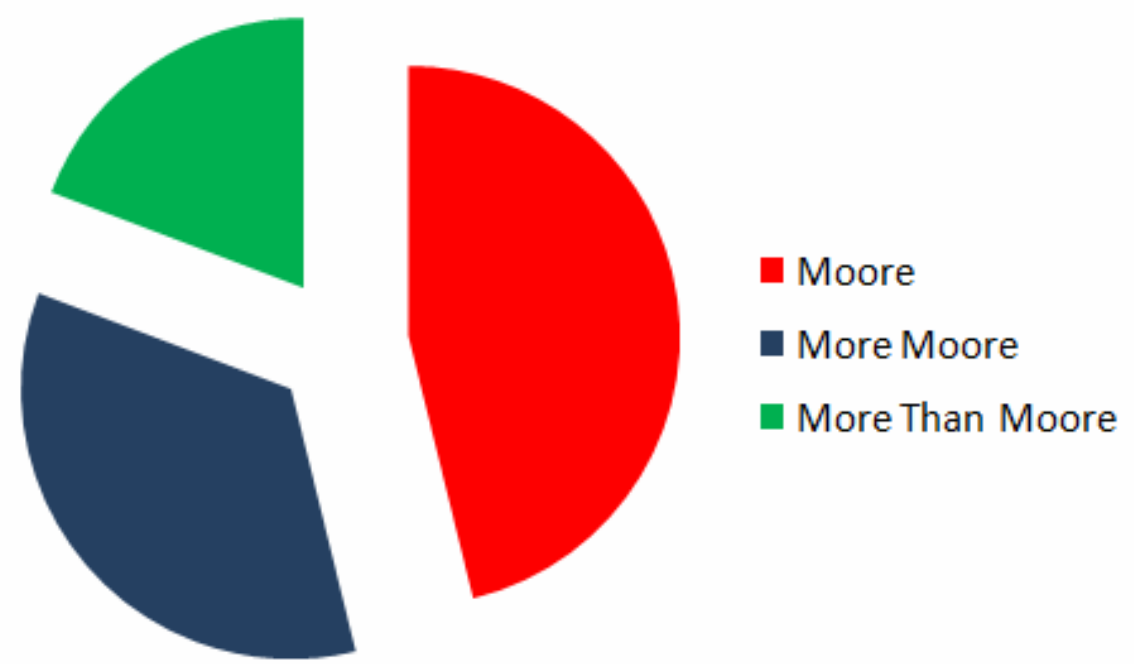
## Example: System-Level Design Solutions

	<b>Geometrical scaling</b>	<b>Equivalent scaling</b>	<b>Functional diversification</b>
	<b>Moore</b>	<b>More Moore</b>	<b>More Than Moore</b>
System level component reuse	1		
Chip package co design methods			1
Improved system level power estimation techniques		1	
On chip network design methods	1		
mixed signal / RF verification		1	
automated interface synthesis			1
HW/SW co design and verification			1
Multi fabric implementation planning (AMS/RF/MEMS)			1

# Moore+ Parameter Inventory

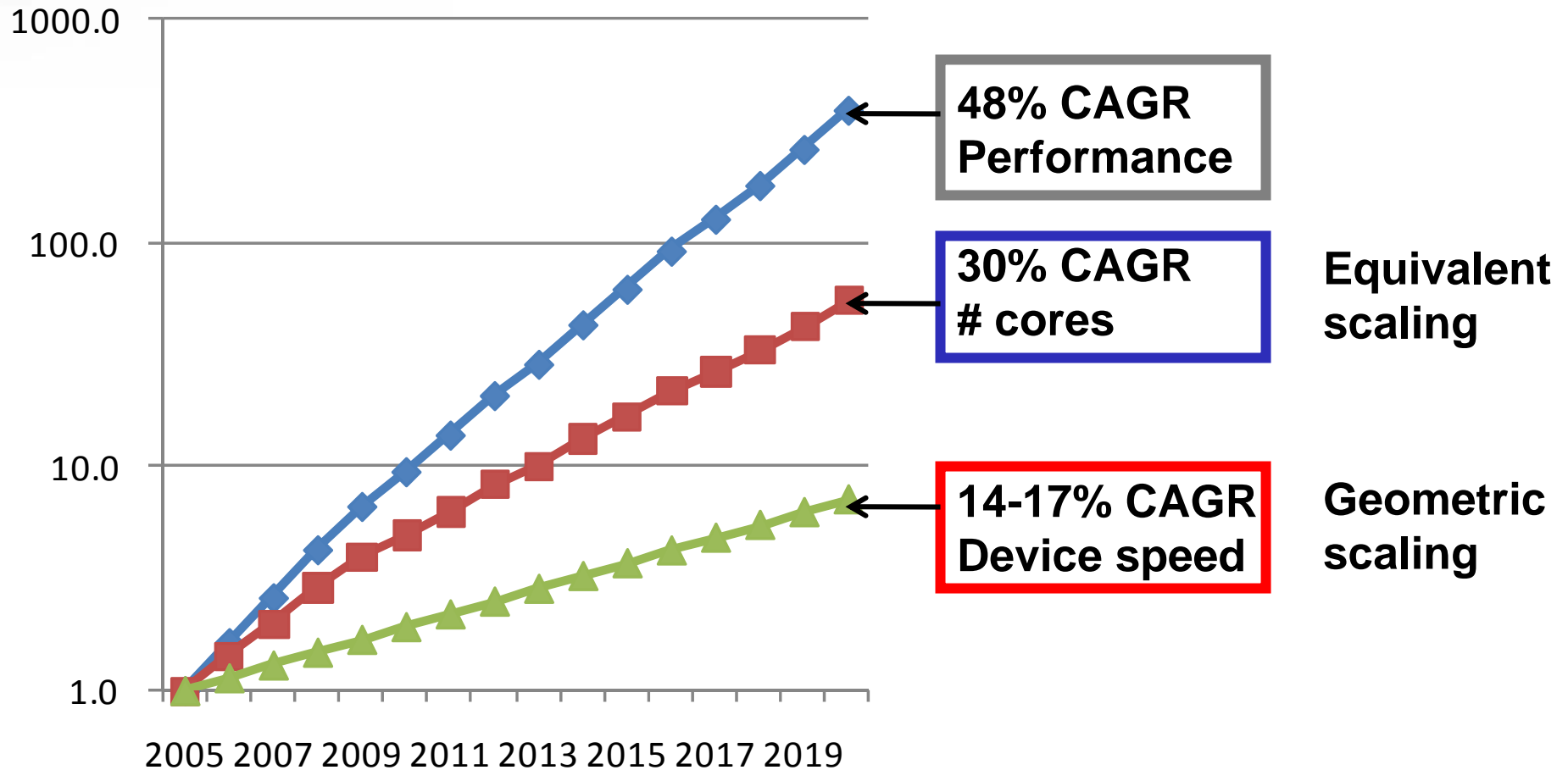
- Large percentage of non-Moore contributions
  - More Moore:
  - More Than Moore:

Moore+ Inventory of Design solutions



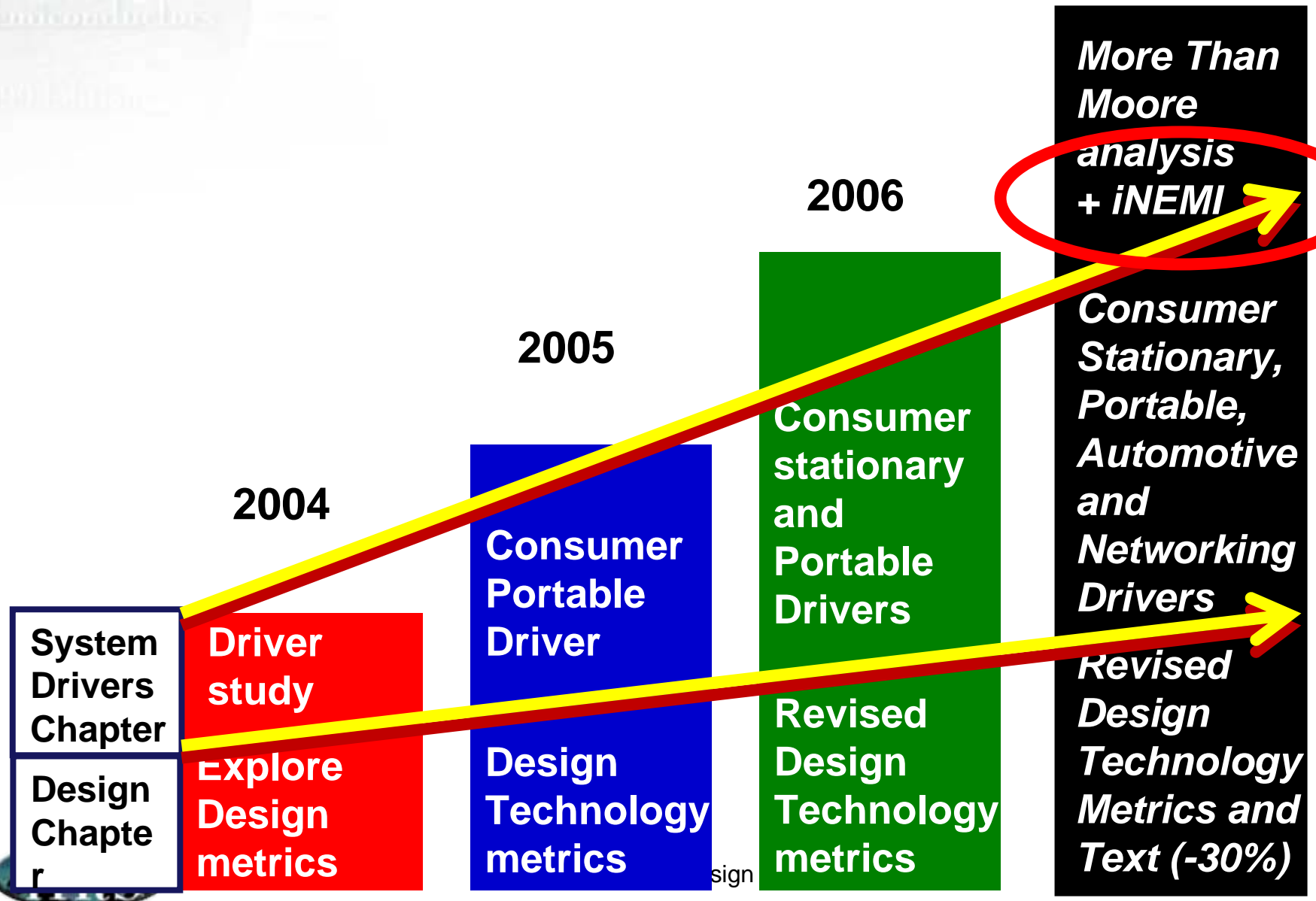
# More Than Moore "Pilot Example"

*Focused on design levers e.g. multi-core*

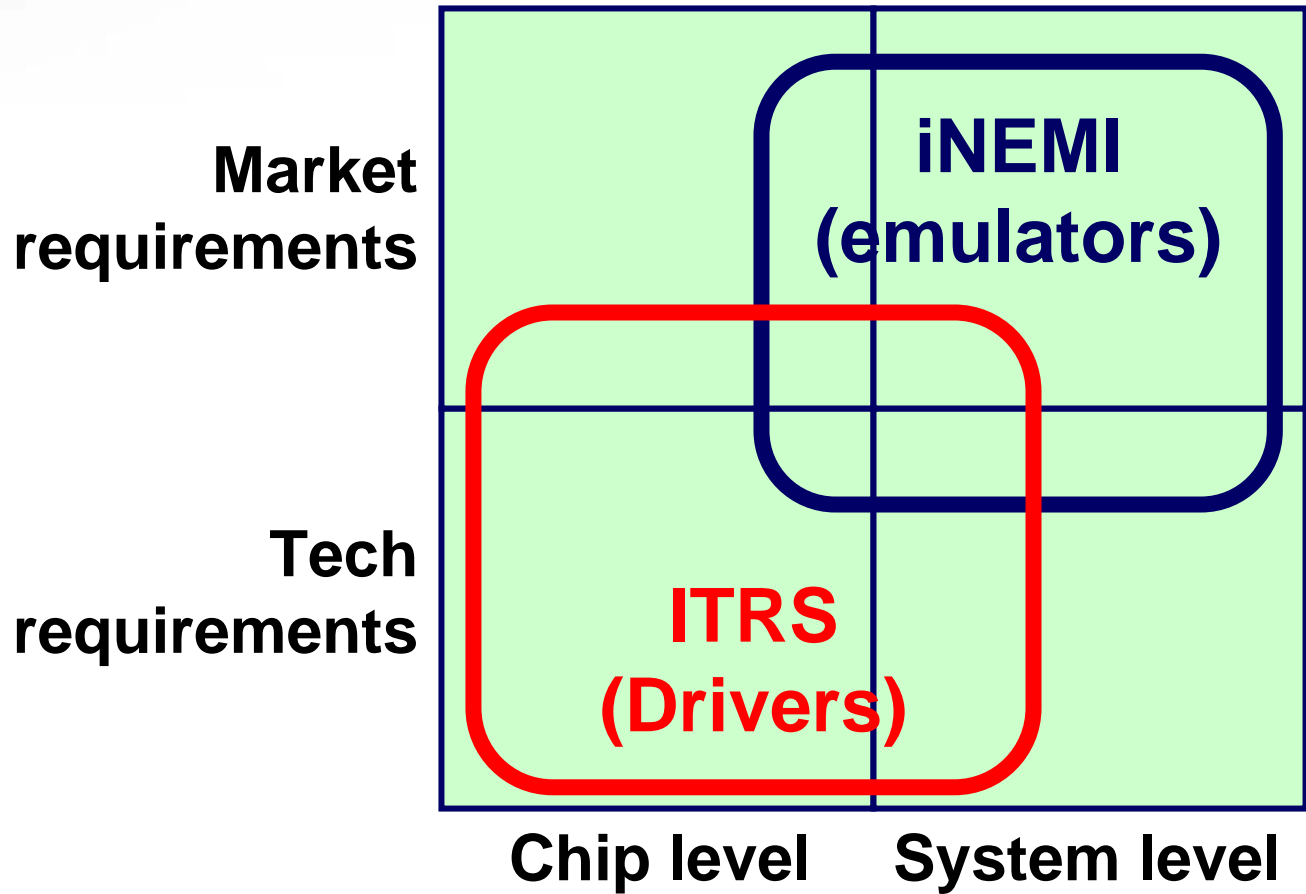


# ITRS Design + System Drivers

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# ITRS-iNEMI Domain Space



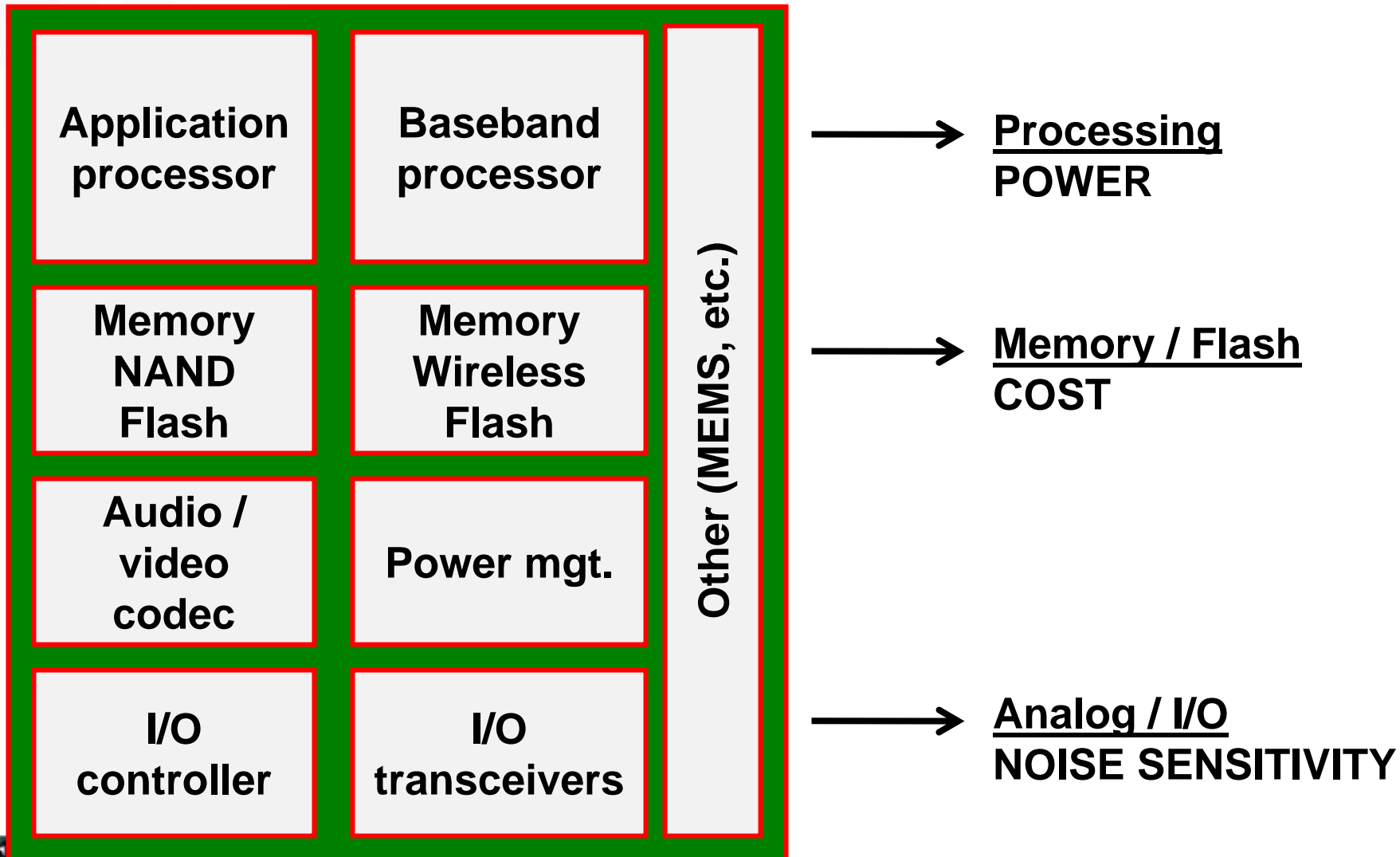
# 1st Alignment Between Chip and System Roadmaps

Consumer portable pilot, focused on power/energy

Parameter	COLOR	Metric	2005	2007	2009	2011	2017	Where in ITRS	
Number of Voltages	Red	#						only one (core logic)	
Minimum Logic Family Voltage	Red	Volts	2.5	2	1.8	1.5	0.8	consumer driver	
Maximum Logic Family Voltage	Red	Volts	5	3.3	2.85	2.2	1.8	consumer driver	
Normal Logic Family Voltage	Green	Volts	3.3	2.85	2.2	1.8	1.2	consumer driver	
<b>POWER</b>									
Power	Yellow	Type	u Polymer, n	u Polymer, n	u Polymer, m	u Polymer, meth	u Polymer, n	NO?	
Spec. energy	Green	Wh/kg	150	175	200	300	400	NO?	
Energy dens	Red	Wh/liter	400	500	550	600	800	NO?	
Specific power	Red	W/kg	1000	2000	4000	5000	6000	NO?	
Shelf life	Red	years	3 years	3 years	4 years	5 years	8 years	NO?	
Avg. standby power	Green	Watts						consumer driver	
Voltage (avg.)	Red	Volts	<b>~10 parameters to be aligned</b>						consumer driver
Voltage (min.)	Red	Volts							consumer driver
Current (avg.)	Red	mA							consumer driver
Run Time Before Recharge	Green	Hours						NO?	
Min. and Max. Operating Temperature	Green	Degrees C						NO?	
Max Reflow Temp	Red	Degrees C						NO?	
<b>THERMAL</b>									
Use Ambient Operating Temperature Range	Red	Deg C - Deg C	-10 to 50	-10 to 50	-10 to 50	-10 to 50	-10 to 50	NO?	
Thermal Design Power (Hottest Chip)	Green	Watts	30	40	45	50	60	consumer driver	
Max Current per Device	Green	Amps						consumer driver	
Thermal Design Flux (Hottest Chip)	Green	W/sq. cm						NO?	
Cooling Method	Green	Passive,Active, I both		both	both	both	both	NO?	
Number of Chips W/Some Heat Sink	Red	# / Assy or Boar						NO?	
Device Cooling Air Temperature (Inside the Box)	Red	Deg C						NO?	
Device Cooling Rail Temperature	Red	Deg C						NO?	
Chips W/ Power < 2W	Red	# / Per Assembl						consumer driver	
Chips W/ Power From 2 - 5 W	Red	# / Per Assembl						consumer driver	
Chipc W/ Power From 5 - 10 W	Red	# / Per Assembl						consumer driver	
Chips W/ Power > 10 W	Red	# / Per Assembl						consumer driver	
Module Power	Yellow	W / sq. cm.						NO?	

# iNEMI-ITRS

## ITRS Portable *System* Model



# iNEMI-ITRS Power Reconciliation

## Top-10 Parameters to be Reconciled

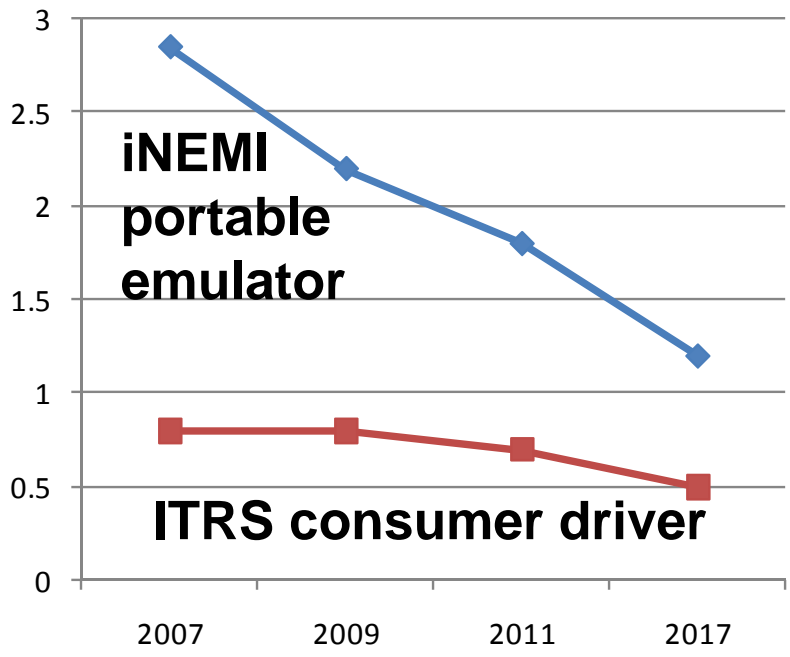
Portable emulator						Consumer portable driver				
iNEMI		iNEMI	iNEMI	iNEMI	iNEMI	ITRS	ITRS	ITRS	ITRS	
iNEMI Parameter	Metric	2007	2009	2011	2017	ITRS parameter	2007	2009	2011	2017
Normal Logic Family Voltage	Volts	2.85	2.2	1.8	1.2	Logic voltage	0.8	0.8	0.7	0.5
<b>POWER</b>										
Spec. energy	Wh/kg	175	200	300	400	N/A				
Avg. standby power	Watts					Total static power	0.052	0.09	0.146	0.58
Run Time Before Recharge	Hours	0.0875	0.05	0.06	0.06667	N/A				
<b>THERMAL</b>										
Use Ambient Operating Temp Range	Deg C - De	-10 to 50	-10 to 50	-10 to 50	-10 to 50	N/A				
Thermal Design Power (Hottest Chip)	Watts	40	45	50	60	total power	0.74	1.281	1.639	3.709
Max Current per Device	Amps					Chip current (P/V)	0.93	1.60	2.34	7.42
Thermal Design Flux (Hottest Chip)	W/sq. cm					N/A				
Cooling Method	Passive,Ac	both	both	both	both	N/A				



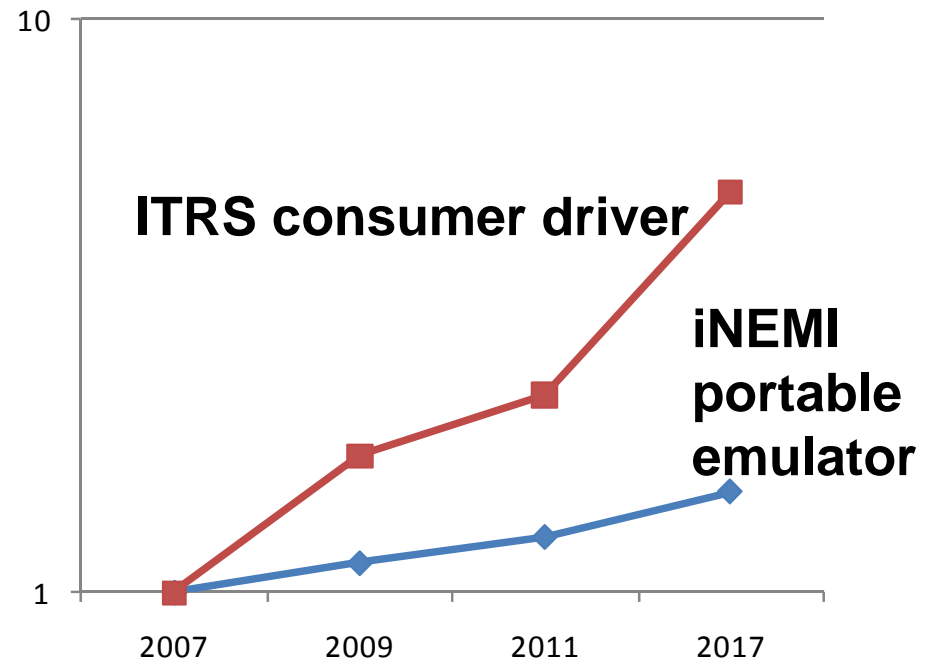
# iNEMI VS ITRS (System V. Chip) Power Parameters' Comparison

**ITRS stuck between lower voltages and higher power trends**

### Voltage supply trends

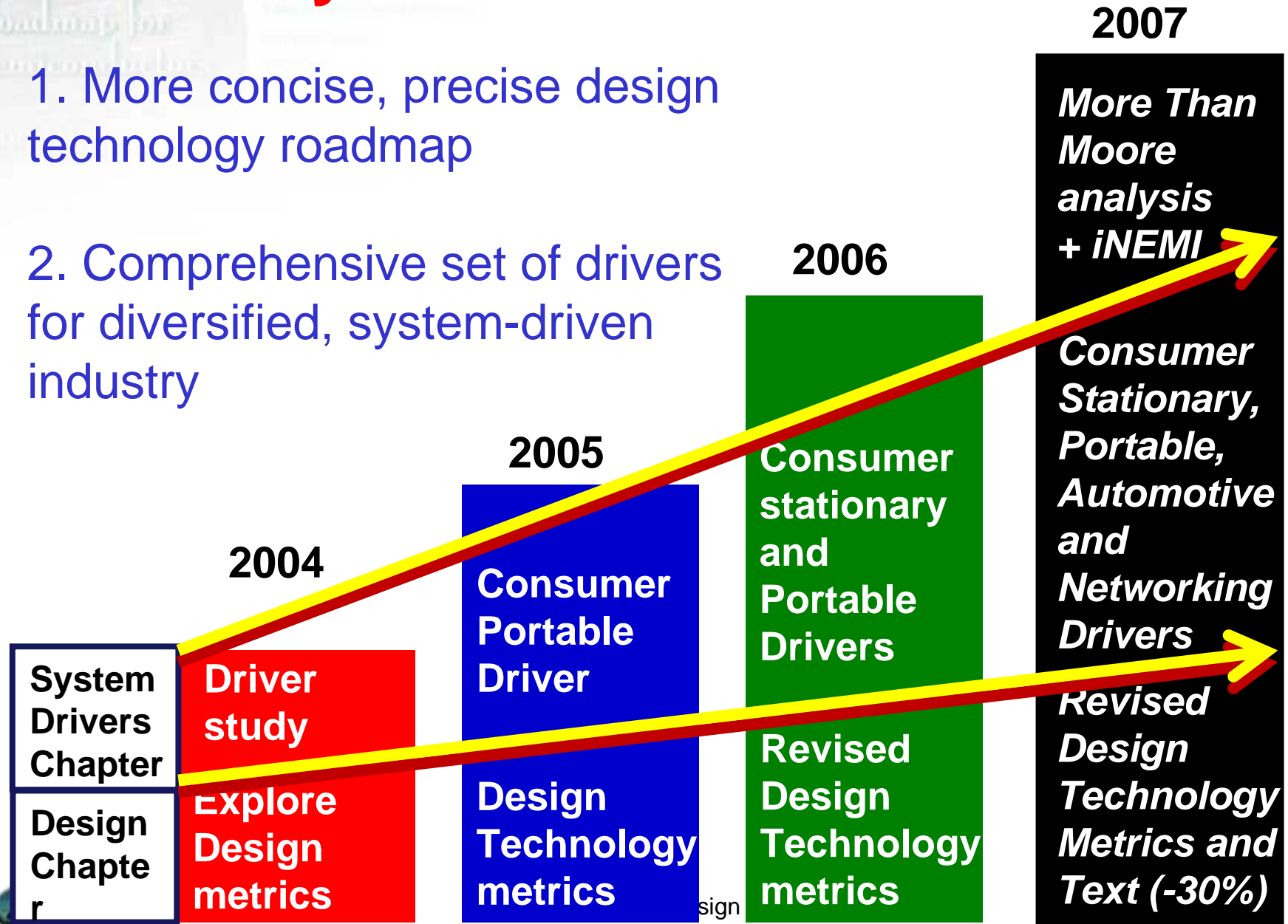


### Power trends

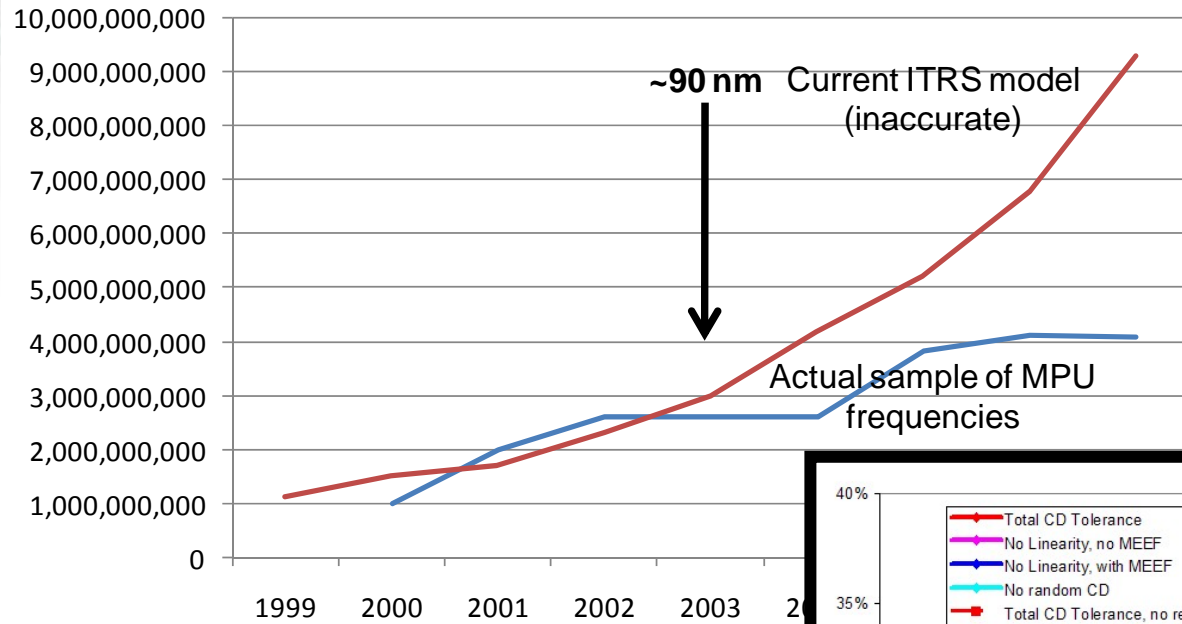


# Summary

1. More concise, precise design technology roadmap
2. Comprehensive set of drivers for diversified, system-driven industry



# Some 2008 Topics



**Adjustment of frequency trends**

**Adjustment of CD tolerance**

