2007 Test and Test Equipment

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San Francisco, USA

Roger Barth

ITRS Test TWG

2007 Test TWG Members

44 members – 26 companies

Name	Affiliation	Name	Affiliation
Dave Armstrong	Advantest	Yi Cai	LSI
Paul Roddy	Advantest	Yasuo Sato	Hitachi (STRJ)
Mike Bienek	AMD	Jerry McBride	Micron
Calvin Cheung	ASE	Peter Maxwell	Micron
Rob Aitken	ARM	Bill Price	NXP Semiconductors
Atul Goel	Avago Technologies	Rene Segers	NXP Semiconductors
Rudy Garcia	Credence	Yasumasa Nishimura	Renesas
Steve Payne	Credence	Rochit Rajsuman	Roctechnology
John Lukez	Credence	Sejang Oh	Samsung
Larry Gilg	Die Products	Mitsuo Yamazaki	Shibasoku (STRJ)
Jack Courtney	IBM	Davide Appello	STMicroelectronics
Shawn Fetterolf	IBM	Sridhar Kannan	Stream Processors
Anne Gattiker	IBM	Tom Williams	Synopsys
Phil Nigh	IBM	Brad Robbins	Teradyne
Jody Van Horn	IBM	Lee Song	Teradyne
Don Wheater	IBM	Steve Comen	TI
Peter Muhmenthaler	Infineon	Ulrich Schoettmer	Verigy
Phil Burlison	Inovys	Erik Volkerink	Verigy
Wendy Chen	KYEC	Yervant Zorian	Virage Logic
Cheng-Chin Ni	KYEC		
Roger Barth	Intel - Chair	Bill Ortner	Consultant
David Wu	Intel	Mike Rodgers	Consultant
		Ken Skala	Consultant
		Burnie West	Consultant

Chapters

No Change

- **Key Drivers, Difficult Challenges, Opportunities**
- **Focus Topic: Test for Yield Learning**
- **Focus Topic: Cost of Test**
- **SoC and SiP**
- **Logic**
- **Memory**
- **Analog, Mixed Signal, RF**
- **Reliability Technology and Burn-in**
- **Mechanical: Handlers and Probers**
- **Interface: Probecards and Test Sockets**

Key Drivers

- **Device trends**
  - Increasing device interface bandwidth (# of signals and data rates)
  - Increasing device integration (SoC, SiP, MCP, 3D packaging)
  - Integration of emerging and non-digital CMOS technologies
  - Complex package electrical and mechanical characteristics
  - Device characteristics beyond one sided stimulus/response model
  - **Multiple I/O types and power supplies on same device**
- **Increasing test process complexity**
  - Device customization during the test process
  - "distributed test" to maintain cost scaling
  - Feedback data for tuning manufacturing
  - **Dynamic test flows via "Adaptive Test"**
  - Higher order dimensionality of test conditions
- **Continued economic scaling of test**
  - Physical limits of test parallelism
  - Managing (logic) test data and feedback data volume
  - Effective limit for speed difference of HVM ATE versus DUT
  - Managing interface hardware and (test) socket costs
  - Trade-off between the cost of test and the cost of quality
  - System test and BIST driving multiple test socketings

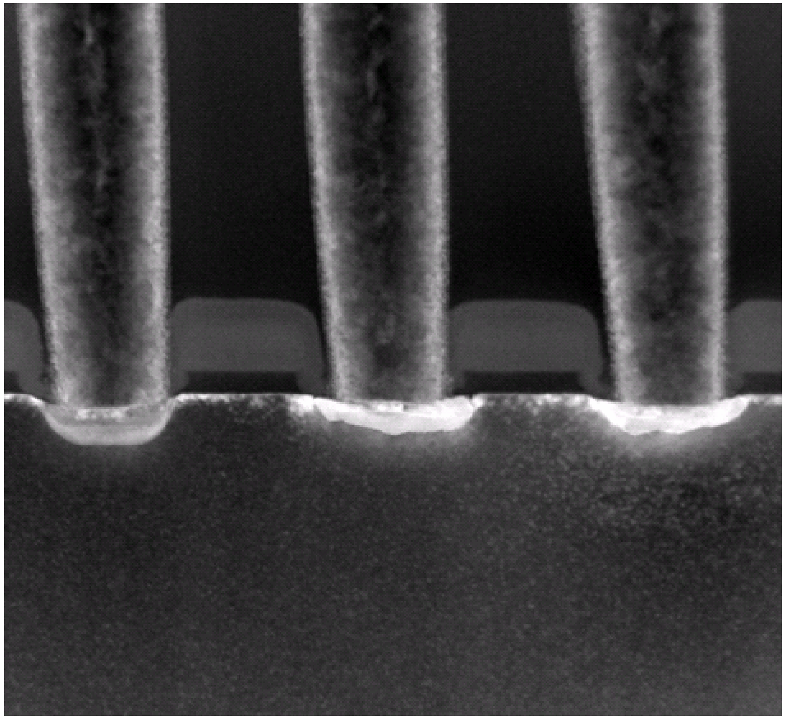
Key Challenges

No Change

- **Test for yield learning**
  - Essential for fab process and device learning below optical capability
- **Increasing systemic defects**
  - Testing for local non-uniformities, not just hard defects
  - Detecting symptoms and effects of line width variations, finite dopant distributions, systemic process defects
- **Screening for reliability**
  - Implementation challenges and efficacies of burn-in, IDDQ, and Vstress
  - Erratic, non deterministic, and intermittent device behavior
- **Potential yield losses**
  - Tester inaccuracies (timing, voltage, current, temperature control, etc)
  - Over testing (e.g., delay faults on non-functional paths)
  - Mechanical damage during the testing process
  - Defects in test-only circuitry or spec failures in a test mode
    - e.g., BIST, power, noise
  - Some IDDQ-only failures
  - Faulty repairs of normally repairable circuits
  - Decisions made on overly aggressive statistical post-processing

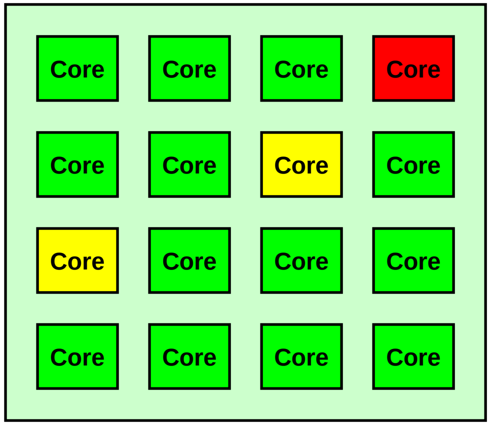
Challenge: Test for Yield Learning

- **“Visualize” Non-visible defects**
  - Predominant in roadmap
  - Feature of approaching the wall
- **Fab improvement**
  - Systematic defects
  - Dependent on test feedback
- **Smart software?**
  - Find common signatures in fail data
- **New device types**
  - Nano-tube
  - PRAM, RRAM, FRAM



Challenge: Fault Tolerant Device "Bad but Good"

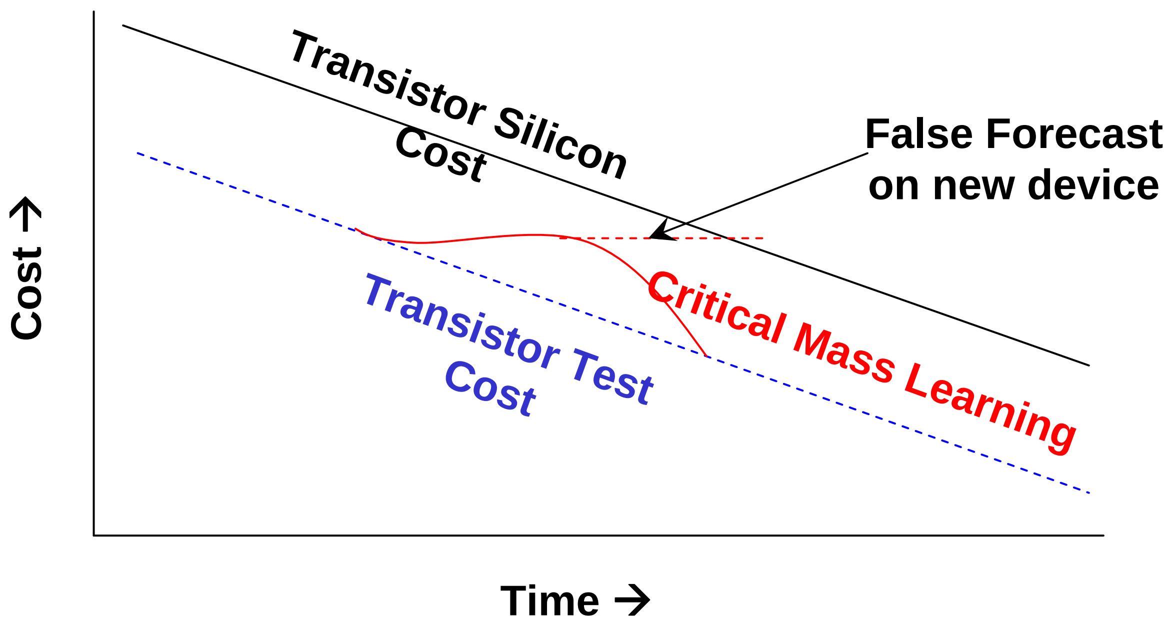
- **Multi identical core MPU**
- **Core issues**
  - 1 bad
  - 2 marginal
- **Is MPU good or bad?**
  - Disable cores?
  - Fix or "Ignore" with smart OS kernel?



Challenge: Cost Trend

- **Maintain Moore's Law learning**
  - Deviations are a call to action - i.e. Functional to Structural test

- **Learning curve lag on new devices, integrations or architectures**
  - Low cost test methods require critical mass learning



Future Opportunities

No Change

- **Test program automation (not ATPG)**
  - Automation of generation entire test programs for ATE
- **Simulation and modeling**
  - Seamless Integration of simulation and modeling of test interface hardware and instrumentation into the device design process
- **Convergence of test and system reliability solutions**
  - Re-use and fungibility of solutions between test (DFT), device, and system reliability (error detection, reporting, correction)

Cost of Test

No Change

$ NRE Costs

- $ DFT design and validation
- $ Test development

$ Device Costs

- $ Die area increase
- $ Yield loss

$ Work-Cell Cost

- $ Building Capital
- $ People
- $ Consumables
- $ Loadboards, DUT interface

$ Capital Equipment

Depreciation of:

- $ Test Equipment
- $ Handler/Prober

Untested Units → **Work-Cell** → Good Units Shipped

Work-Cell → Rejected Units

UPH/$M

Effectiveness Measure

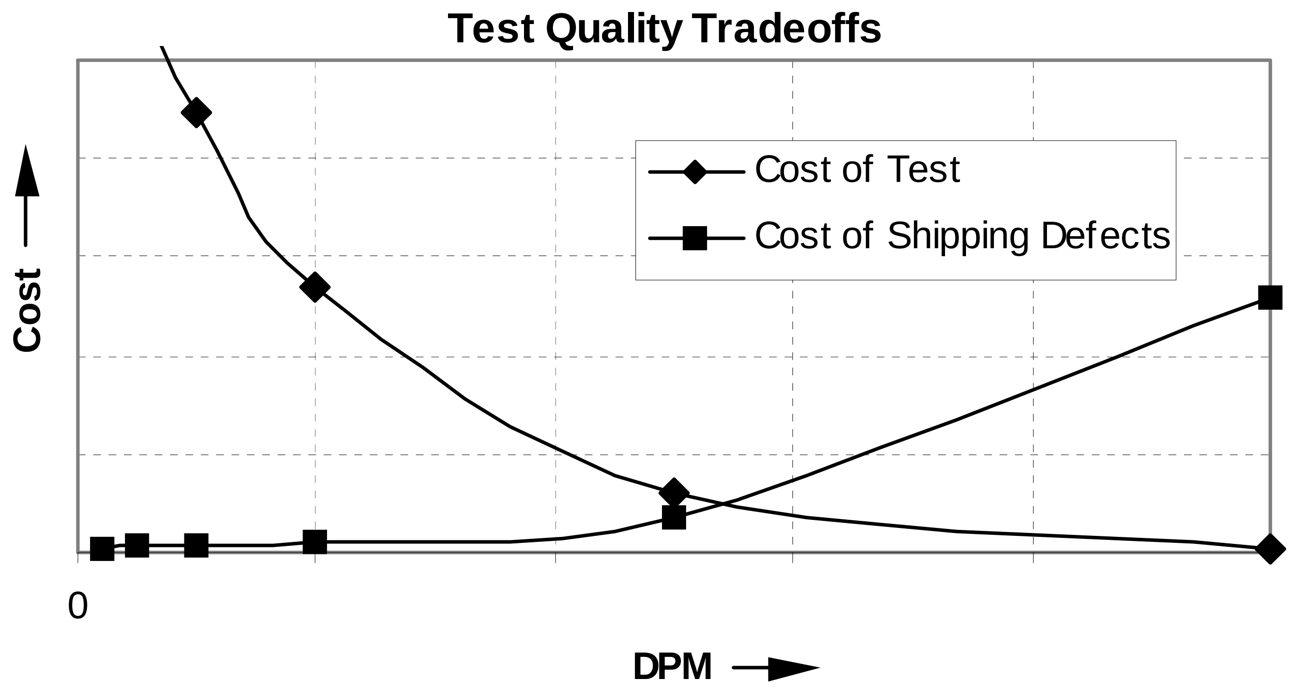
Goal is to optimize product cost

- Must strike a balance between cost/value of design, manufacture, yield learning, and test

Cost of Quality

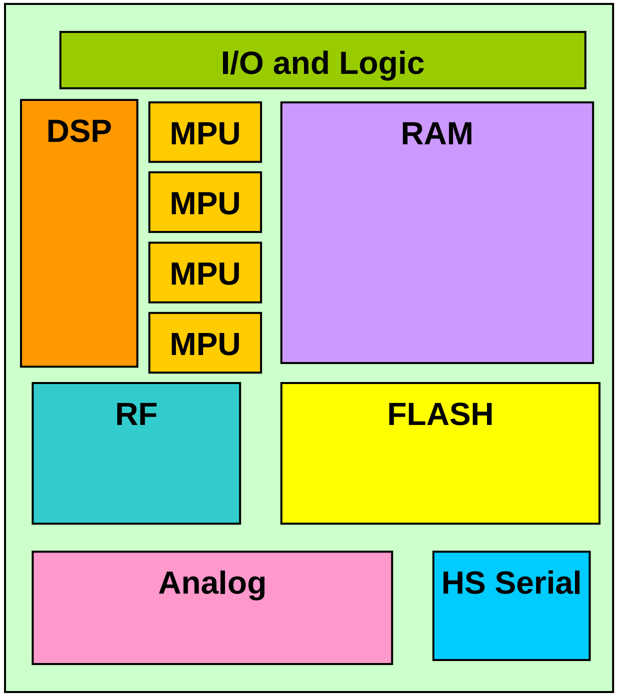
No Change

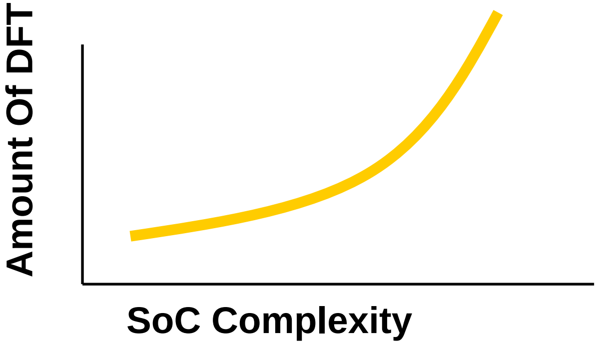
- **Test is a balance of DPM and cost**
- **Shipped defect cost is more than bad components**
  - Customer relationships, goodwill, penalties



SoC – Consumer Logic

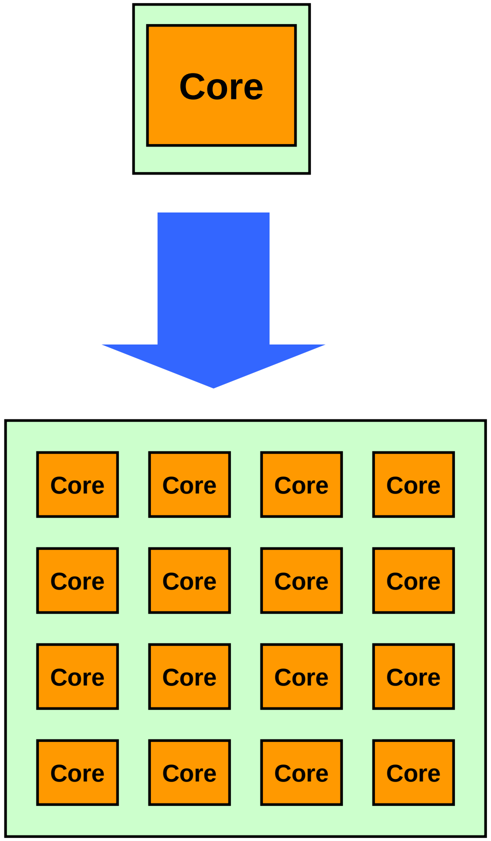
- **Combination of cores**
  - MPU / logic
  - Memory
  - Analog / RF
  - HS serial
- **Per core DFT**
- **SoC test challenges**
  - Management of per core DFT
  - Standardization of core "wrappers"
    - IEEE 1500 core test
    - IEEE P1687 JTAG chip-test



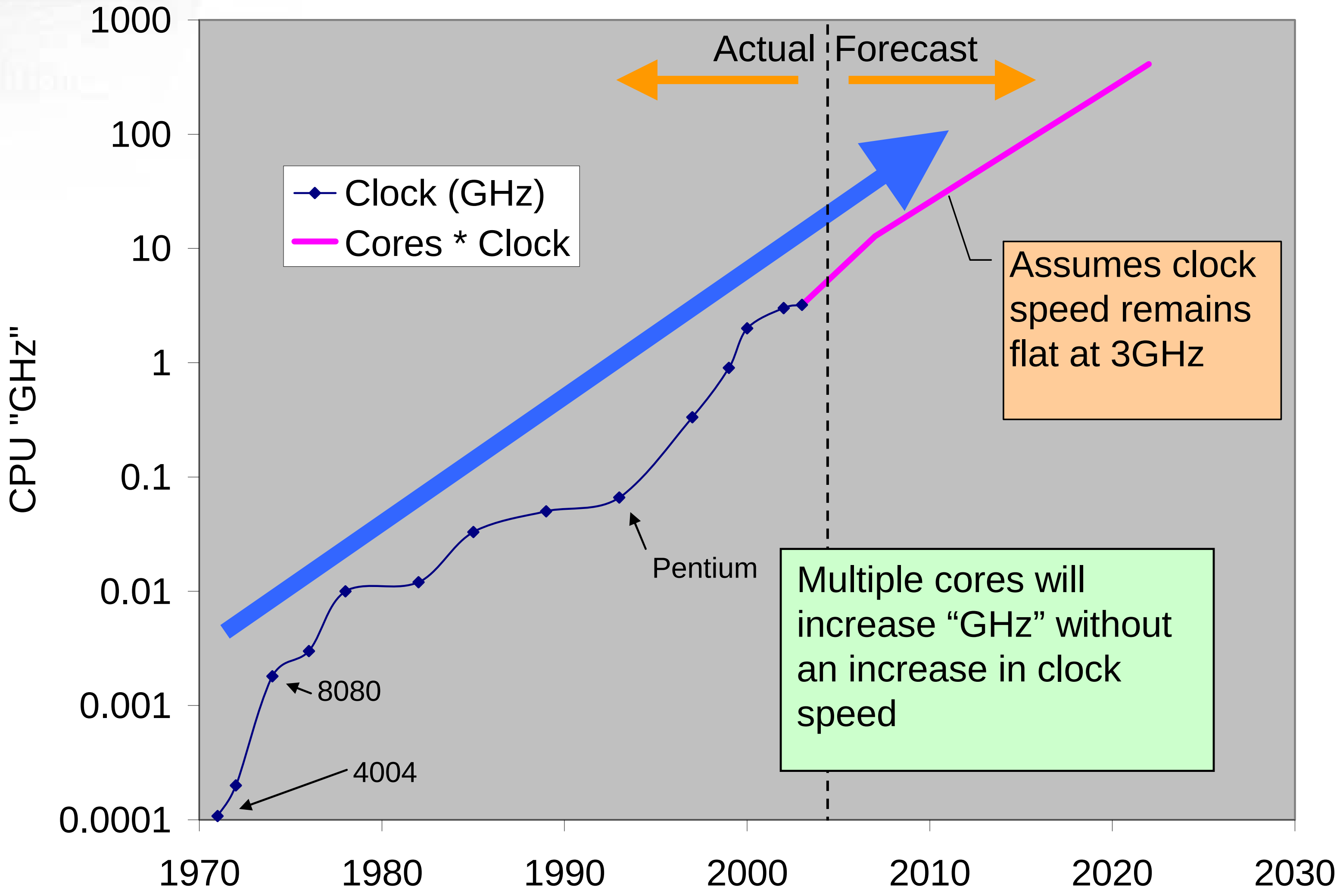


High End Logic

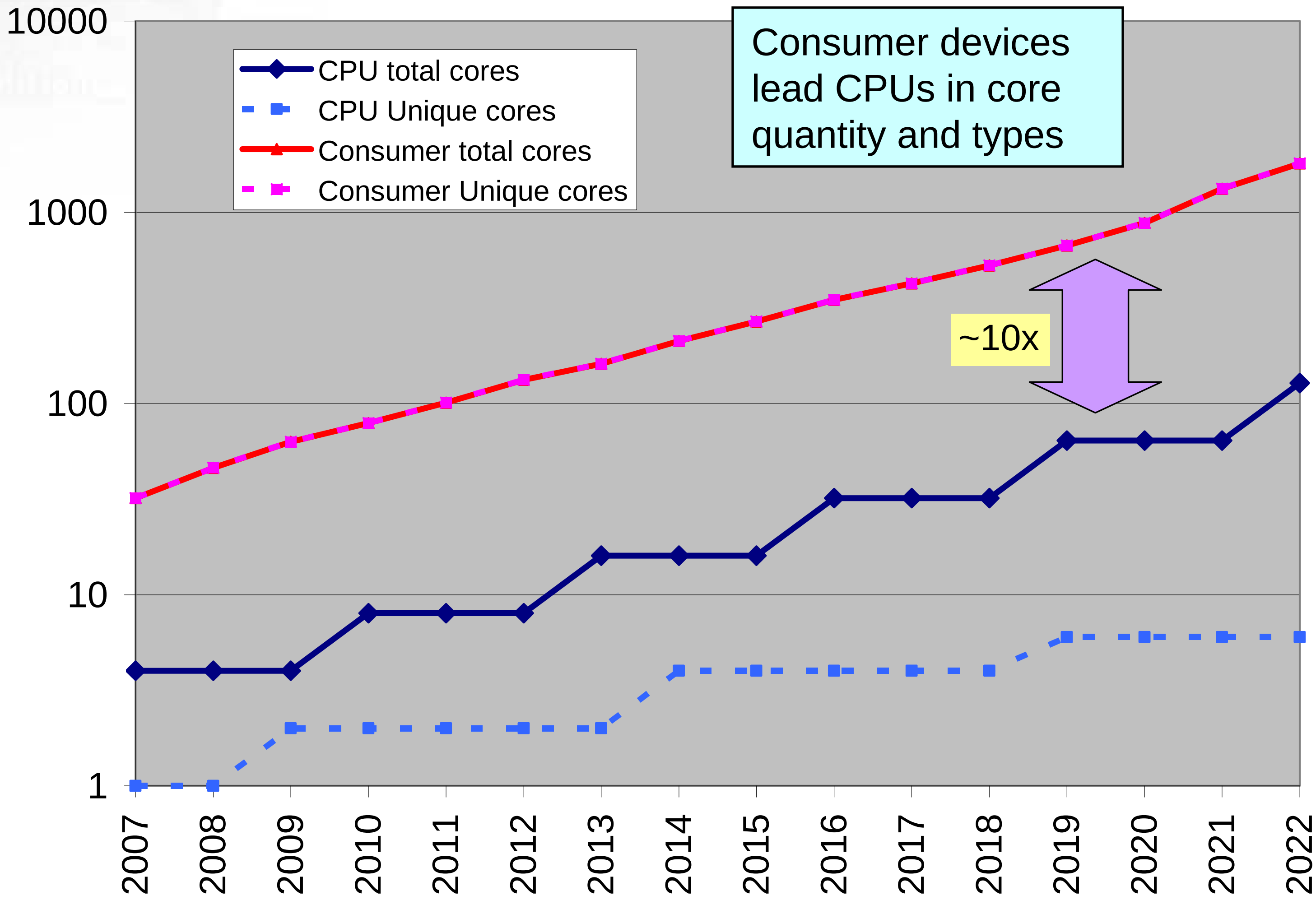
- **Trend: Single to Multi core**
  – Forecast for > 100 cores by 2020
- **I/O GT/s increasing**
  – Aligned to number of cores
  – Multi-lane HS serial to 20GT/s
- **Non-dif I/O will remain below 2 GT/s**
  – Accuracy and noise limitations
- **Structural test at low speed**
  – Vectors increasing with FF count



MPU “GHz” by “Cores”

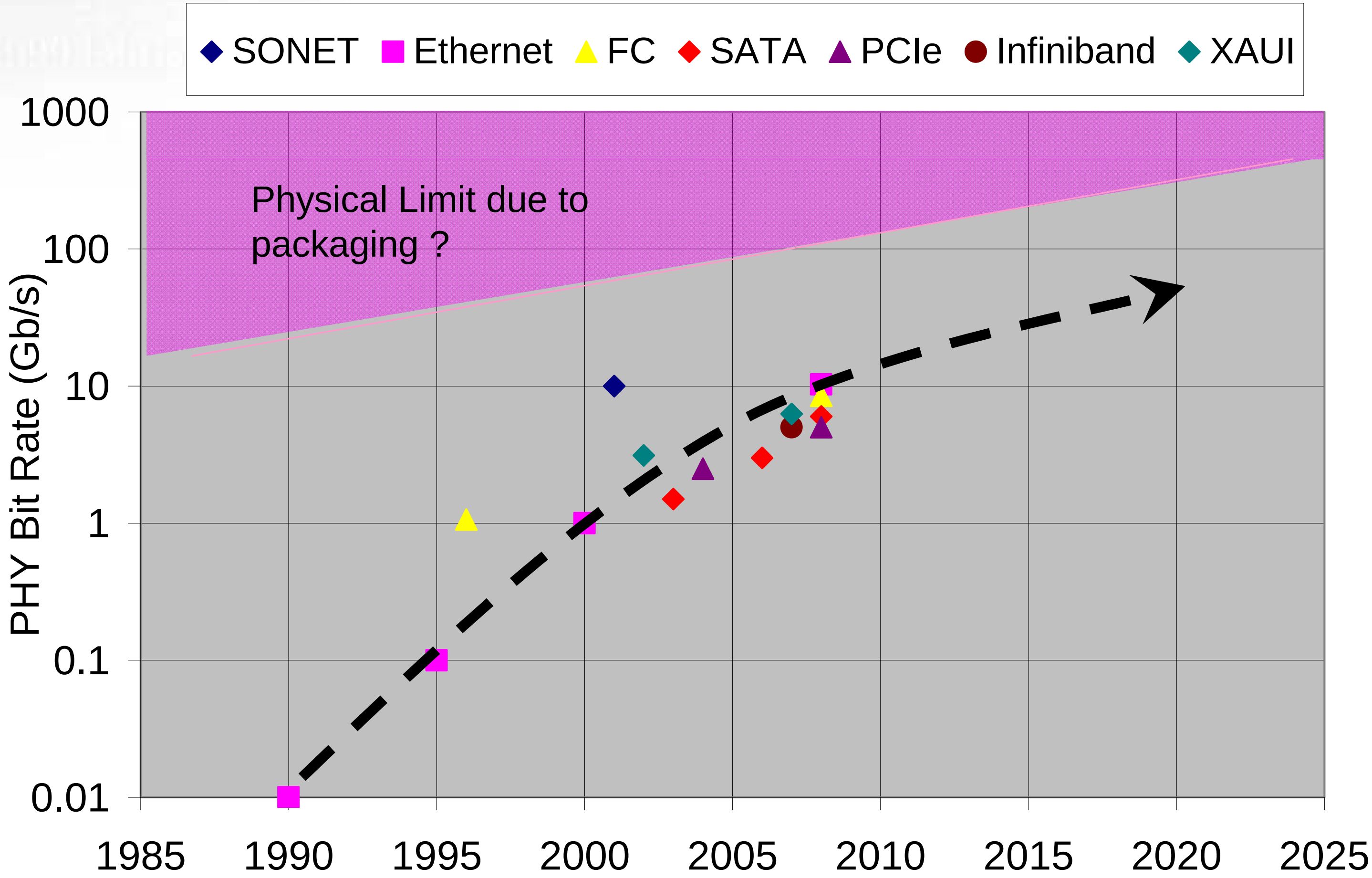


Proliferation of Cores



- **Cores are specialized processors**
  - Graphic, Integer, DSP, task manager, etc

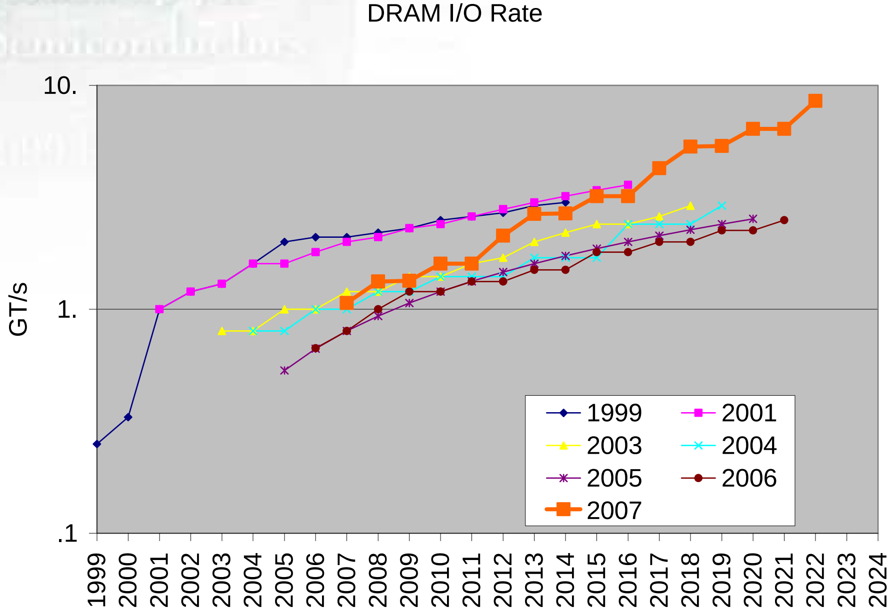
High Speed Interfaces



Test Sockets are not able to support controlled impedance contacts at >15 GT/s

- **Bit bandwidth increasing – Physical limit? Test limit?**

DRAM Model



		single I/O MegaTransitions per second						
	Clk	SDR	DDR	DDR2	DDR3	DDR4	DDR5	DDR6
1997	133	133						
1998	133	133						
1999	166	166						
2000	166	166	266 333					
2001	200		400					
2002	200		400					
2003	266			400 533				
2004	333			666				
2005	333			666				
2006	400			800				
2007	533				800 1066			
2008	666				1333			
2009	666				1333			
2010	800				1600			
2011	800				1600			
2012	1066					1600 2133		
2013	1333					2666		
2014	1333					2666		
2015	1600					3200		
2016	1600					3200		
2017	2133						3200 4266	
2018	2666						5333	
2019	2666						5333	
2020	3200						6400	
2021	3200						6400	
2022	4266							6400 6532

DDR4 thru DDR6 roadmaps are pure speculation

- **Each DDRx family has 3 primary bit rates plus two optional**
  - First two speeds available in intro year
  - Third speed available +1 year (+ half node)
  - Fourth Speed available +3 year (+ 1 litho node)
  - Fifth Speed available +4 year or never (+1.5 litho nodes)
- **xDRX family cycle change**
  - 2000→2007 - 3 years
  - 2007+ - 5 years

RF

Roadmap mm-Wave Tables

0.8 GHz		2 GHz			5 GHz	10 GHz	28 GHz	77 GHz	94 GHz
GSM CDMA ISM	PDC GPS SAT Radio	DCS PCS DECT CDMA	WLAN 802.11b/g Bluetooth ZigBee	SAT TV	WLAN 802.11a	SAT TV WLAN Hyperlink UWB	LMDS WLAN	AUTO Radar	All Weather Landing

Year of Production	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*	*2014*	*2015*	*2016*	*2017*	*2018*	*2019*	*2020*	*2021*	*2022*
Carrier Frequency (GHz) Leading edge	18	18	22	22	60	77	77	95	95	95	95	95	95	95	95	95
Carrier Frequency (GHz) High Volume	6	8	12	12	22	22	36	36	36	36	36	36	36	36	36	36
Modulation RF BW (MHz) Leading edge	80	528	528	528	528	528	528	528	528	528	528	528	1000	1000	1000	1000
Modulation RF BW (MHz) High Volume	20	40	80	528	528	528	528	528	528	528	528	528	528	528	1000	1000
Amplitude Accuracy (dB)	<0.8	<0.6	<0.5	<0.5	<0.5	<0.25	<0.25	<0.25	<0.25	<0.25	<0.25	<0.25	<0.125	<0.125	<0.125	<0.125
ACLR (dB)	65	65	70	72	72	72	75	75	80	80	80	85	85	85	85	85
Number of RF Ports per Device	<9	<12	<16	<20	<24	<20	<18	<16	<16	<16	<16	<16	<16	<16	<16	<16
Phase Noise (dBc/Hz @ 100k offset)	-125	-130	-135	-140	-142	-145	-148	-150	-150	-150	-152	-152	-152	-152	-152	-152
Error Vector Magnitude 3G/4G	1-2%	1-2%	0.5%	0.5%	0.5%	0.5%	0.5%	0.5%	0.5%	0.5%	0.5%	0.5%	0.5%	0.5%	0.5%	0.5%
OIP3 (dBm)	30	30	30	30	30	30	30	30	30	30	30	30	30	30	30	30
IIP3 (dBm)	40	50	60	60	60	60	60	60	60	60	60	60	60	60	60	60

- **High Frequency RF is characterized and sample tested**
- **>50 GHz testing is a roadblock**

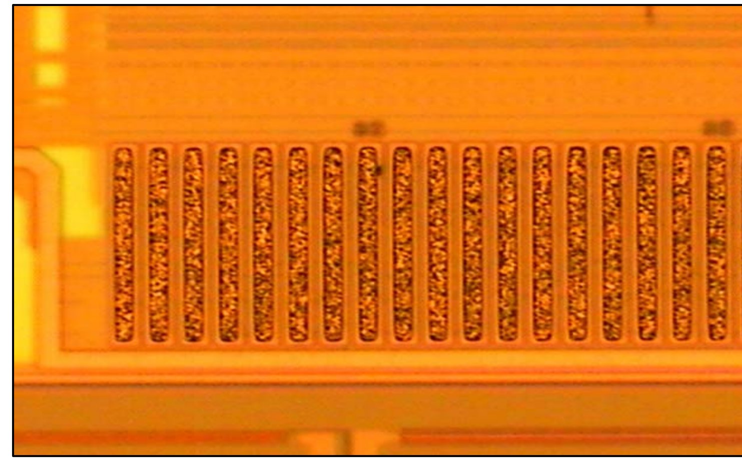
DUT Interface

- **Probe**
  - Wide range of test parallelism
    - High end logic – x1
    - NAND – Full wafer
  - Pad size requirements based on probing area & temp range
  - KGD performance test difficult – interface effects
- **Sockets**
  - Tables added for 2007
    - TSOP – Flash (NAND) – Contact blade
    - BGA – DRAM – Spring Probe
    - BGA – SoC – Spring Probe (50 ohm)
    - BGA – SoC – Conductive Rubber
  - Test limitations for pitch below 0.5mm and frequency > 30GHz

Specialty Devices

1.5x30mm - Linear CCD Image Sensor

- **New 2007 section**
- **Targets non roadmap HVM devices**
- **2007 devices**
  - LCD drivers
    - Form factor of 30mm x 1.5mm
    - Long bond pads on 23um centers
  - Image sensors
    - Micro lens check with pupil test
  - 3 axis MEMS Accelerometer
    - for consumer drop/rotate applications
      - iPhone



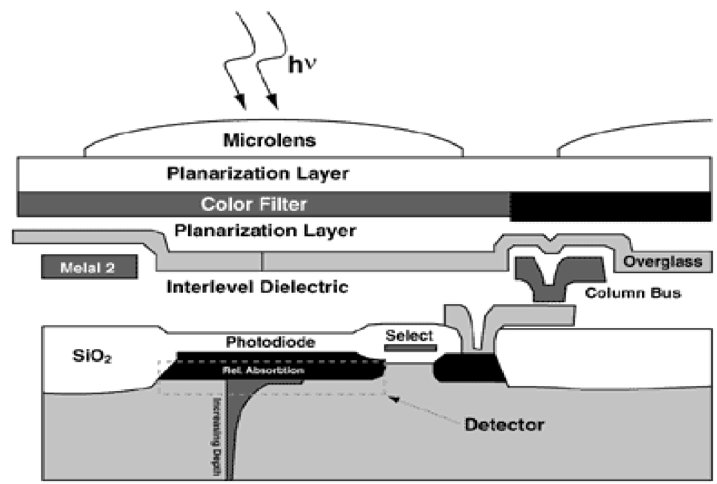


Image sensor structure cross section

2007 Focus and Cross TWG

- **2007 Focus**
  - Simplification of the 2005 message
  - Additions of RF, sockets, and High Speed interfaces
  - Consolidation of Memory, Hander and prober tables
  - Connecting the logic and SoC test model assumptions

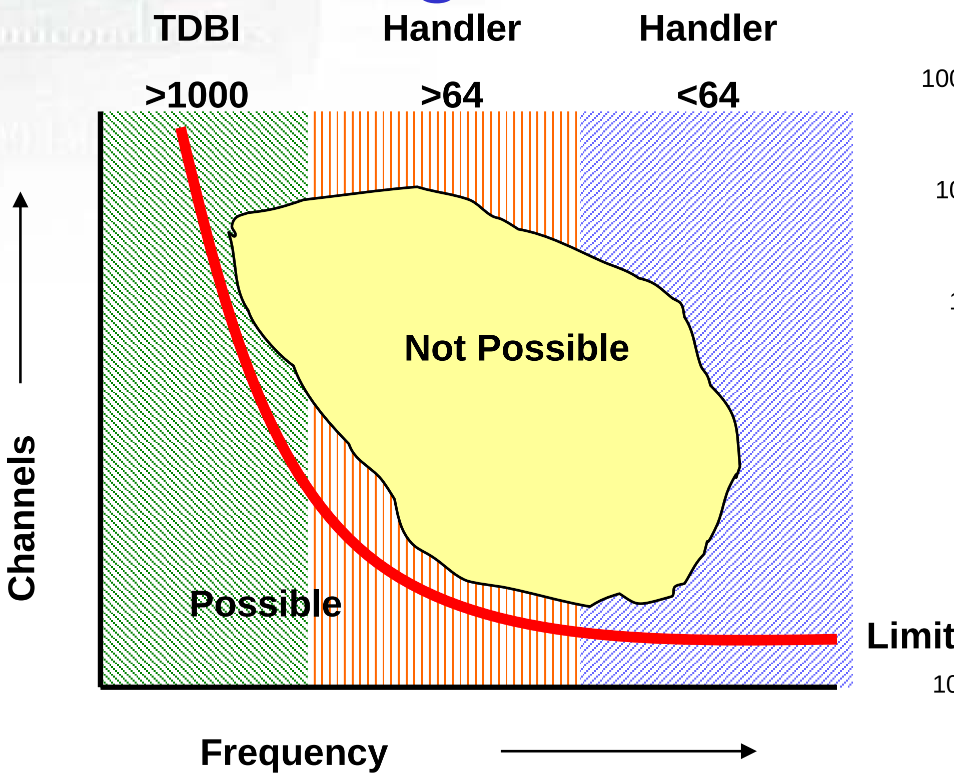
- **Cross TWG**
  - Wireless - Future frequency requirements
  - Assembly/Packaging -TSVs, KGD, pad damage
  - Design - Cores, Memory in MPU and consumer SoC

Summary

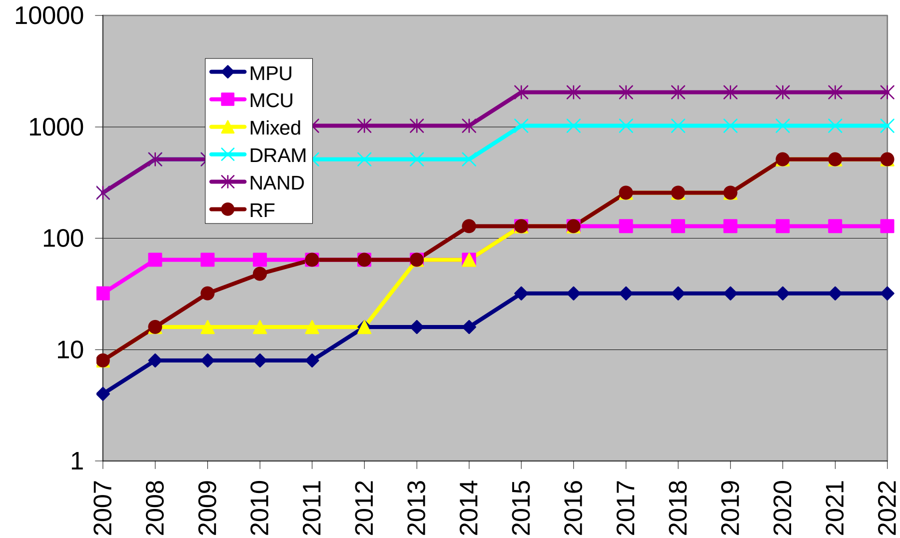
- **Trends**
  - More cores, transistors, bits
  - Higher speed I/O
  - Smaller, lighter and more complex packages
  - 450mm wafers
- **Challenges**
  - Step around the “walls”
  - Continued economic scaling of test
  - Yield learning thru test
  - Dealing with fault tolerant devices

Backup

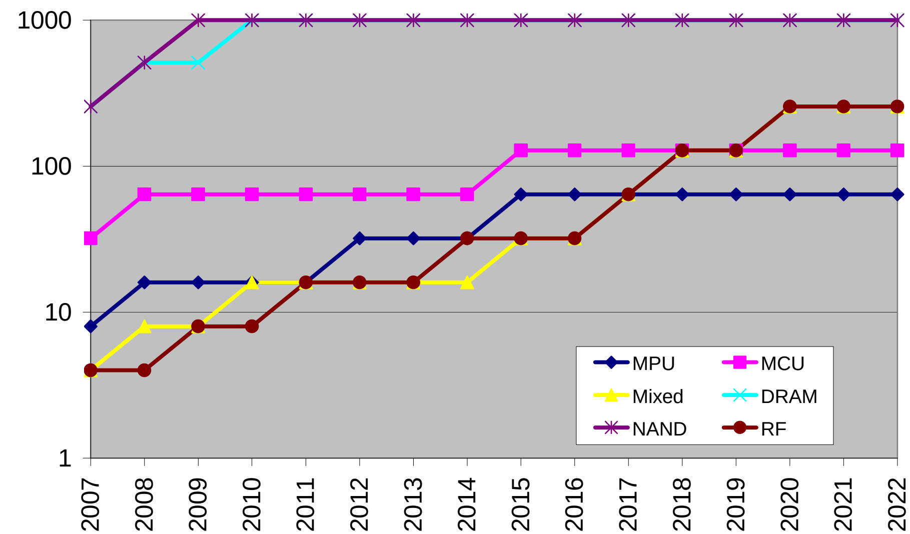
Challenge: Limits to test parallelism



Packaged Test Parallelism



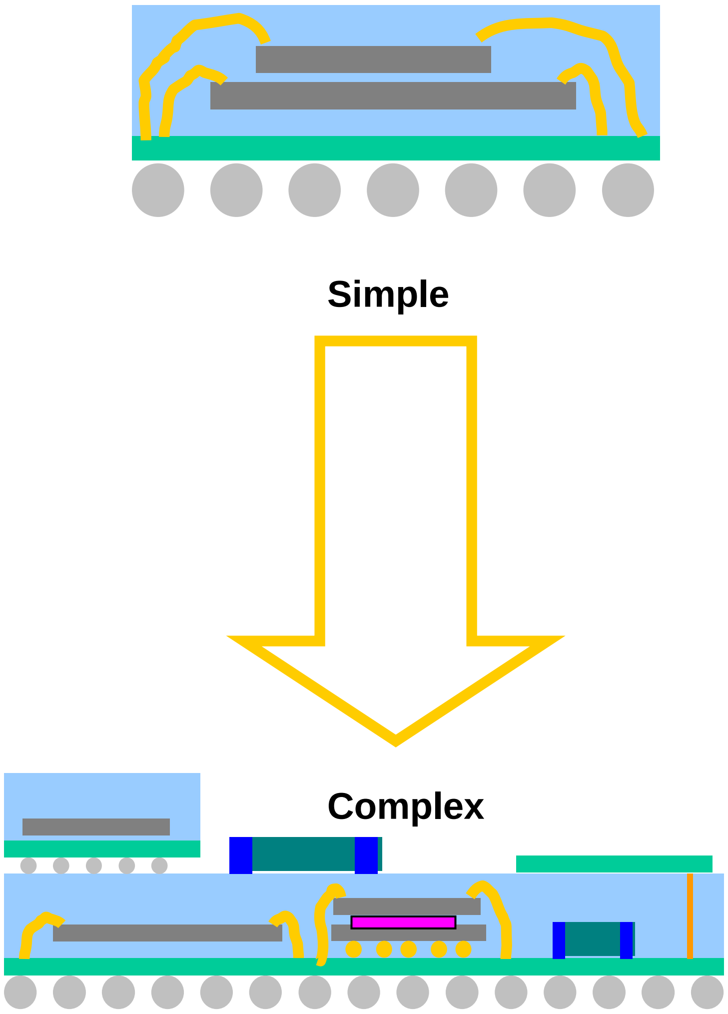
Probe Parallelism



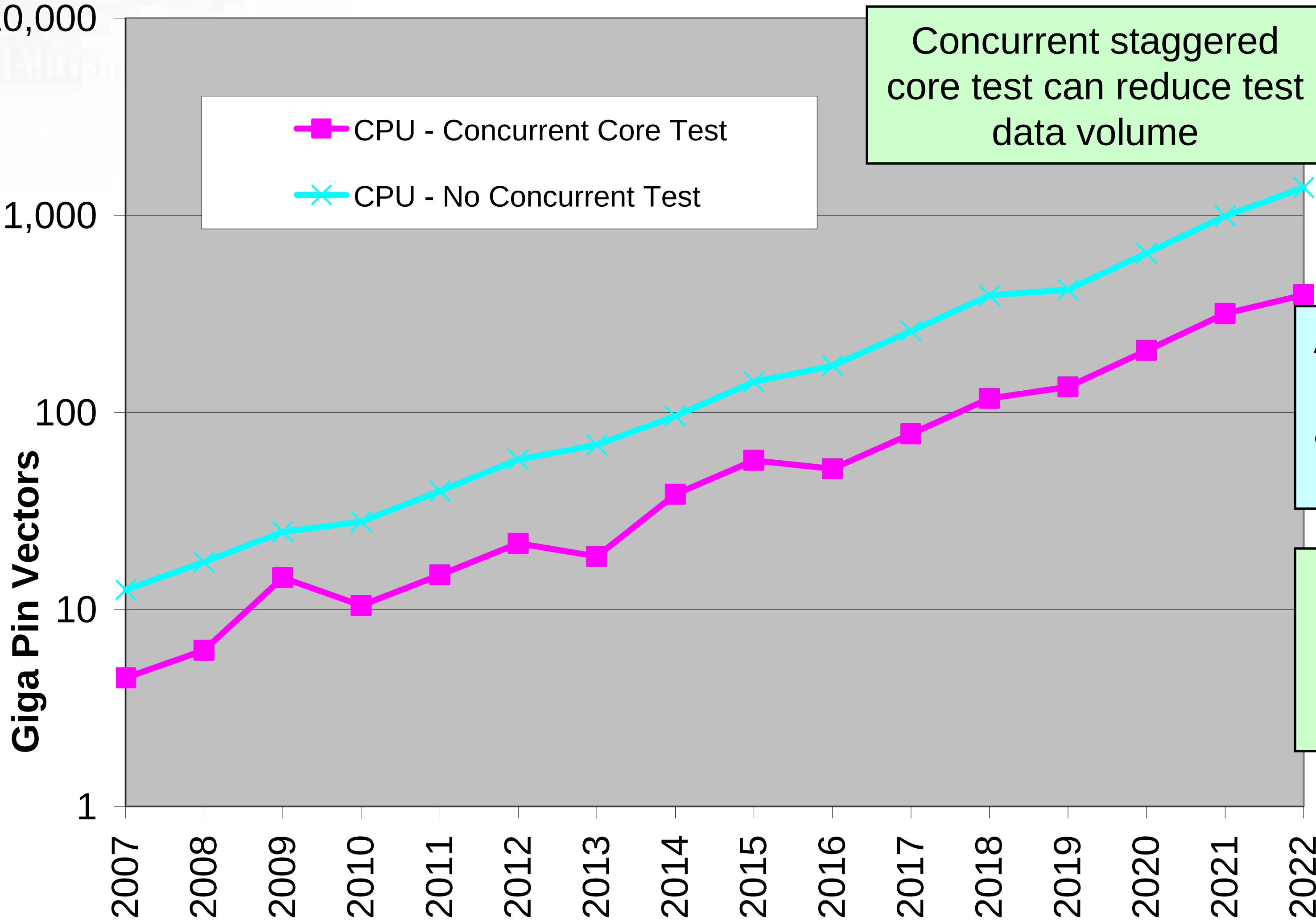
- **Low Frequency: Mechanical - Cables and connections**
- **High Frequency: Electrical - Signal integrity**
- **Parallelism is a function of test time**

SiP

- **Initially “2 chips in a package”**
- **Evolved to “Anything is Possible”**
  - Any Silicon (digital, analog, mixed)
  - Passives
  - Packaged ICs,
  - Other SiP
  - Connectors to top of SiP
- **Complexity**
  - Single test solution not easy
    - Core & connectivity test
    - No implemented test standard
  - More complex SiPs on horizon
    - Optical?



Digital Logic Test Data Volume

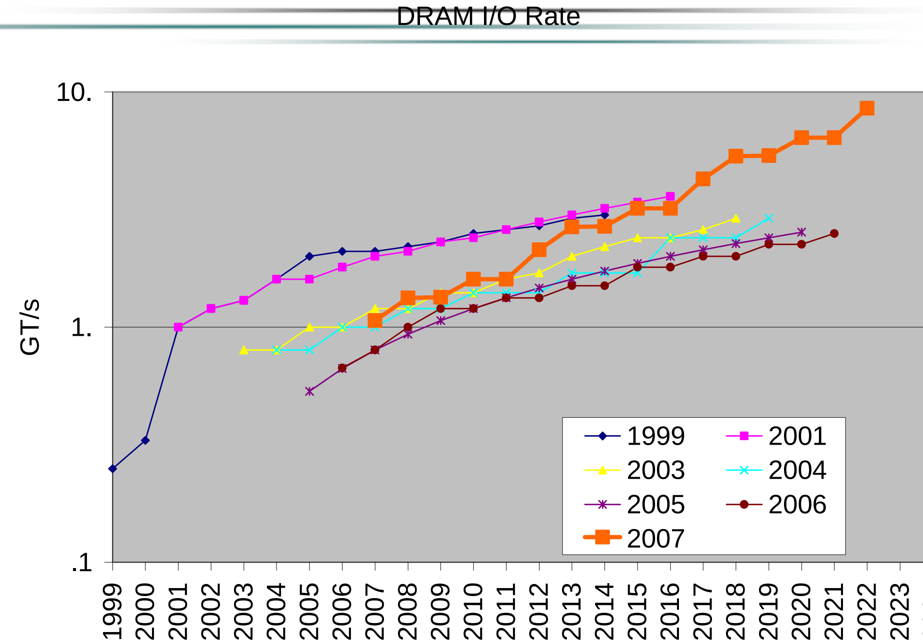


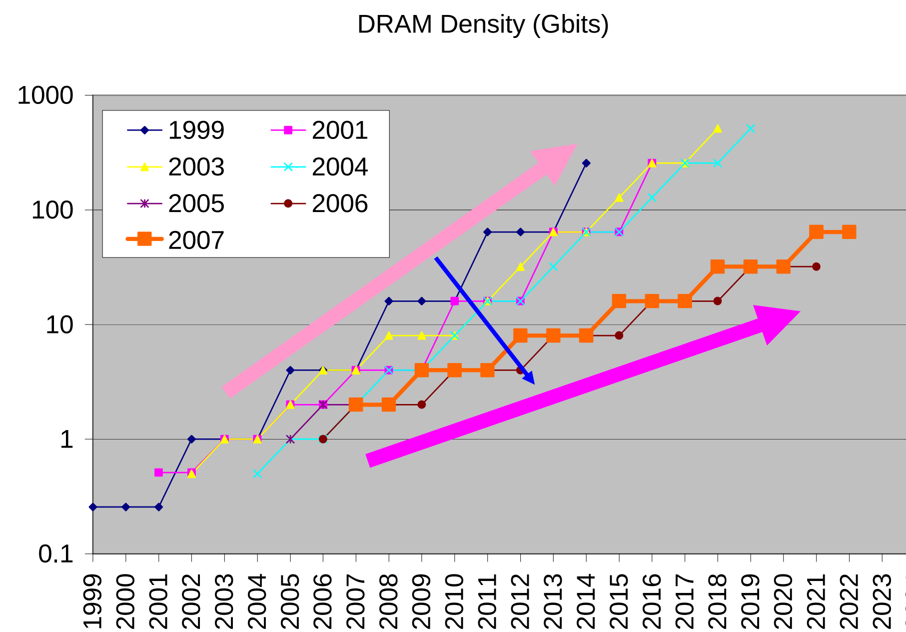
Assumes only identical cores are tested in parallel.

Helps tool reuse by limiting data volume

DRAM Trends
vs. Fcst

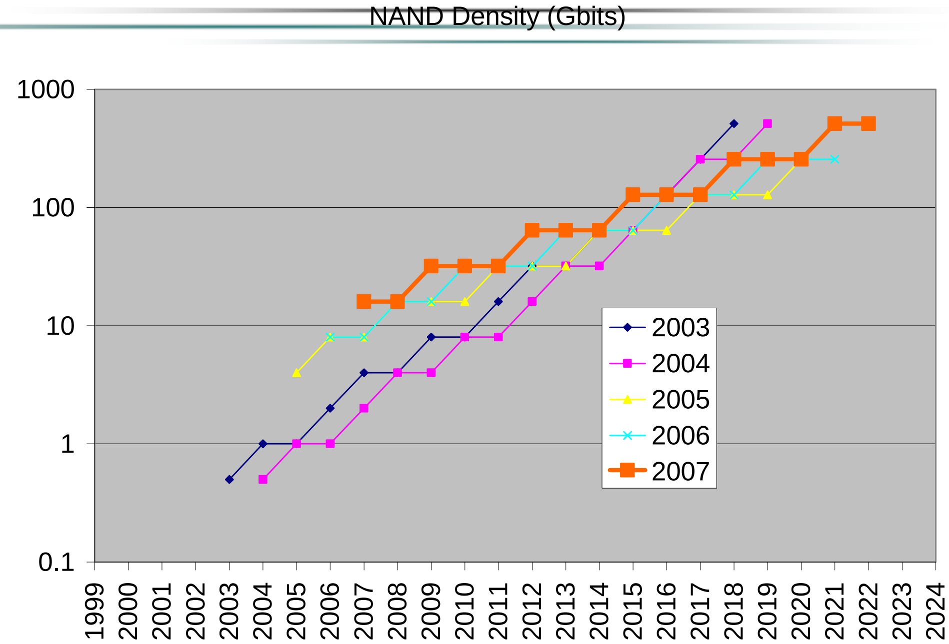
- **Speculative beyond DDR3**
- **Cell size remains $6F^2$**
- **Increased I/O rate in 2007 to support revised DDR4→DDR6 model**
- **Density aligned to litho roadmap**





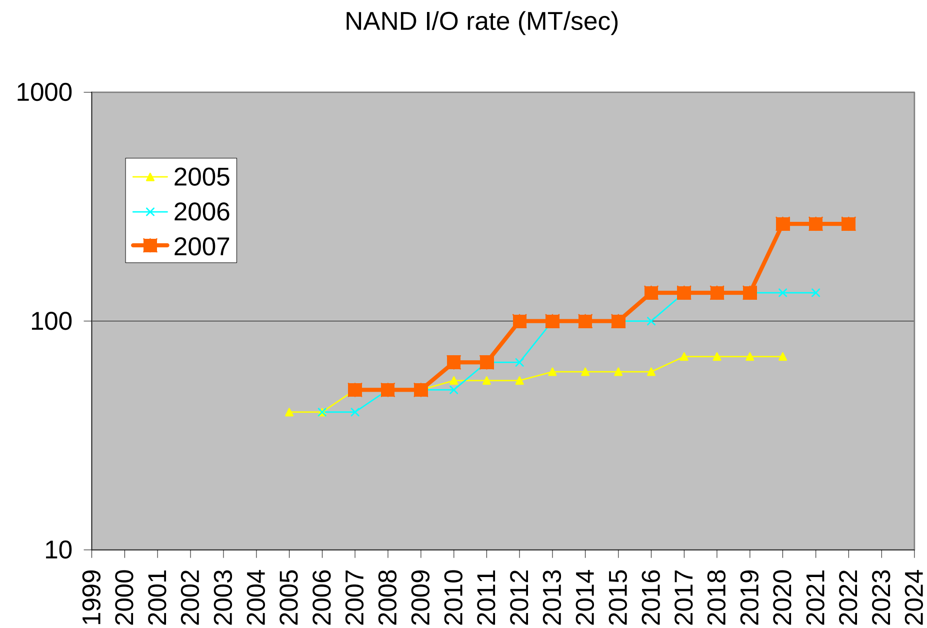
NAND Trends
vs. Fcst

- **Density growth has flattened slightly**
  - Litho has caught up
  - $4F^2$ Cell size (SBC)
  - 3 year Litho trend
  - 2 B/C assumed



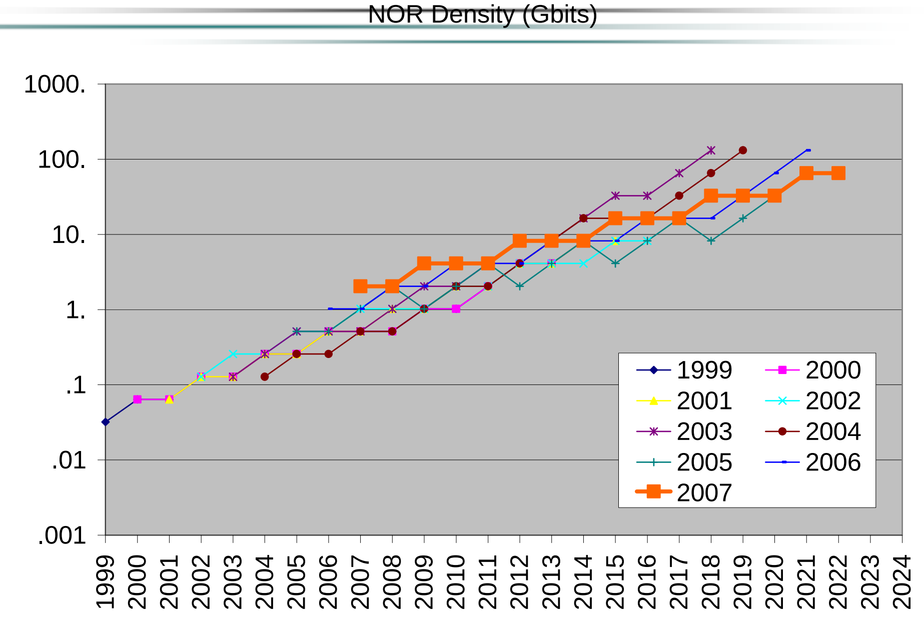
- **I/O MT/s W/R rate driven**

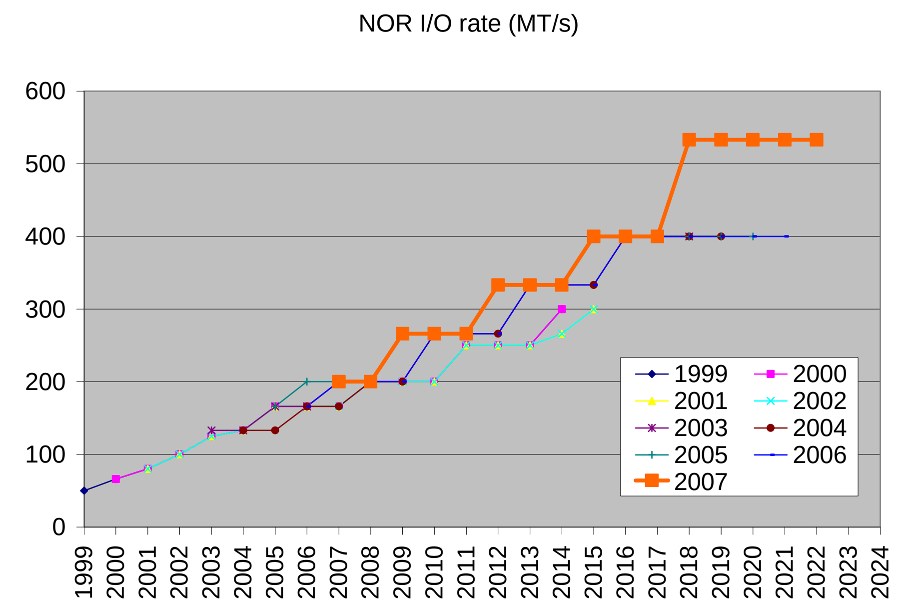
- **ONFI spec**
  - DDR
  - Block Abstraction
  - Common command set



NOR Trends
vs Forecasts

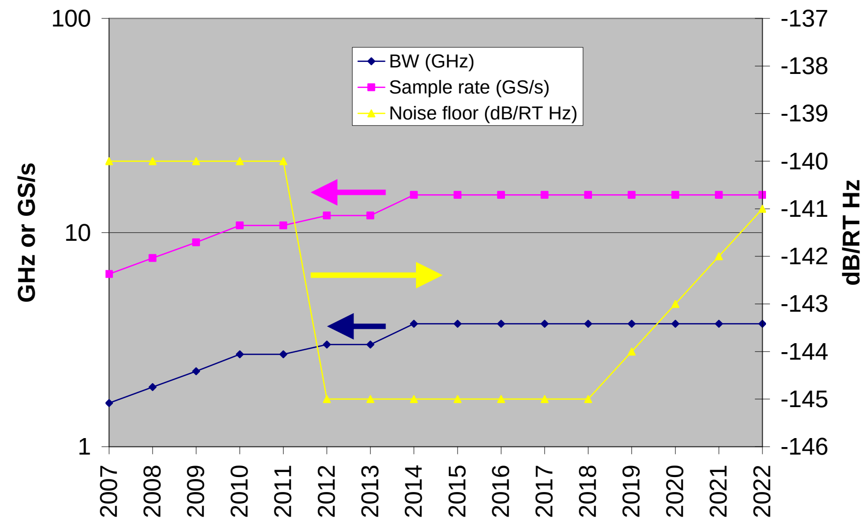
- **I/O rate scaling to Cellular requirements**
- **Density roadmap well known**
  - MLC prior to 1999
- **X32 data has not appeared**
  - Forecasting for 2012?





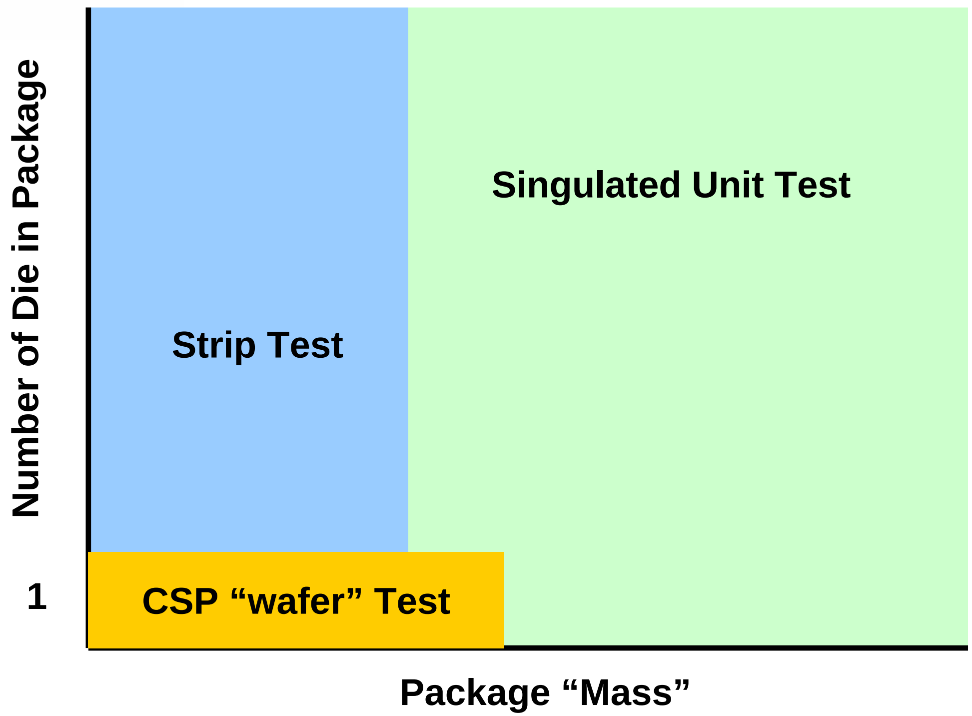
Mixed Signal

- **Small changes from 2005**
  - Noise floor flattened
  - Sampling rate increased



	2007	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*	*2014*	*2015*	*2016*	*2017*	*2018*	*2019*	*2020*	*2021*	*2022*
Low Frequency Waveform																
BW (MHz)	**50**	**75**	**75**	**75**	**100**	**100**	**100**	**100**	**100**	**100**	**100**	**100**	**100**	**100**	**100**	**100**
Sample rate (MS/s)	**Moving from Nyquist sample rates to over/under sampling sources/digitizers**															
Resolution (bits)	**DSP computation to 24 bits, effective number of bits limited by noise floor**															
Noise floor (dB/RT Hz)	**-155**	**-160**	**-160**	**-160**	**-165**	**-165**	**-165**	**-165**	**-165**	**-165**	**-165**	**-165**	**-165**	**-165**	**-165**	**-165**
Very High Frequency Waveform Source																
Level V (pk–pk)	**4**	**4**	**<4**	**<4**	**<4**	**<4**	**<4**	**<4**	**<4**	**<4**	**<4**	**<4**	**<4**	**<4**	**<4**	**<4**
Accuracy (±)	**0.50%**	**0.50%**	**0.50%**	**0.50%**	**0.50%**	**0.50%**	**0.50%**	**0.50%**	**0.50%**	**0.50%**	**0.50%**	**0.50%**	**0.50%**	**0.50%**	**0.50%**	**0.50%**
BW (GHz)	**1.6**	**1.9**	**2.25**	**2.7**	**2.7**	**3**	**3**	**3.75**	**3.75**	**3.75**	**3.75**	**3.75**	**3.75**	**3.75**	**3.75**	**3.75**
Sample rate (GS/s)	**6.4**	**7.6**	**9**	**10.8**	**11**	**12**	**12**	**15**	**15**	**15**	**15**	**15**	**15**	**15**	**15**	**15**
Resolution (bits) AWG/Sine†	**8/10**	**8/10**	**8/10**	**8/10**	**8/10**	**10/12**	**10/12**	**10/12**	**10/12**	**10/12**	**10/12**	**10/12**	**10/12**	**10/12**	**10/13**	**10/14**
Noise floor (dB/RT Hz)	**-140**	**-140**	**-140**	**-140**	**-140**	**-145**	**-145**	**-145**	**-145**	**-145**	**-145**	**-145**	**-145**	**-145**	**-145**	**-145**
Very High Frequency Waveform Digitizer																
Level V (pk–pk)	**4**	**4**	**<4**	**<4**	**<4**	**<4**	**<4**	**<4**	**<4**	**<4**	**<4**	**<4**	**<4**	**<4**	**<4**	**<4**
Accuracy (±)	**0.50%**	**0.50%**	**0.50%**	**0.50%**	**0.50%**	**0.50%**	**0.50%**	**0.50%**	**0.50%**	**0.50%**	**0.50%**	**0.50%**	**0.50%**	**0.50%**	**0.50%**	**0.50%**
BW (GHz) (under sampled)	**9.2**	**10.8**	**10.8**	**12.5**	**12.5**	**15**	**15**	**15**	**15**	**15**	**15**	**15**	**15**	**15**	**15**	**15**
Sample rate (GS/s)	**0.4**	**0.4**	**0.4**	**0.4**	**0.4**	**0.6**	**0.6**	**0.6**	**0.6**	**0.6**	**0.6**	**0.6**	**0.6**	**0.6**	**0.6**	**0.6**
Min resolution (bits)	**12**	**12**	**12**	**12**	**12**	**14**	**14**	**14**	**14**	**14**	**14**	**14**	**14**	**14**	**14**	**14**
Noise floor (dB/RT Hz)	**-145**	**-145**	**-145**	**-145**	**-145**	**-150**	**-150**	**-150**	**-150**	**-150**	**-150**	**-150**	**-150**	**-150**	**-150**	**-150**
Time Measurement																
Jitter measurement (ps RMS)	**Will be driven by high-speed serial communication ports**							**Will be driven by high-speed serial communication ports**								
Frequency measurement (MHz)	**Will be driven by high-performance ASIC clock rates**							**Will be driven by high-performance ASIC clock rates**								
Single shot time capability (ps)	**Will be driven by high-speed serial communication ports**							**Will be driven by high-speed serial communication ports**								

Package Size & Test



Package roadmap supports 0.2mm thickness

Singulated Unit test appears to have limits based on mass

Mechanical

- **Single Prober Roadmap**
  - 450mm wafers assumed in 2014

Year of Production	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*	*2014*	*2015*	*2016*	*2017*	*2018*	*2019*	*2020*	*2021*	*2022*
Wafer diameter (mm)	300	300	300	300	300	300	300	450	450	450	450	450	450	450	450	450
Wafer thickness (um)	80–775	80–775	80–775	80–775	80–775	80–775	80–775	50–1000	50–1000	50–1000	50–1000	50–1000	50–1000	50–1000	50–1000	50–1000
Maximum I/O pads	3000	4000	4000	5300	5300	5300	5300	5300	5300	5300	5300	5300	5300	5300	5300	5300
Chuck X & Y positioning accuracy (um)	2	2	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Chuck Z positioning accuracy (um)	1	1	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5
Probe-to-pad alignment (μm)	4.5	4.5	4.5	3.5	3.5	3.5	3.5	3.5	3.5	3.5	3.5	3.5	3.5	3.5	3.5	3.5
Maximum chuck force (kg)	100	100	100	100	100	100	100	100	100	100	100	100	100	100	100	100
Set point range (ºC)	-30 to +85	-30 to +85	-30 to +85	-45 to +125	-45 to +125	-45 to +125	-45 to +125	-45 to +125	-45 to +125	-45 to +125	-45 to +125	-45 to +125	-45 to +125	-45 to +125	-45 to +125	-45 to +125
Total power (Watts)	130	130	250	250	250	250	250	250	250	250	250	250	250	250	250	250
Power density (Watt/cm^2)	60	60	120	120	120	120	120	120	120	120	120	120	120	120	120	120

- **Three handler groups**
  - High power - > 10W
    - Low parallelism: < 4
  - Medium Power → 0.5 to 10W
    - Medium parallelism: < 16
  - Low Power → < 0.5W (Memory, MCU, etc)
    - High parallelism: <250