2007 Litho ITRS Update

Lithography iTWG

July 2007

Outline

- Lithography Potential Solutions
- Variability Control
- Double Exposure

Planned 2007 Update

DRAM 1/2 Pitch	2010	2013	2016	2019
	2008 2009	2011 2012	2014 2015	2017 2018 / 2020 2021
65nm	45nm	32nm	22nm	16nm

65 — 193 nm; 193 nm immersion with water

45 — 193 nm immersion with water; 193 nm immersion double patterning; 193 nm immersion with other fluids; EUV, ML2

32 — EUV; 193 nm immersion double pattern; 193 nm immersion with ...; ML2, Imprint

22 — EUV; Innovative 193 nm immersion; ML2, imprint, innovative technology

16 — Innovative technology; Innovative EUV, ML2, imprint

Narrow options

Flash Half-pitch

> 193nm immersion with water
> 193nm immersion double exposure / patterning

> 193nm immersion double exposure / patterning
> EUVL
> 193i+
> ML2, Imprint

> Add Directed Self-Assembly

Research Required | Development Underway | Qualification/Pre-Production | Continuous Improvement

This legend indicates the time during which research, development, and qualification/pre-production should be taking place for the solution.

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Preferred Technology by Year

2006 SEMATECH Litho Forum survey results

Percentage of Votes

70%
60%
50%
40%
30%
20%
10%
0%

2009
45nm HP

2012
32nm HP

2015
22nm HP

- 193 dry SE
- 193i SE
- 193/193i DE
- 193i+
- EUVL
- EPL
- Nanoimprint
- Maskless

193nm Litho – Numerical Aperture

Year	2007	2008	2009	2010	2011	2012	2013	2014	2015
DRAM HP	65	57	50	45	40	36	32	28	25
NA required for memory (single exposure)	**1.01**	**1.20**	**1.35**	**1.52**	**1.70**	**1.91**	**2.14**	**2.41**	**2.70**
NA required for logic (single exposure)	**0.91**	**1.04**	**1.20**	**1.38**	**1.54**	**1.73**	**1.94**	**2.18**	**2.45**
NA required for double exposure (memory)	**0.72**	**0.86**	**0.96**	**1.08**	**1.22**	**1.36**	**1.53**	**1.72**	**1.93**
NA required for double exposure (logic)	**0.62**	**0.72**	**0.82**	**0.95**	**1.06**	**1.19**	**1.34**	**1.50**	**1.68**

Memory k1=0.28, Logic k1=0.32, Double exposure k1=0.2
Fluid index scaling assumes 0.93NA highest for air

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Lithography Technology Requirements

Year of Production	*2007*	*2010*	*2013*	*2016*	*2019*	*2022*
DRAM ½ pitch (nm) (contacted)	**65**	**45**	**32**	**22**	**16**	**11**
DRAM and Flash						
DRAM ½ pitch (nm)	**65**	**45**	**32**	**23**	**16**	**11**
Flash ½ pitch (nm) (un-contacted poly)	**54**	**36**	**25**	**18**	**13**	**9**
Contact in resist (nm)	**70**	**50**	**35**	**25**	**18**	**12.4**
Contact after etch (nm)	**64**	**45**	**32**	**23**	**16**	**11.3**
Overlay [A] (3 sigma) (nm)	**13**	**9.0**	**6.4**	**4.5**	**3.2**	**2.3**
CD control (3 sigma) (nm) [B]	**6.8**	**4.7**	**3.3**	**2.3**	**1.7**	**1.2**
MPU						
MPU/ASIC Metal 1 (M1) ½ pitch (nm)	**68**	**45**	**32**	**23**	**16**	**11**
MPU gate in resist (nm)	**42**	**30**	**21**	**15**	**11**	**8**
*MPU physical gate length (nm) **	**25**	**18**	**13**	**9**	**6**	**4**
Contact in resist (nm)	**84**	**56**	**39**	**28**	**20**	**14**
Contact after etch (nm)	**77**	**51**	**36**	**25**	**18**	**13**
*Gate CD control (3 sigma) (nm) [B] ***	**2.6**	**1.9**	**1.3**	**0.9**	**0.7**	**0.5**

Lithography Roadmap

90
80
70
60
50
40
30
20
10
0

Half-pitch (nm)

DRAM HP
CDU gate
Overlay

Variability

Pitch

14
12
10
8
6
4
2
0

CD Uniformity / Overlay (nm)

2005 2010 2015 2020

Year

Roadmap Scaling

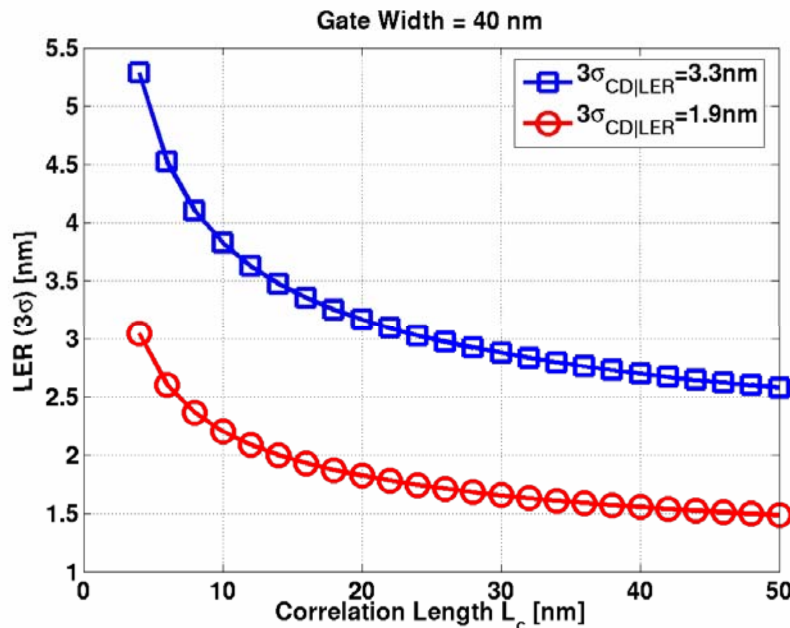
- Pitch
- Variability

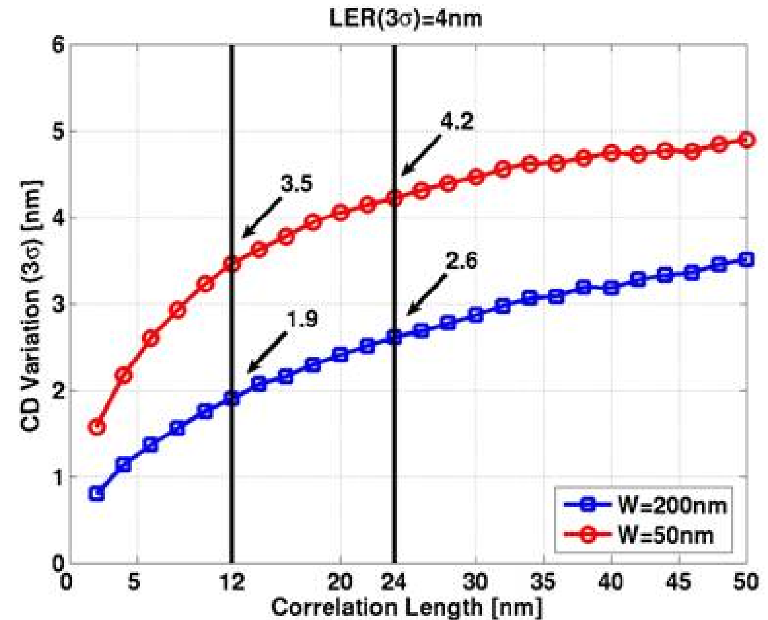
CDU Uniformity

- Literature reports have demonstrated CDU ~1.3nm (3σ)
  - One wafer, in resist, one pitch, one orientation, excluding mask error
  - This is not the ITRS definition
- Contributions to add to match ITRS value:
  - Mask variation, OPC non-correctable error, Wafer-to-wafer, Lot-to-lot, Multiple orientations
- Estimate: Total CDU from adding other components is ~3.2nm
  - Minor change in achievable CDU
  - Gate CDU requirement remains red in near-term years
  - There is no known solution for the broad definition of all CD uniformity components
- Gate CD Uniformity target is 12% of final etched gate size

LER/LWR Requirement

- LER drives an additional component of CD Uniformity
  - AMD paper
    - "Line Edge Roughness Impact on Critical Dimension Variation," Yuangsheng Ma et al, SPIE 2007
- CD variation increases with smaller gate width
- Required LWR/CD decreases with node





Overlay

- Overlay: 20% of DRAM half-pitch (not Flash)
  - DRAM drives overlay more so than flash
  - Accelerated Flash schedule would affect ability to hit overlay
  - Note: most CDU values are driven by tightest half-pitch (flash)

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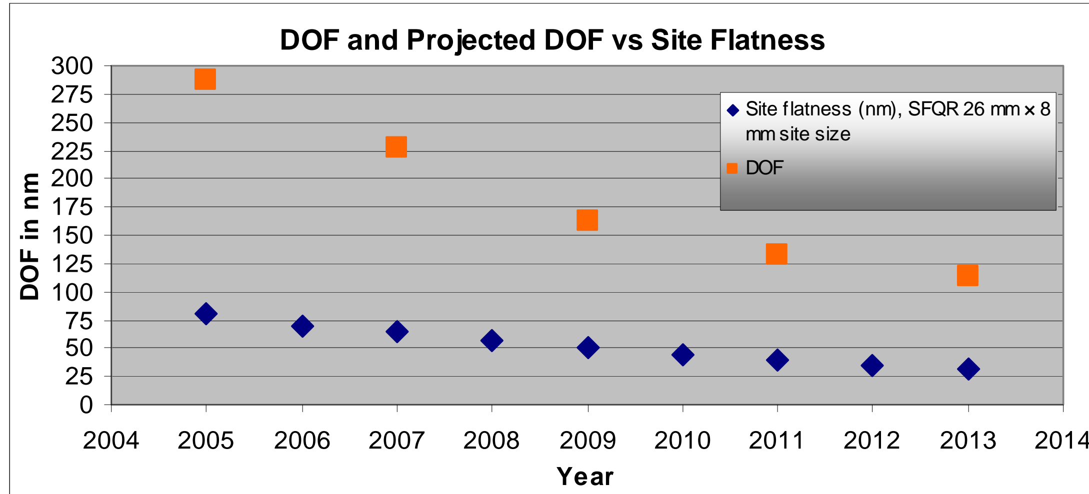
Wafer Flatness Requirement

- 193i at high NA has small DoF
- Need requirement for post-CMP, chucked wafer flatness over 26x10mm scan slit size
  - Only roadmap number today is a bare wafer site flatness requirement



Year of Production	2005	2006	2007	2008	2009	2010	2011	2012	2013
Site flatness (nm), SFQR 26 mm × 8 mm site size	80	70	65	57	45	42	36	35	32
New Site Flatness Targets	80	70	63	54	50	45	40	32	29

2007 Update 193DE/DP

Optical Mask Requirements	*2006*	*2007*	*2010*	*2013*
DRAM HP (nm)	*70*	*65*	*45*	*32*
Image placement for double patterning	**5.7**	**4.9**	**3.4**	**2.4**
Difference in CD Mean-to-target for two masks as a double patterning set	**2.8**	**2.6**	**1.8**	**1.3**
Dual line: mask image placement	**2.5**	**2.3**	**1.6**	**1.2**
Dual line: mask CD 3s	**2.5**	**2.3**	**1.6**	**1.2**
Dual space: repeatability and uniformity of etch bias for double patterning	**1.6**	**1.4**	**1.0**	**0.7**
Spacer PEE process: thickness deviation of deposited layer	To be determined			
Spacer PEE process: thickness uniformity of deposited layer				

Footnote: generic case covers dual space double exposure and patterning but not dual line

Double Exposure

- Simple double exposure: each feature is exposed independently (2006 ITRS)
  - Mask placement tightens by 70%
  - Mean-to-target of mask sets must be matched to within MTT/2
- Defining spaces by dual space exposure (dual space/trench) or defining lines by dual line exposure
  - Adds etch bias uniformity / repeatability
- Defining spaces by dual line exposure or lines by dual space exposure
  - CD of resulting features defined by overlap of two exposures
  - Mask image placement tightens
  - Mask CD 3σ tightens

Double Patterning Figures

Dual Trench

Mask 1

Print trenches and etch hardmask

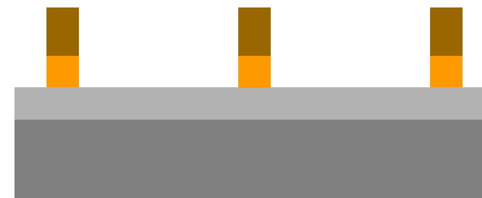
Mask 2

Strip first resist and coat and expose second resist

Etch hardmask and strip second resist

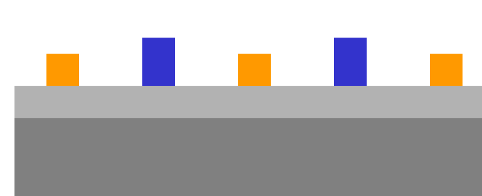
Dual Line

Mask 1



Print trenches and etch hardmask

Mask 2



Strip first resist and coat and expose second resist

Etch hardmask and strip second resist

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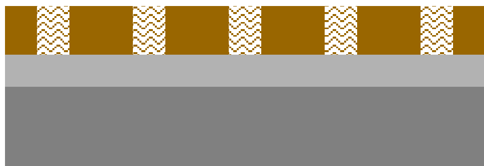
Double Exposure Figures

Dual Trench

Mask 1

Expose trenches

Mask 2

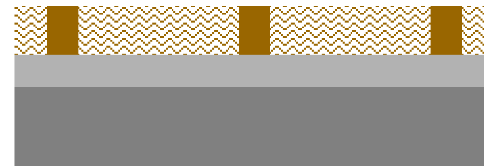


Expose trenches

Develop and etch

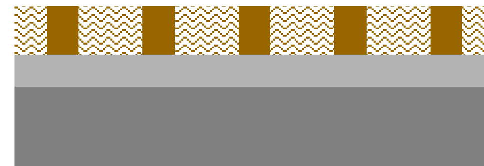
Dual Line

Mask 1

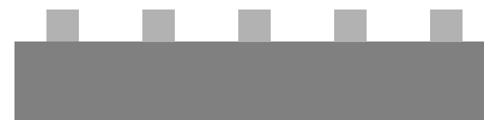


Expose lines

Mask 2



Expose lines



Develop and etch

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Summary

- Lithography potential solutions are being narrowed for 45nm DRAM half-pitch
  - 2008 update will be major decision point for 32nm DRAM half-pitch
- Variability control is becoming one of the largest roadmap concerns
  - No known solutions for gate CD uniformity and Line Width Roughness control
- Double exposure / patterning requires a complex set of parameters when different exposures are used to define single features

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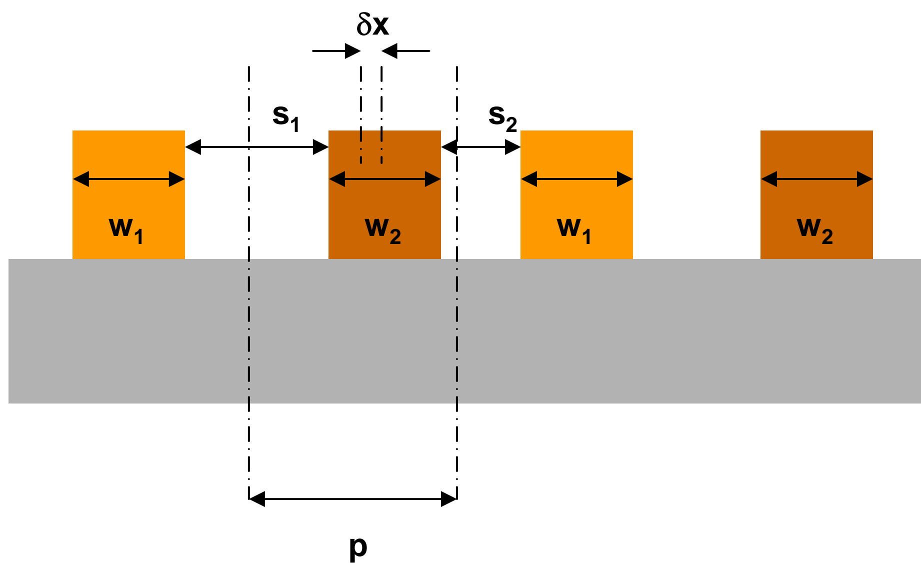
δx
s1
s2
w1
w2
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