

Metrology Roadmap

2007



Metrology Roadmap

7-07 & 4-07

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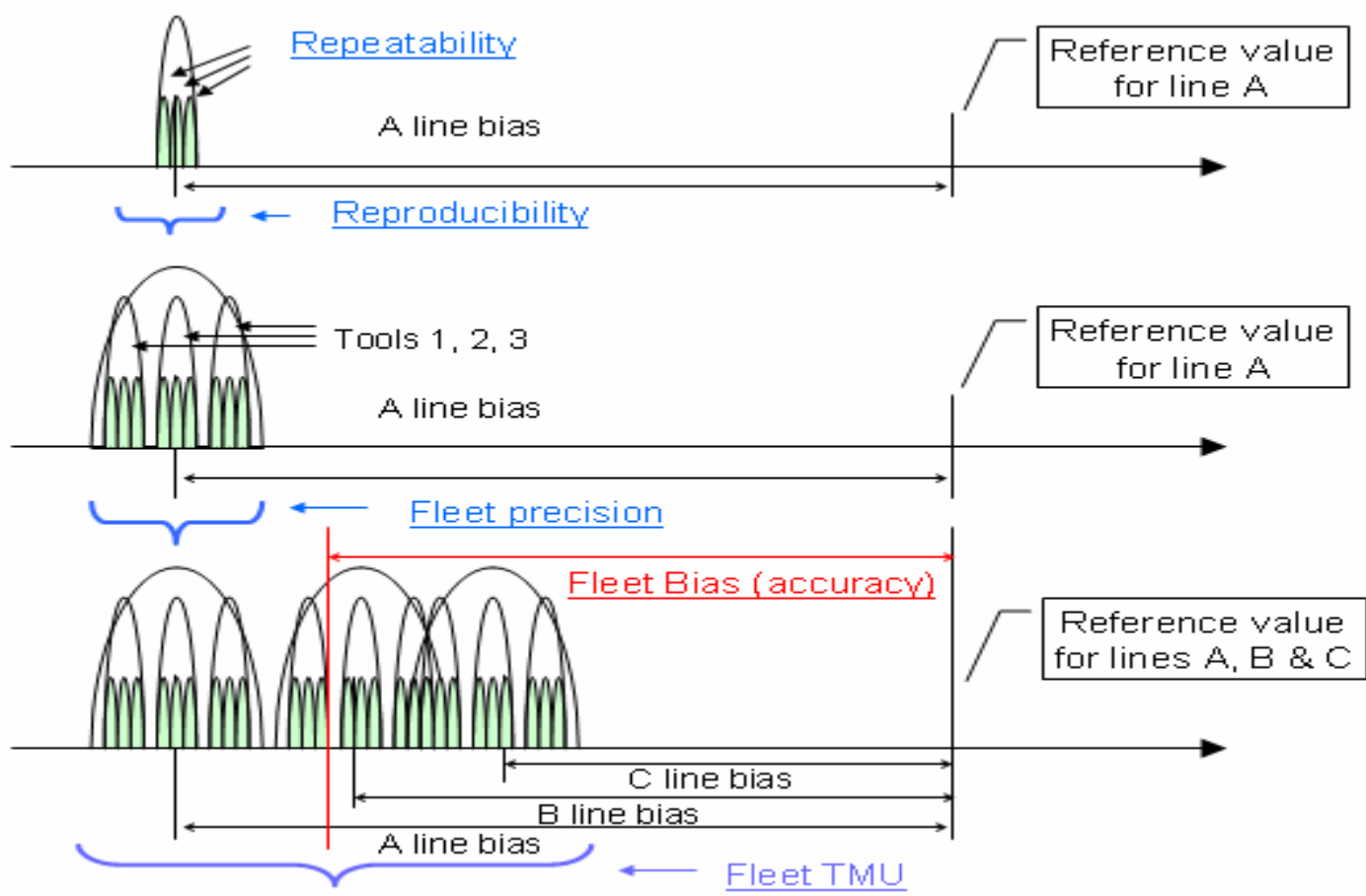
Victor Vartanian (ISMI)



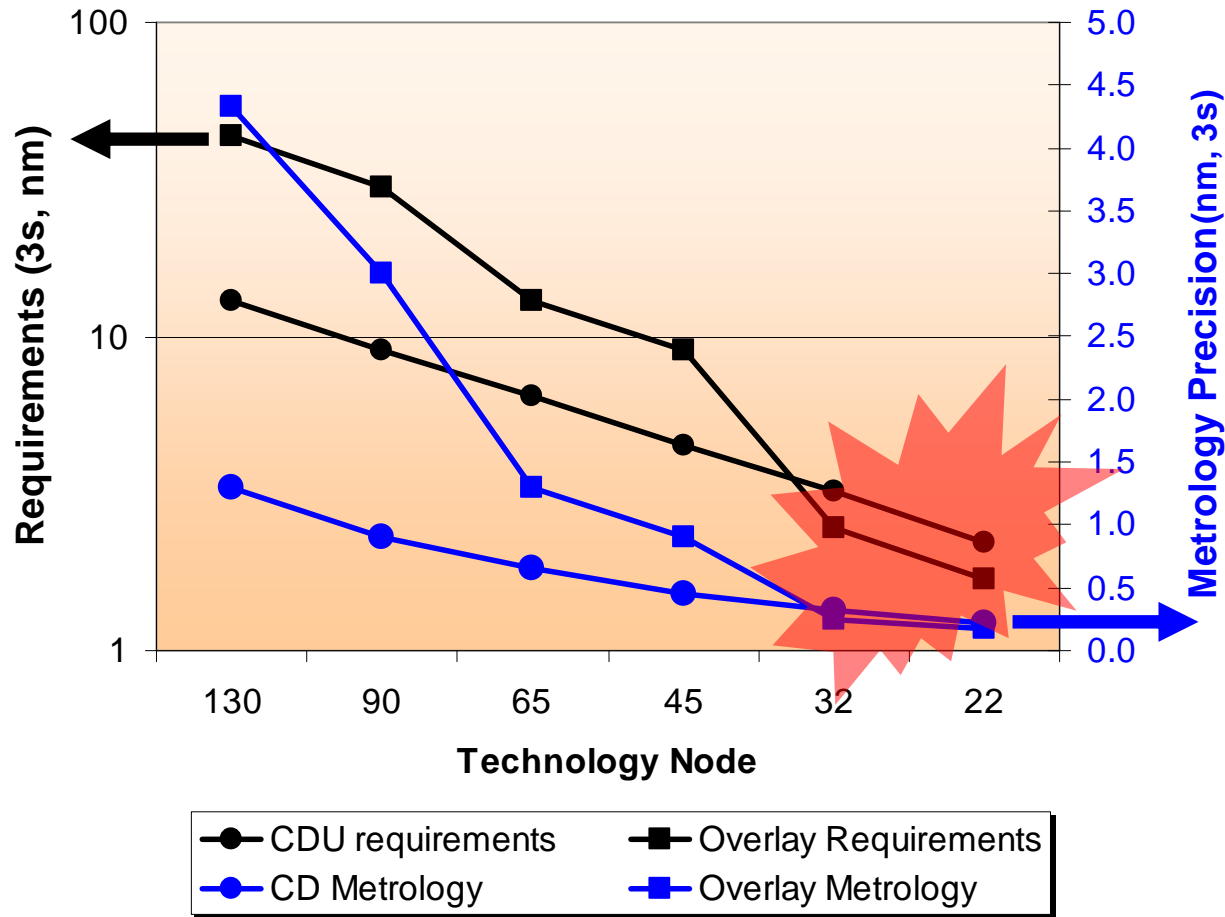
2007 ITRS Changes

		2007	2010	2013	2016	2018	2020
Technology Node		65 nm	45 nm	32 nm	22 nm	18nm	14 nm
	DRAM ½ Pitch (nm)	65	45	32	23	18	14
	FLASH ½ Pitch (nm)	54	36	25	18	14	11
	MPU Printed Gate Length (nm)	42	30	21	15	12	9
	MPU Physical Gate Length (nm)	25	18	13	9	7	6
	Wafer Overlay Control (nm)	13	9	6.4	4	3.2	2.5
	Lithography Metrology						
Gate	Physical CD Control (nm) Allowed Litho Variance = 3/4 Total Variance	2.6	1.9	1.3	0.9	0.7	0.6
	Wafer CD metrology tool uncertainty (3s, nm) at P/T = 0.2	0.52	0.37	0.26	0.19	0.15	0.12
	Etched Gate Line Width Roughness (nm) <8% of CD	2.0	1.4	1.0	0.7	0.6	0.5
Dense Lines	Printed CD Control (nm) Allowed Litho Variance = 3/4 Total Variance	6.8	4.7	3.3	2.4	1.9	1.5
	Wafer CD metrology tool uncertainty (3s, nm) at P/T = 0.2	1.4	0.9	0.7	0.5	0.4	0.3
Dual Patterning Overlay Metrology							
	Double Exposure and Etch - Process Range (nm)	?	?	?	?	?	?
	Double Exposure and Etch - Uncertainty (nm)	?	?	?	?	?	?
Front End Processes Metrology							
	High Performance Logic EOT equivalent oxide thickness (EOT), nm	1.1	0.6	0.5	0.5	0.5	0.5
	Logic Dielectric EOT Precision 3σ, nm	0.0044	0.0024	0.002	0.002	0.002	0.002
Interconnect Metrology							
	Barrier layer thick (nm)	5.2	3.3	2.4	1.7	1.3	1.1
	Void Size for 1% Voiding in Cu Lines	6.5	4.5	3.2	2.3	1.8	
	Detection of Killer Pores at (nm) size	6.5	4.5	3.2	2.3	1.8	

Replace Precision with Measurement Uncertainty



Overlay Metrology measurement uncertainty issue at 32 nm node (Double Patterning)

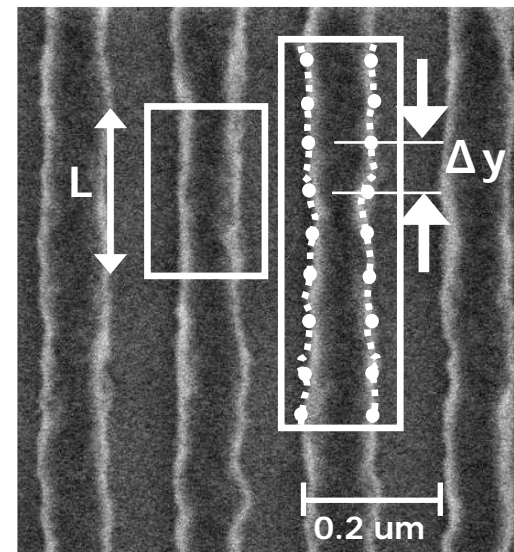


LER/LWR measurement

- Test method is approved as a SEMI standard in Nov./2006 and is available at SEMI homepage

P47-0307 : “Test Method for Evaluation of Line-Edge Roughness and Linewidth Roughness”

- Suggested measurement parameters are
Measurement length L : 2 μm or longer
Sampling interval Δy : 10nm or less
- One of our collaboration results among TWGs and related people



Courtesy of A. Ymaguchi (Hitachi)

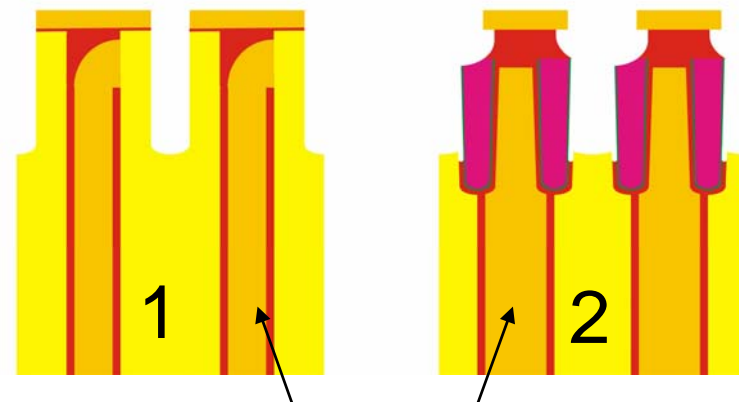
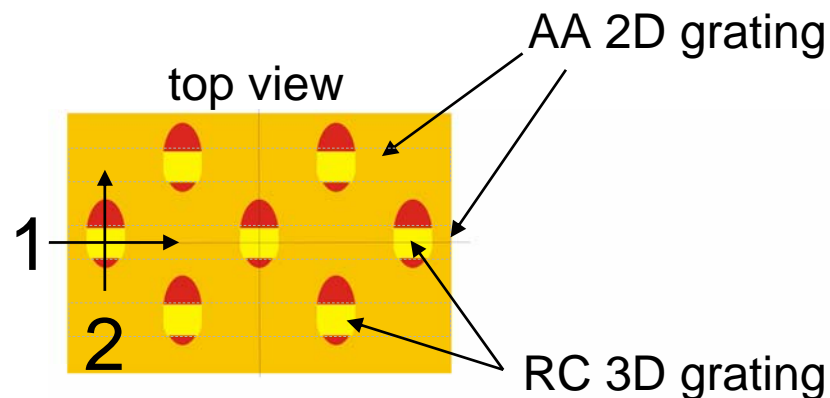
3D Metrology Requirements

example:

- Recess Channel Device

challenges:

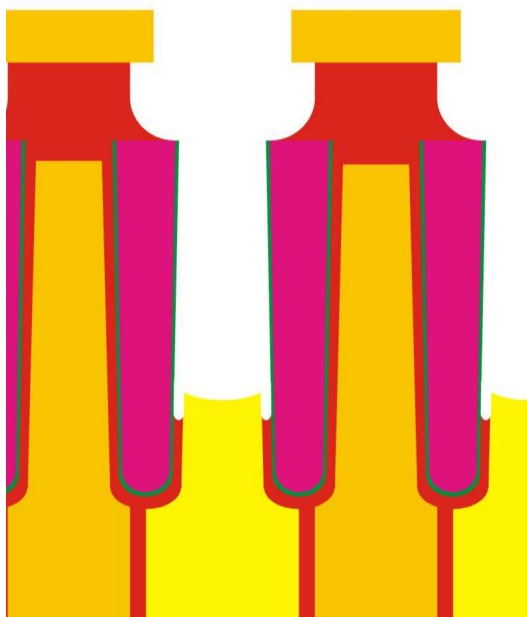
- complex grating-over-grating structure
- includes overlay shift between the gratings
- profile/geometry in different orientations is relevant
- small profile features may be relevant (e.g. corner devices)



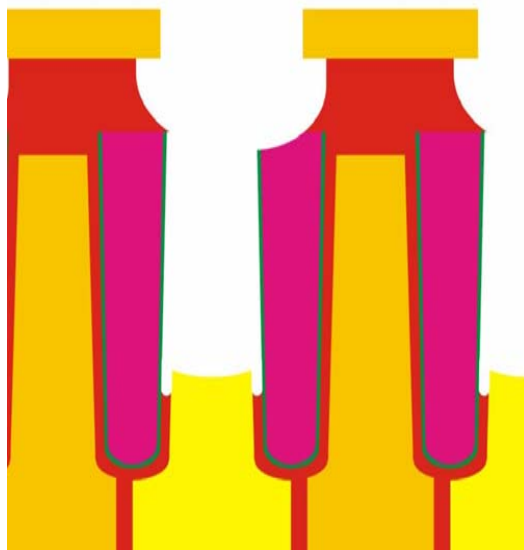
Deep Trench pattern
(not present in test structures)

3D Metrology Requirements

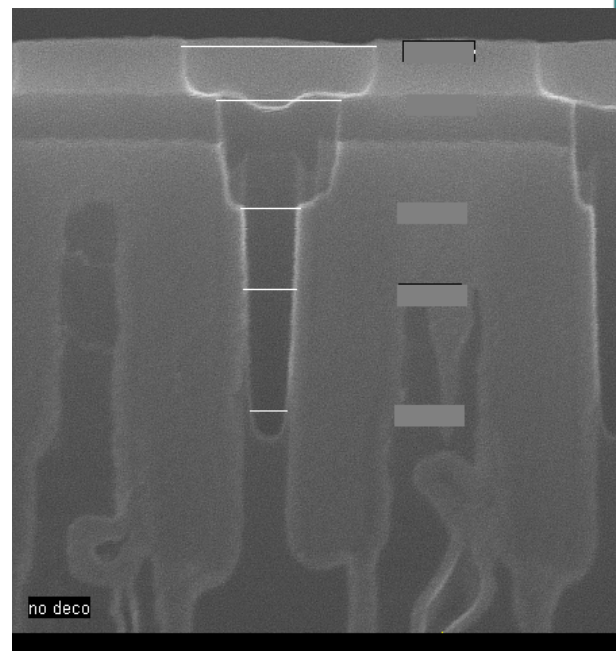
perfect overlay



overlay shift
creates asymmetry



cross section example



FEP Metrology:

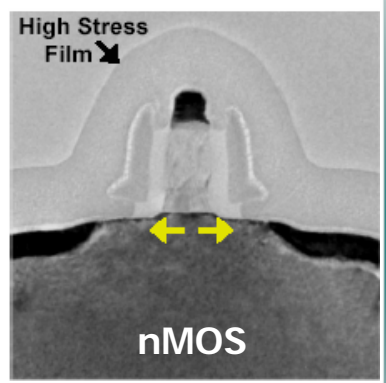
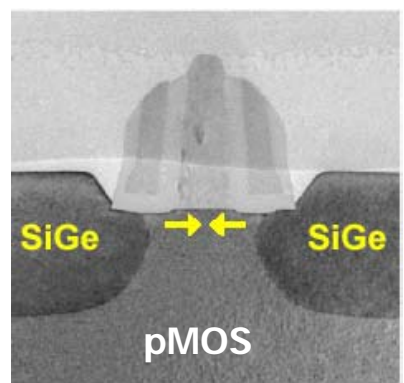
Expanded Emphasis on Areas beyond High k

- Increase in Mobility by using local stressing of transistors –
FEP Call for local stress metrology in the channel
- Metal Gates in production – Is routine Work Function measurement is a new requirement?
- New transistor designs are advancing rapidly.
Example: FIN-FETs require 3D metrology
- Rapid annealing at 32/22 nm Generation will drive new dopant metrology needs & characterization of active carriers in transistors.

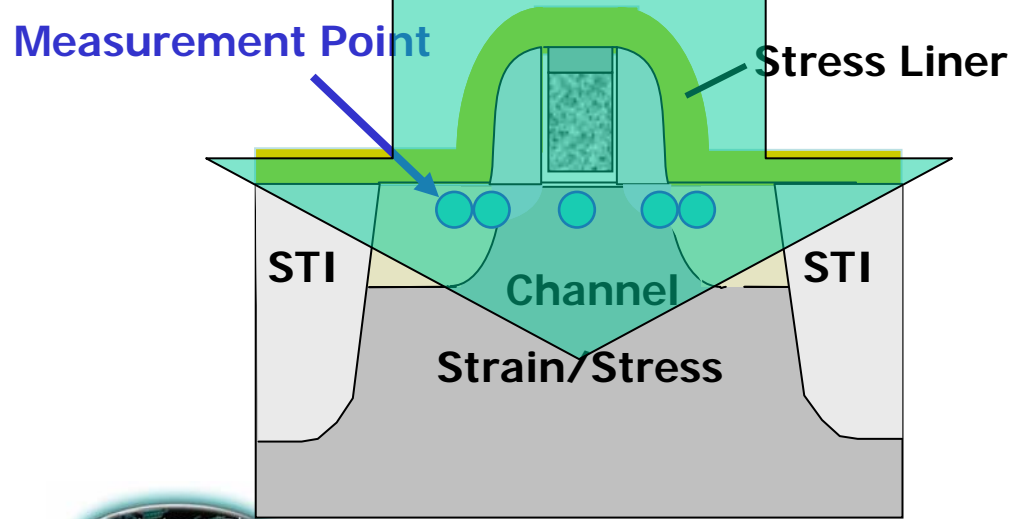


Local Strain/Stress Measurement

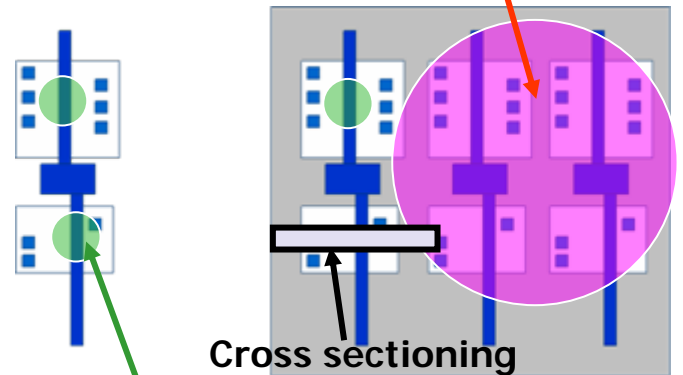
Proposal of new item on FEP table



Ghani, et al (Intel)



Wide laser spot for extracting average stress



Modified from Fichtner's figure



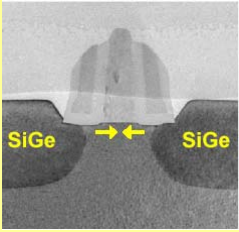




New table for Local Strain/Stress Measurement need inputs from FEP and PIDS

Table 120a Front End Processes Metrology Technology Requirements—Near-term Years

<i>Year of Production</i>	<i>2007</i>	<i>2008</i>	<i>2009</i>	<i>2010</i>	<i>2011</i>	<i>2012</i>	<i>2013</i>	<i>2014</i>	<i>2015</i>
DRAM ½ Pitch (nm) (contacted)	65	57	50	45	40	36	32	28	25
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	68	59	52	45	40	36	32	28	25
MPU Physical Gate Length (nm)	25	22	20	18	16	14	13	11	10
Mobility Enhancement Factor For Idsat (Table 40ab)									
- Extended Planar Bulk	1.08	1.09	1.1	1.1	1.12	1.11			
- UTB FDS		1.06	1.06	1.06	1.06	1.05	1.05	1.04	1.04
- DG					1.05	1.04	1.05	1.04	1.04
Stress measurement with 50MPa resolution									
Spatial resolution (Offline, destructive, single Tr.)	1/5 of Gate Length								
	5	4.4	4	3.6	3.2	2.8	2.6	2.2	2
Spatial resolution (Inline, non-destructive, Test pattern for average stress measurement)	Same size with HP								
	65	57	50	45	40	36	32	28	25
	Using test pad of 100um X 100um								
	100	100	100	100	100	100	100	100	100
Throughput (wafers/hour) (Inline, non-destructive, Test pattern)	25 sites per wafer								
	2	2	2	2	2	2	2	2	2



Local Strain/Stress Measurement Method (Tentative)

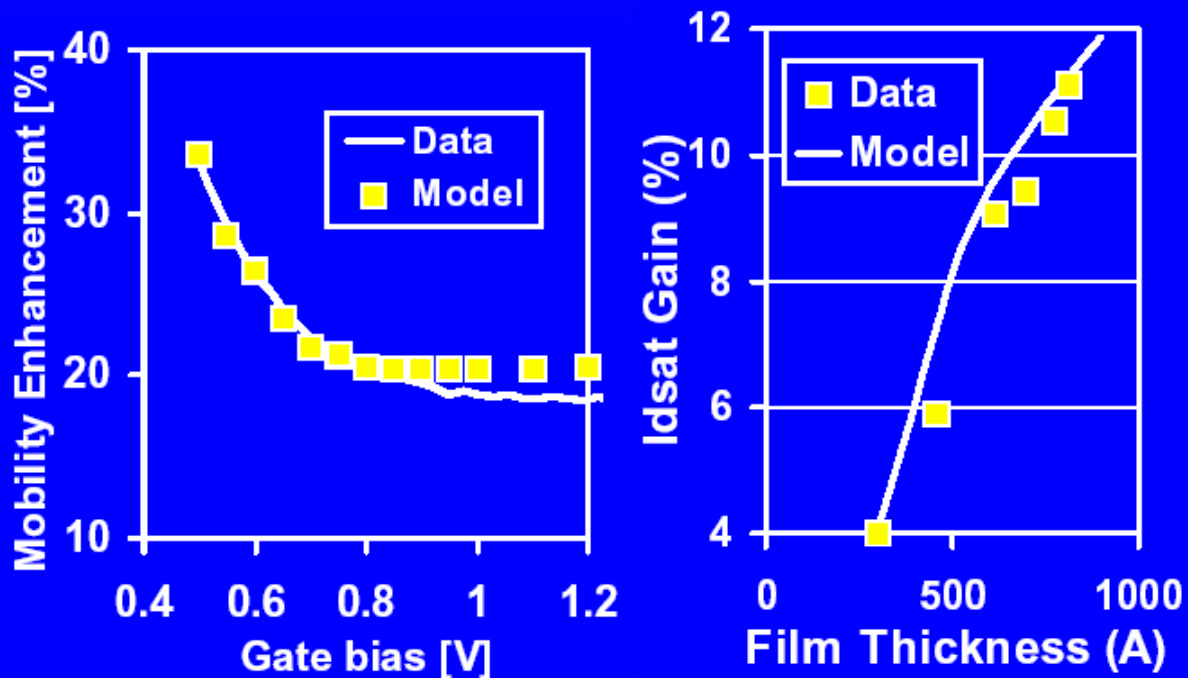
Area of Interest	Measurement Method	Sensitivity		Measurement Area	Sample Thickness	
		Stress	Strain			
Transistor Level 	- CBED	20 MPa	0.02%	10-20nm	<100nm	Destructive
	- NBD	100 MPa	0.1%	~10nm	<300nm	Destructive
	- TERS	50 MPa	0.05%	<50nm		Destructive Non-Destructive
Micro-Area Level 	- Confocal Raman	20 MPa	0.05%	~150nm		Non-Destructive
	- XRD	10 MPa	0.01%	100um		
	- Photoreflectance Spectroscopy					
<i>Handling Area of ITRS</i>						
Die 	- Die level flatness					Non-Destructive
	- Laser Interferometry					
	- Coherent Gradient Sensing					
Wafer 	- Laser Interferometry	10 MPa	0.001%	wafer		Non-Destructive
	- Coherent Gradient Sensing					
						
* Stress – Strain relation : need to be clarified						

TERS (Tip Enhanced Raman Scattering)
 CBED (Convergent Beam Electron Diffraction)
 NBD (Nano Beam Electron Diffraction)
 XRD (X-ray Diffraction)

Trend : Use Modeling to connect what you can measure with what you need to know

Example: Metrology of Strained Channel Devices

Short Channel NMOS Gain



MD Giles, et. al., VLSI Symposium

2004

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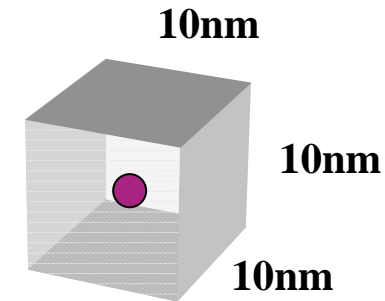
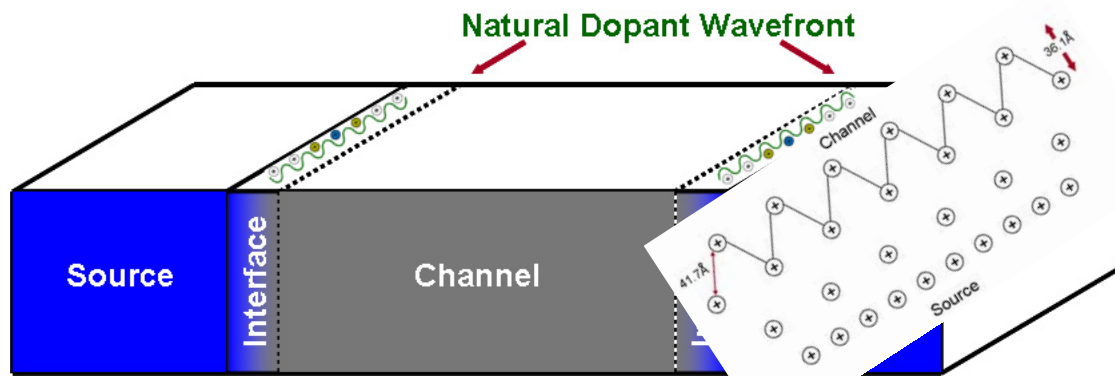


Dopant profile measurement (Essentially destructive)

•2006 Update

Table 120a Front End Processes Metrology Technology Requirements—Near-term Years *UPDATED*

Year of Production	2005	2006	2007	2008	2009	2010	2011	2012	2013
DRAM ½ Pitch (nm) (contacted)	80	70	65	57	50	45	40	36	32
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	90	78	68	59	52	45	40	36	32
MPU Physical Gate Length (nm)	32	28	25	22	20	18	16	14	13
WAS Lateral/depth spatial resolution for 2D/3D dopant profile (nm)	3.5	3.1	2.8	TBD	TBD	TBD	TBD	TBD	TBD
IS Lateral/depth spatial resolution for 2D/3D dopant profile (nm)	3.5	3.1	2.8	2.5	2.2	2	1.8	1.5	TBD
At-line dopant concentration precision (across concentration range) [D]	4%	4%	4%	4%	4%	2%	2%	2%	2%



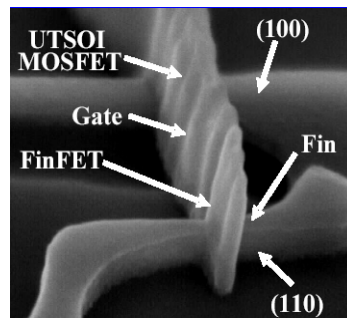
1×10^{18} atoms/cm³

Dan Herr - SRC

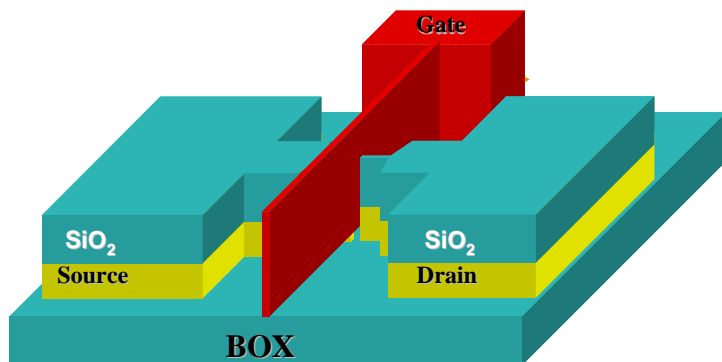
Total throughput of analysis is one of remaining issues

Do we need to put in a throughput requirement?

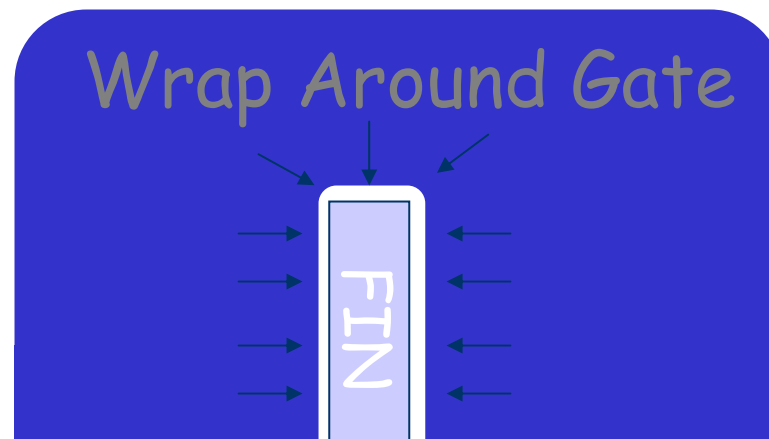
Wrap Around Gate Metrology



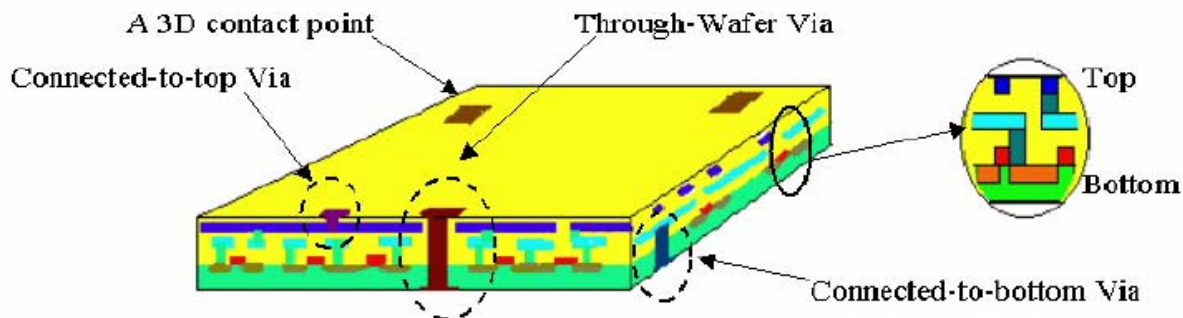
FINFET



Side Wall and Top Dielectric
Thickness and Composition

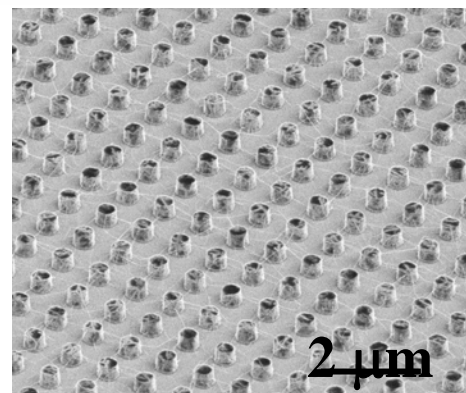


Future Interconnect (ITRS 2007)

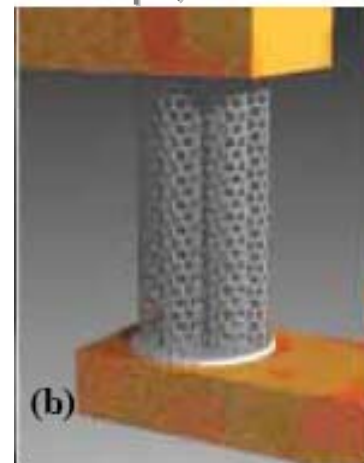


• 3D Interconnect ?

• Carbon Nanotubes ?



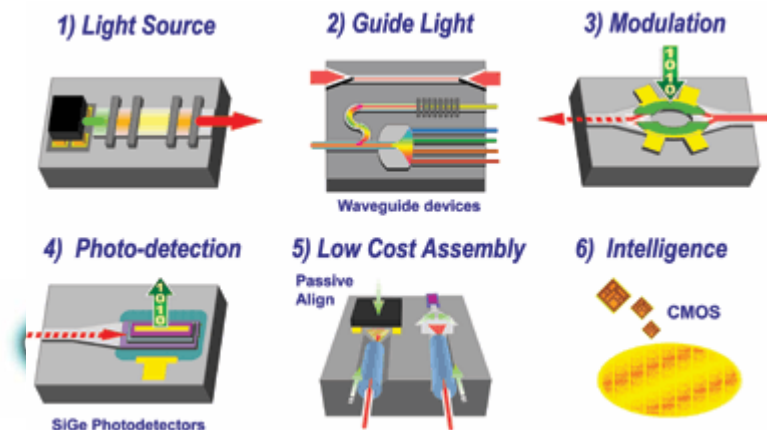
Kreupl, Infineon



MARCO Center

• Optical Interconnect ?

Intel



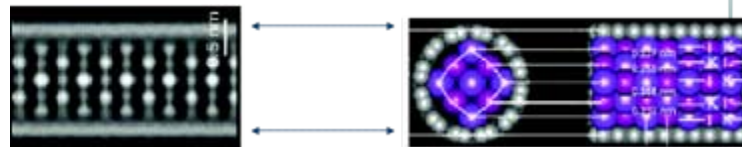
2006/2007 Interconnect Activities

- **Air Gap based “dielectric” near term potential solution for 22 nm $\frac{1}{2}$ pitch \neq porous low k**
- **Air Gap sacrificial layer does not require unique metrology**
- **Metrology is needed for 3D Integration**
 - Alignment of chips for stacking – wafer level integration
 - Defects in bonding
 - Damage to metal layers
 - Defects in vias between wafers
 - **Through Si via is high aspect ratio CD issue**
- **Measurements of Sidewall barrier thickness and sidewall damage (compositional changes in low k) after etch remains a Major Gap - It will soon also be a Gap for FEP Metrology**
- **New - Porous low k is projected for 32 nm $\frac{1}{2}$ Pitch.**



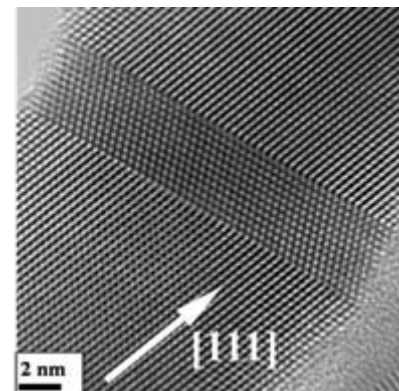
Metrology for Emerging Research Devices and Materials – 2007 ERM Teleconferences

- Atomic and nanoscale structure (including defects) of low Z materials, such as carbon nanotubes and graphitic materials



Aberration corrected HR-TEM of CNT with KI

- Correlate nanostructure to macro-scale: *bandgap, contact resistance, adhesion, mobility, dynamic properties, and nano-mechanical properties*
- Uniformity measurements of nanoscale properties over large areas
- In-Situ measurements that enable enhanced synthetic and process control



Metrology enables understanding the effect of crystal twins on mobility and mechanical properties

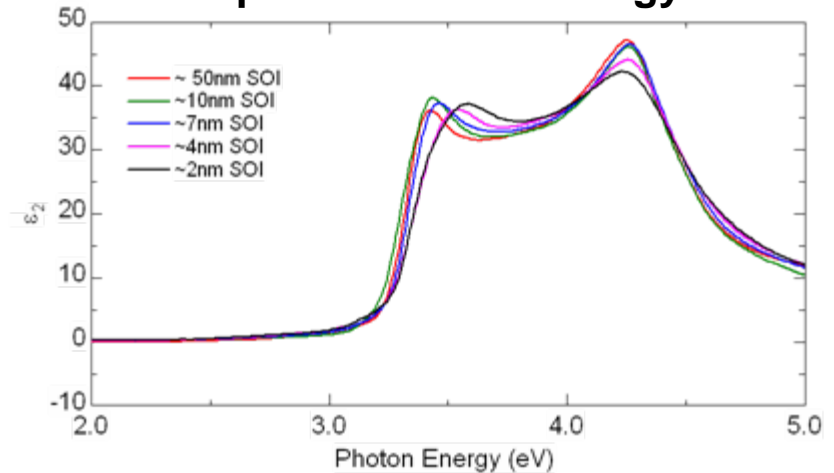


Metrology for Emerging Research Devices and Materials – 2007 ERM Teleconferences

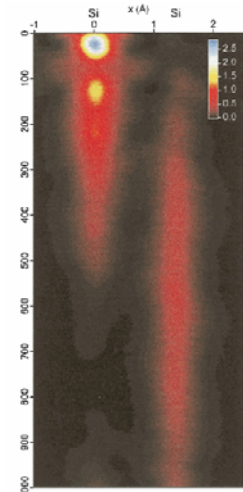
- Nondestructive 3D imaging of embedded interface, nanostructure, and atomic scale matrix properties
- Optical properties of isolated and integrated low dimensional materials
- Methods that resolve and separate surface from bulk
- Integrated metrology and modeling tools that deconvolve probe - sample interactions
- Nanoparticle monitors for ES&H, which include size, dose, and composition.

Dimensional Confinement effects

Properties and metrology

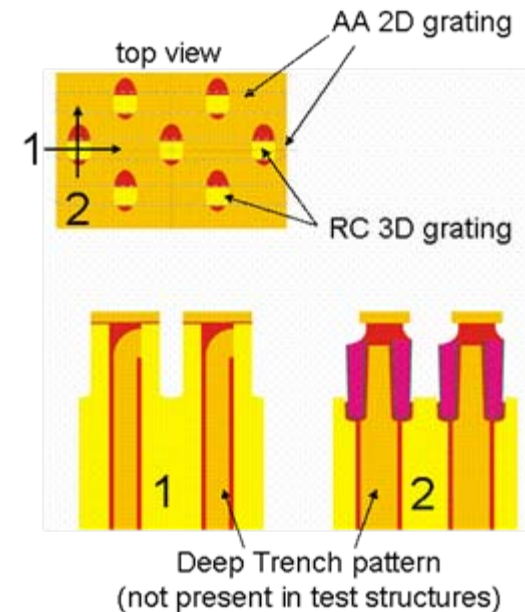
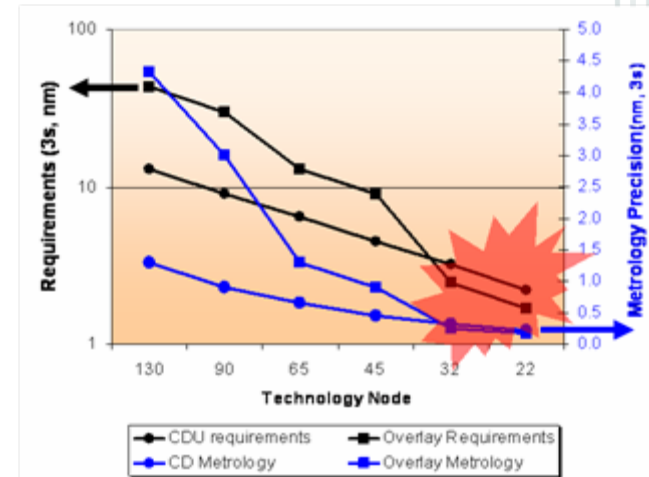


Simulation shows ebeam skipping to next atomic column



Metrology Key Messages

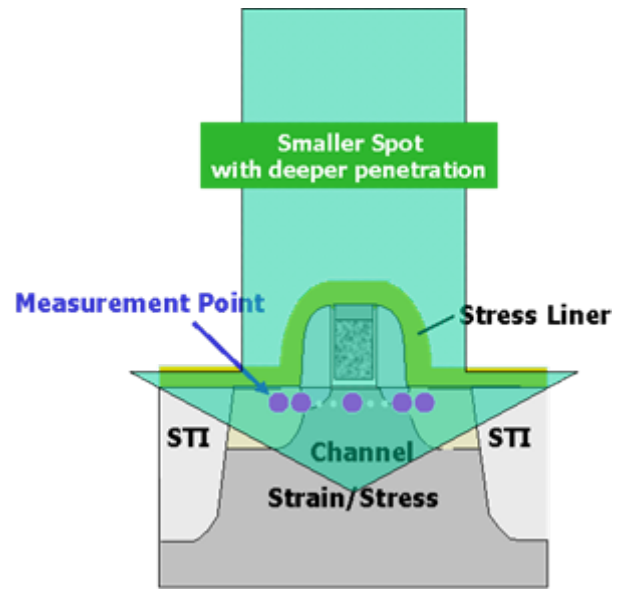
- **Litho Metrology**
 - **Dual Patterning Overlay Metrology**
 - **Overlay Metrology Capability for Single Layer in RED for 45 nm $\frac{1}{2}$ pitch**
 - **Overlay Definition for 32 nm $\frac{1}{2}$ Pitch?**
 - **Tightened to 70% of single layer**
 - **Challenge of High Aspect Ratio Contact Hole Metrology**
 - **SEMI Standard for LER / LWR accepted**
 - **Wafer Sampling Methodology Section added**
 - **New Uncertainty Definition- replace Precision**
 - **Main challenge to CD Metrology before 32 nm $\frac{1}{2}$ pitch is tool matching**
- **3D Dimensional and Shape Metrology for FEP, Interconnect and Litho**



Metrology Key Messages

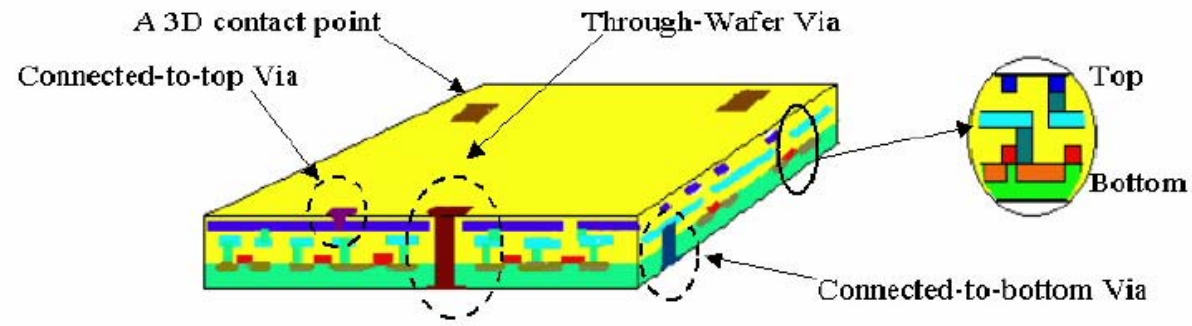
- FEP Metrology

- Stress/Strain Metrology Requirements added in 2007
- 2D/3D Dopant Profiling turn around time requirement added in 2007



- Interconnect Metrology

- 3D Interconnect Metrology added in 2007



Conclusions

- **CD Measurement improvements show a path to the 32 nm Node**
- **Propose definition for LWR and including LER**
- **Transistor channel engineering requires Stress and Mobility Measurement**
- **Interconnect requires Sidewall Measurements for barrier/seed and low κ trench**
- **ERM and ERD require both improved imaging (such as aberration corrected TEM) and image simulation**

