

ITRS Public Conference

Emerging Research Devices

San Francisco

Jim Hutchby – SRC

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- Samsung
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Highlights of Changes

□ Scope of ERD Chapter

- Invent the new “switch” – Emerging information processing* devices to eventually replace CMOS Boolean logic
- Supplement Si CMOS – Use the physics of emerging research devices to realize complex typically nonlinear functions in an accelerator-like fashion
 - ✓ Perform certain functions more efficiently than digital CMOS
 - ✓ Eventually extend CMOS and nanoelectronics to address new applications

□ Spin off a new chapter on Emerging Research Materials

□ Expand the Emerging Architecture Section

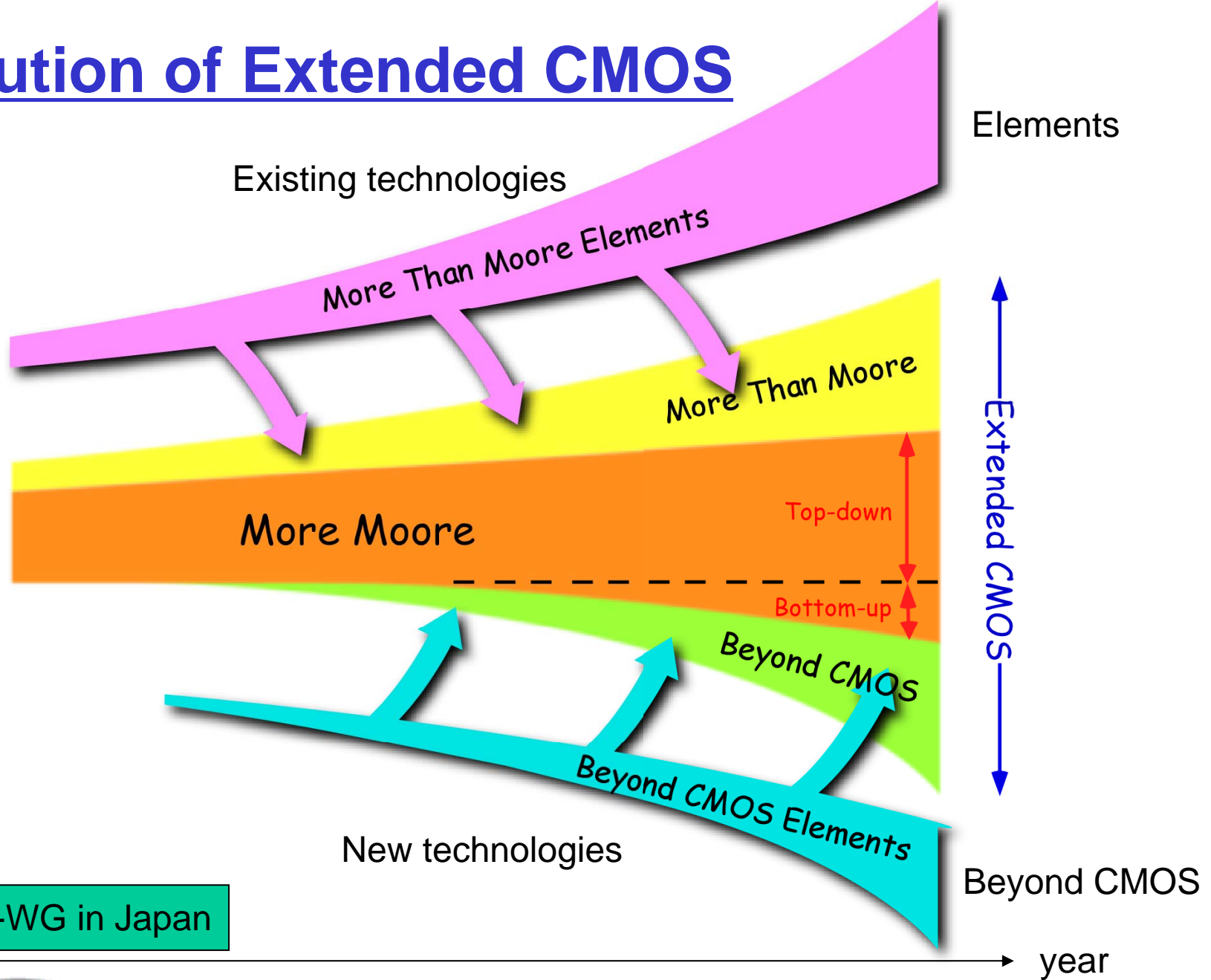
□ Expand scope of the Emerging Logic Section – supplement CMOS

- Example: Image Processing using emerging research devices integrated on a CMOS Platform.

□ Update the Emerging Memory Section

*ERD Chapter includes the following elements of Information Processing:
Data manipulation or processing, storage and communication.

Evolution of Extended CMOS



ERD-WG in Japan

2005 ITRS ERD Chapter

Emerging Research Memory Devices

	Nano-floating Gate Memory	Engineered tunnel barrier Memory	Ferroelectric FET Memory	Insulator Resistance Change Memory	Polymer Memory	Molecular Memories
<i>Storage Mechanism</i>	Charge on floating gate	Charge on floating gate	Remanent polarization on a ferroelectric gate dielectric	Multiple mechanisms	Not known	Not known
<i>Cell Elements</i>	1T	1T	1T	1T1R or 1R	1T1R or 1R	1T1R or 1R
<i>Device Types</i>	1 Nanocrystal 2 Direct tunneling	Graded insulator	FET with FE gate insulator	1 M-I-M 2 Solid Electrolyte 3 FE tunneling 4 FE Schottky diode 5 FE-LFE	M-I-M (nc)-I-M	Bi-stable switch
Capacitance-based				Resistance-based		

OUT

Expand

2007 ITRS ERD Chapter

Transition Table for Emerging Memory Devices

	<i>IN/OUT</i>	<i>Reason for IN/OUT</i>	<i>Comment</i>
<i>Nanofloating gate memory</i>	OUT	Natural evolution of FG FLASH. No outstanding research issues -became a prototypical technology	ERD recommends to include NFLG memory in PIDS (Not included in 2007PIDS chapter)
<i>Insulator Resistance Change Memory</i>	OUT	Replaced by three new memory categories (see below)	This memory category included several different memory types based on different mechanisms of operation
<i>Fuse/Antifuse Memory</i>	IN	Replacement for the Insulator resistance change memory	
<i>Ionic Memory</i>	IN	Replacement for the Insulator resistance change memory	
<i>Electronic Effects Memory</i>	IN	Replacement for the Insulator resistance change memory	
<i>Nano-mechanical memory</i>	IN	New device concept, promising characteristics, several recent publications	

2007 ITRS ERD Chapter

Capacitance-based memory technologies

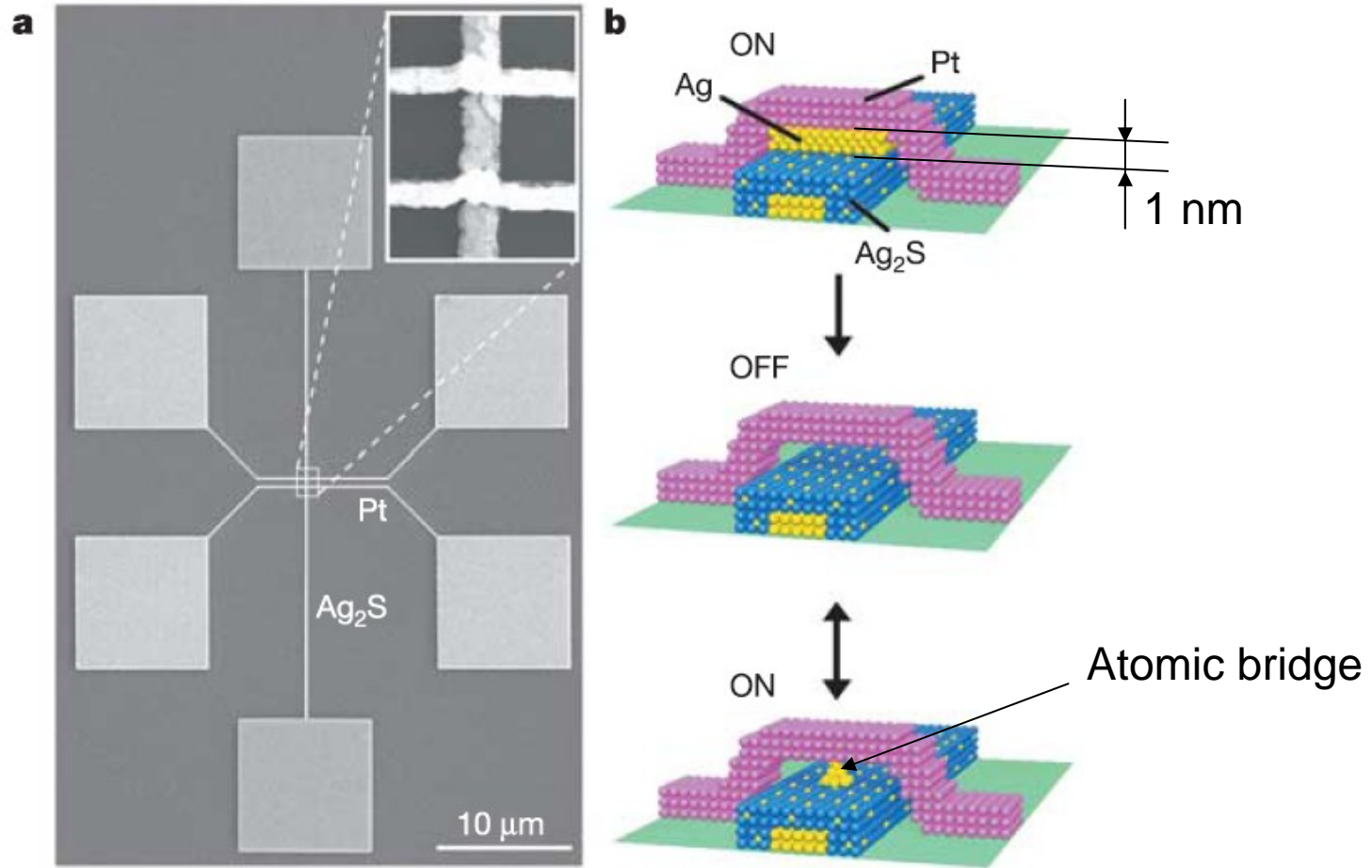
	Engineered tunnel barrier Memory	Ferroelectric FET Memory
<i>Storage Mechanism</i>	Charge on floating gate	Remnant polarization on a ferroelectric gate dielectric
<i>Cell Elements</i>	1T	1T
<i>Device Types</i>	Graded insulator	FET with FE gate insulator

2007 ITRS ERD Chapter

Resistance-based memory technologies

	Nanomechanical memory	Fuse/Anti fuse Memory	Ionic Memory	Electronic effects Memory	Polymer Memory	Molecular Memories
<i>Storage Mechanism</i>	Electrostatically-controlled bi-stable mechanical switch	Multiple mechanisms	Ion transport in solids	Multiple mechanisms	Not known	Not known
<i>Cell Elements</i>	1T1R or 1D1R	1T1R or 1D1R	1T1R or 1D1R	1T1R or 1D1R	1T1R or 1D1R	1T1R or 1D1R
<i>Device Types</i>	CNT bridge CNT cantilever Si cantilever Nanoparticle	M-I-M e.g. Pt/NiO/Pt	1) Solid Electrolyte 2) RedOx reaction	1) Charge trapping 2) Mott transition 3) FE Barrier effects	M-I-M (nc)-I-M	Bi-stable switch

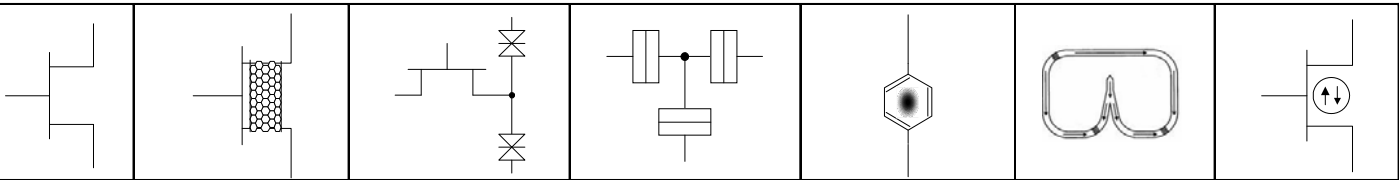
Atomic Switch



K. Terabe et al. Nature 433 (2005) 47.

2005 ITRS ERD

Emerging Research Logic Devices

<p><i>Device</i></p> 	<p><i>FET [B]</i></p>	<p><i>1D structures</i></p>	<p><i>Resonant Tunneling Devices</i></p>	<p><i>SET</i></p>	<p><i>Molecular</i></p>	<p><i>Ferromagnetic logic</i></p>	<p><i>Spin transistor</i></p>
<p><i>Types</i></p>	<p><i>Si CMOS</i></p>	<p><i>CNT FET NW FET NW h structure</i></p>	<p><i>RD-FET RTT</i></p>	<p><i>SET</i></p>	<p><i>Crossbar latch Molecular transistor Molecular QCA</i></p>	<p><i>Moving domain wall M: QCA</i></p>	<p><i>Spin transistor</i></p>
<p><i>Supported Architectures</i></p>	<p><i>Conventional</i></p>	<p><i>Conventional and Cross-bar</i></p>		<p><i>CNN</i></p>	<p><i>Cross-bar and QCA</i></p>	<p><i>CNN Reconfigure logic and QCA</i></p>	<p><i>Conventional</i></p>

Expand

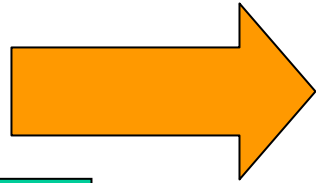
Transition

Logic Device Conclusions

- ◆ Continued analysis of alternative technology entries likely will continue to yield the same result:
 - **Nothing beats MOSFETs overall for performing Boolean logic operations at comparable risk levels**
- ◆ Certain functions, e.g. image recognition (associative processing), may be more efficiently done in networks of non-linear devices rather than Boolean logic gates

Supplementing CMOS

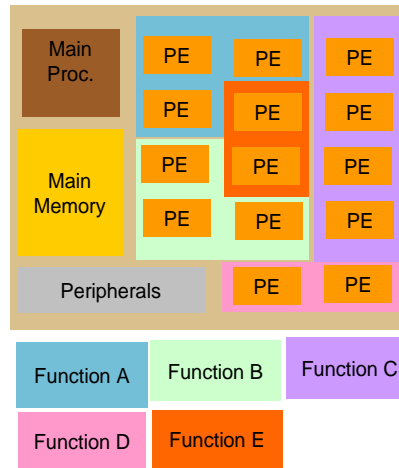
Basis of Existing Assessments of Logic Devices



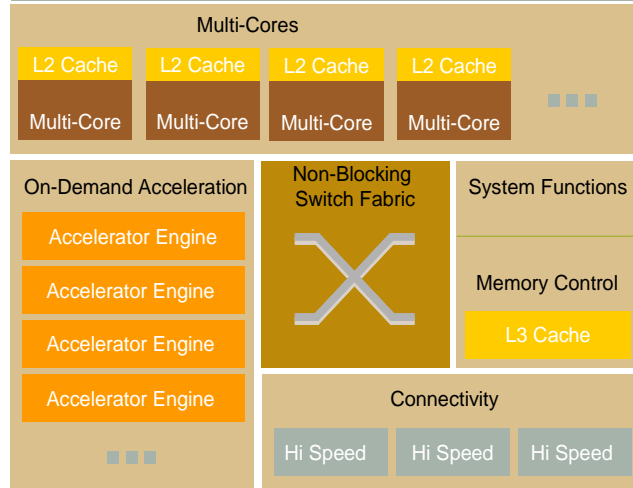
A possible ultimate evolution of **on-chip** architectures is Asynchronous **Heterogeneous** Multi-Core with Hierarchical Processors Organization

General Purpose Processor

SOC-PE Architecture



Multi-Core/Accelerator Engine Platform (SOC-MC/AE Architecture)



Courtesy Fawzi Behmann - Freescale

New Focus & Direction of Logic Section

Consider new information processing technologies that supplement CMOS to provide enhanced hardware capability and can be optimally executed with alternative devices

Focus

- ◆ Understand the performance of the device in terms of its non-linear characteristics

Direction

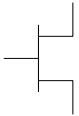
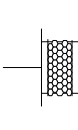
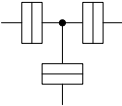


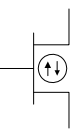
- ◆ Retain present table that evaluates technology entries (TEs) against CMOS devices for Boolean logic
- ◆ Include a second table (new) that evaluates technology entries against CMOS for special purpose “macro-functions” e.g. image processing
- ◆ Consider inclusion of new technology entries based on enhanced functionalities in new operations

Transition Table for Emerging Logic Devices

	<i>IN/OUT</i>	<i>Reason for IN/OUT</i>	<i>Comment</i>
<i>Rapid Single Flux Quanta</i>	OUT	RSFQ devices, systems and circuits have been developed, prototyped, and fabricated. They could become an important technology if the correct market driver emerges	Design and fabrication lines for RSFQ systems exist. Cryogenic operation, cost and material integration issues limit application space
<i>CMOS extension-</i>	IN	Low bandgap, compound III-V materials can potentially improve transistor performance	Research on compound III –V materials on SI substrates has increased significantly over the last 2 years
<i>Impact Ionization MOS</i>	IN (pending)	Simulation results showing very low sub threshold slopes indicate potential for low power operation	May be included in future editions
<i>Nano Electro Mechanical Systems</i>	IN (pending)	Potential for ultra low leakage device based on nano relay operation	May be included in future editions
<i>Lateral interband tunneling transistor</i>	IN (pending)	Potential to utilize gate modulated interband tunneling to reduce subthreshold slope	May be included in future editions
<i>Floating gate MOS devices</i>	IN (pending)	Devices with nanocrystals embedded in gate allow circuits with tuneable thresholds. Potential for low power circuits	May be included in future editions

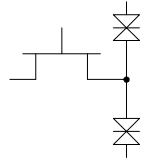
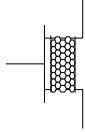
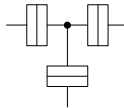
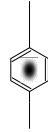

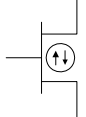
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CMOS Scaling & Replacement Devices (1st)

Device							
	<i>FET</i>	<i>CMOS Extension Low dimensional structures</i>	<i>CMOS Extension III-V channel replacement</i>	<i>SET</i>	<i>Molecular</i>	<i>Ferromagnetic logic</i>	<i>Spin transistor</i>
Types	Si CMOS	<ul style="list-style-type: none"> •CNT FET •NW FET •NW hetero-structures •Nanoribbon transistors 	<ul style="list-style-type: none"> •III-V compound semiconduct or channel replacement 	SET	<ul style="list-style-type: none"> •2-terminal •3-terminal FET •3-terminal bipolar transistor •NEMS •Molecular QCA 	<ul style="list-style-type: none"> •Moving domain wall •Hybrid Hall effect •Magnetic Resistive Element •M: QCA 	<ul style="list-style-type: none"> •Spin Gain transistor •HMF Spin MOSFET •Spin Torque Transistor
Supported Architectures	Conventional	Conventional	Conventional	Threshold logic	Memory-based QCA	Lithographically defined	conventional

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CMOS Supplement Devices (2nd Table)

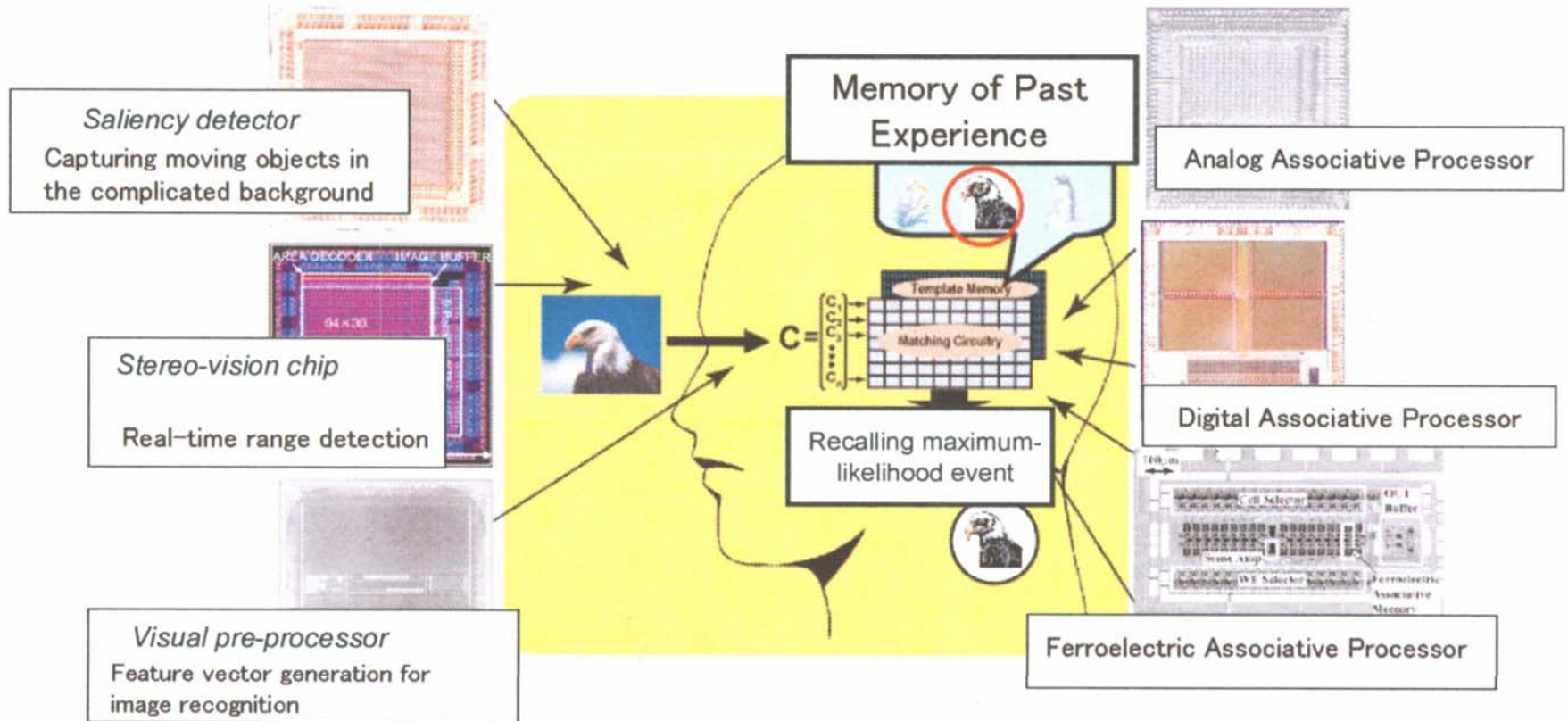
						
Device	Resonant tunneling diodes	Muti ferroic tunnel junctions	Single Electron Transistors	Molecular devices	Ferromagnetic devices	Frequency coherent spin devices
State variable	Charge	Dielectric and magnetic domain polarization	Charge	Molecular Conformation	Ferromagnetic polarization	Precession frequency
Response function	Negative differential resistance	Four resistive states	Coulomb blockade	Hysteritic	Non-linear	Nonlinear

Potential Supplemental Applications

- ◆ Image recognition
- ◆ Speech recognition
- ◆ DSP (cross correlation)
- ◆ Data Mining
- ◆ Optimization
- ◆ Physical simulation
- ◆ Sensory data processing (biological, physical)
- ◆ Image creation
- ◆ Cryptographic analysis

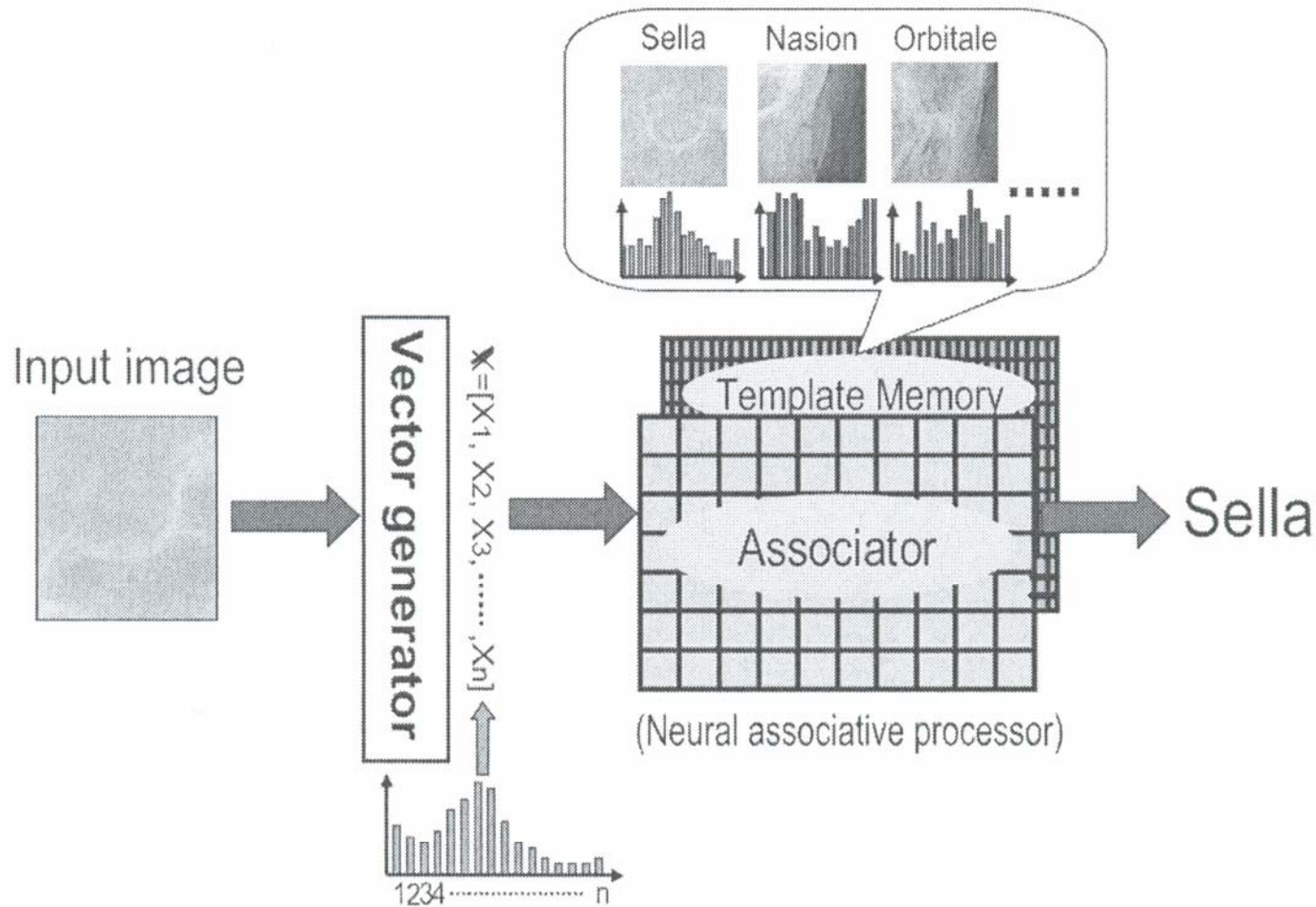
Illustrative
Example

Top down information processing Image Recognition



Tadashi Shibata, University of Tokyo

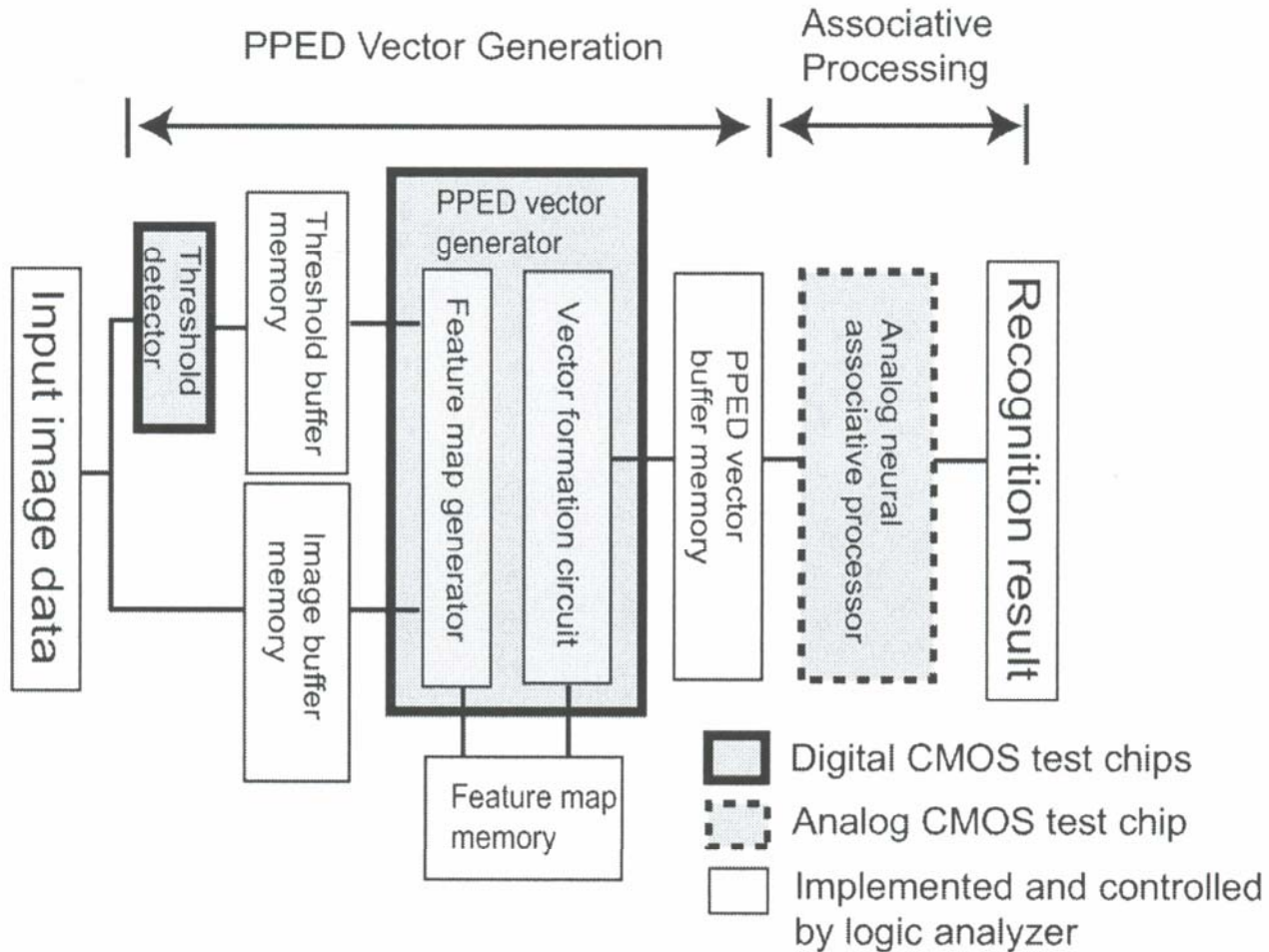
Image recognition



(a)

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Image recognition



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Specialized devices for image recognition

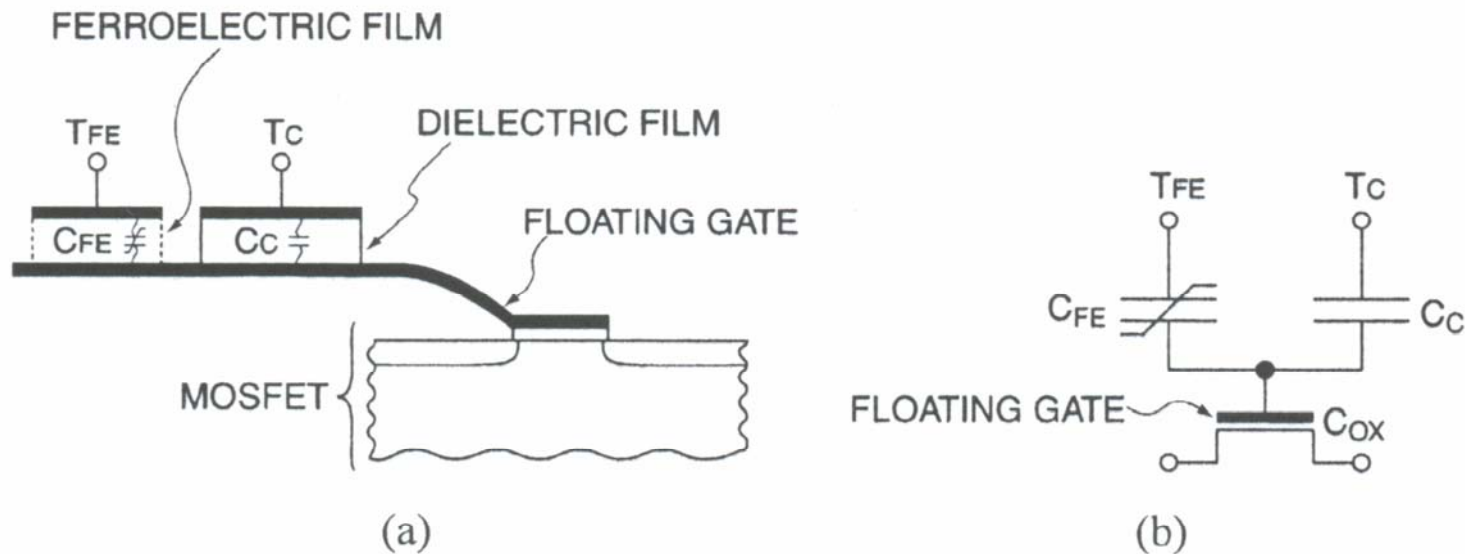


Fig. 1. (a) Conceptual drawing of the basic structure of the heterogate FGMOS. (b) Symbol representing the device.

Heterogate ferroelectric FGMOS FET

Tadashi Shibata, University of Tokyo

Image recognition

TABLE I
PERFORMANCES COMPARISON OF IMAGE RECOGNITION SYSTEMS

Search target: Sella (a pituitary gland)

Number of templates (generated by learning algorithm): 15

Search Area: 75x100-pel area

	Power(W)	Computational time (Second)	Total energy(J)
Pentium 4 1.5GHz Optimized in an assembly language level	54.7	5	273.5
Mobile Pentium 3 500MHz/1.1V Optimized in an assembly language level	3.5	15	52
Our digital vector generator & neural analog associative processor	0.152	1.2	0.182

Tadashi Shibata, University of Tokyo

Emerging Research Architectures

Architecture	Implementation	Computational Elements	Network	Application	Research Activity
Homogeneous Many-Core	Symmetric cores	CMOS	Irregular/Fixed	Synthesis/GPP	
Heterogeneous	Asymmetric cores	CMOS	Irregular/Fixed	Synthesis/GPP	
	CMOL	CMOS+Molecular Switches	Irregular/Fixed	Synthesis/GPP	
	Molecular Cross-bar	Molecular Switches	Regular/Flexible	Synthesis/GPP	
	Check-point	CMOS+ Ferromagnetic logic	Irregular/Fixed	Synthesis/GPP	
Morphic	CNN	CMOS+Sensors	Regular/Flexible	Recognition/Vision	
	AMP	FG-FET, SET	Irregular/Fixed	Recognition/Vision	
	Bio-inspired	MFTD, Spin-gain transistor	Mixed	Recognition Mining Synthesis	

CMOL – ‘Molecule on CMOS’ architecture
 CNN – Cellular Nonlinear Network
 AMP – Associative Memory Processor

GPP – General Purpose Processor
 FG-MOS – Floating Gate MOS devices
 SET – single electron transistor

MFTD – multiferroic tunnel diode

Summary

- ◆ **Scope:** Broaden scope to encourage emerging technologies both to supplement CMOS as well as eventually to invent the new “switch”.
- ◆ **Materials Section:** Spin out a new cross-cut chapter on Emerging Research Materials.
- ◆ **Memory Section:** Added NEMS mechanical memory to section.
 - Divide Emerging Memory Tables into Resistive and Capacitive subcategories
 - Updated section in 2007.
- ◆ **Logic Section:** Reformulated Logic Device Section to encourage high potential, but high risk approaches while maintaining Technology Entry evaluation function.
 - Re-considered status of candidate Technology Entries.
 - Re-structured Logic Section.
- ◆ **Architecture Section:** Revised section to focus on encouraging research to explore optimal organization of emerging non-linear devices to efficiently realize accelerator-like functions to supplement the CMOS platform technology.