

# Issues and Results for 2007 ITRS

Peter M. Zeitzoff for  
**PIDS Technology Working Group**

**ITRS Public Meeting  
San Francisco, CA  
July 18, 2007**



# PIDS Roster

## Taiwan

- R. Liu (Chair)
- Y. J. Mii
- C. Diaz
- M. Ma (Co-chair)
- M. J. Tsai
- E. Po

## Korea

- I. S. Yeo
- K. H. Lee

## Europe

- T. Skotnicki (Chair)
- K. Schruefer
- S DeLeonibus
- K. De Meyer
- R. Lander
- M. Jurczak

## Japan

- K. Imai (Chair)
- T. Sugii
- S. Sawada
- S. Oda
- T. Hiramoto
- S. Takagi
- K. Shibahara
- A. Hori
- D. Hisamoto
- T. Nakamura
- Y. Tadaki
- Y. Tagawa
- Y. Takeda
- N. Kasai
- Y. Akasaka
- H. Inoue
- M. Yoshimi
- M. Mifuji
- M. Ogura
- J. Ida
- K. Kamei

## Japan (con't)

- T. Tanaka
- Y. Kiyota
- M. Fujisawa
- T. Eimori
- US
- P. Zeitzoff (Chair)
- J. Chung
- J. Brewer
- A. Lochtefeld
- M. Rodder
- W. Maszara
- B-Y. Nguyen
- T. Ning
- G. Yeap
- M. Duane
- T. Dellin
- W. Tsai
- J. Hutchby



# Outline

- *Scope and Subcategories*
- **Logic**
- **Non-Volatile Memory**
- **DRAM**
- **Reliability**



# **PIDS Scope**

- **PIDS = Process Integration, Developments, and Structures**
- **Main concerns**
  - **MOSFET, memory, and passive devices and structures**
    - **Device physical and electrical characteristics and requirements**
  - **Broad issues of device and circuit performance, density, and power dissipation, particularly as they drive overall technology requirements**
  - **Reliability**



# PIDS Subcategories

- **Logic**
  - High-performance
  - Low-power (mobile applications)
- **Memory**
  - DRAM
  - Non-volatile memory (NVM)
- **Reliability**

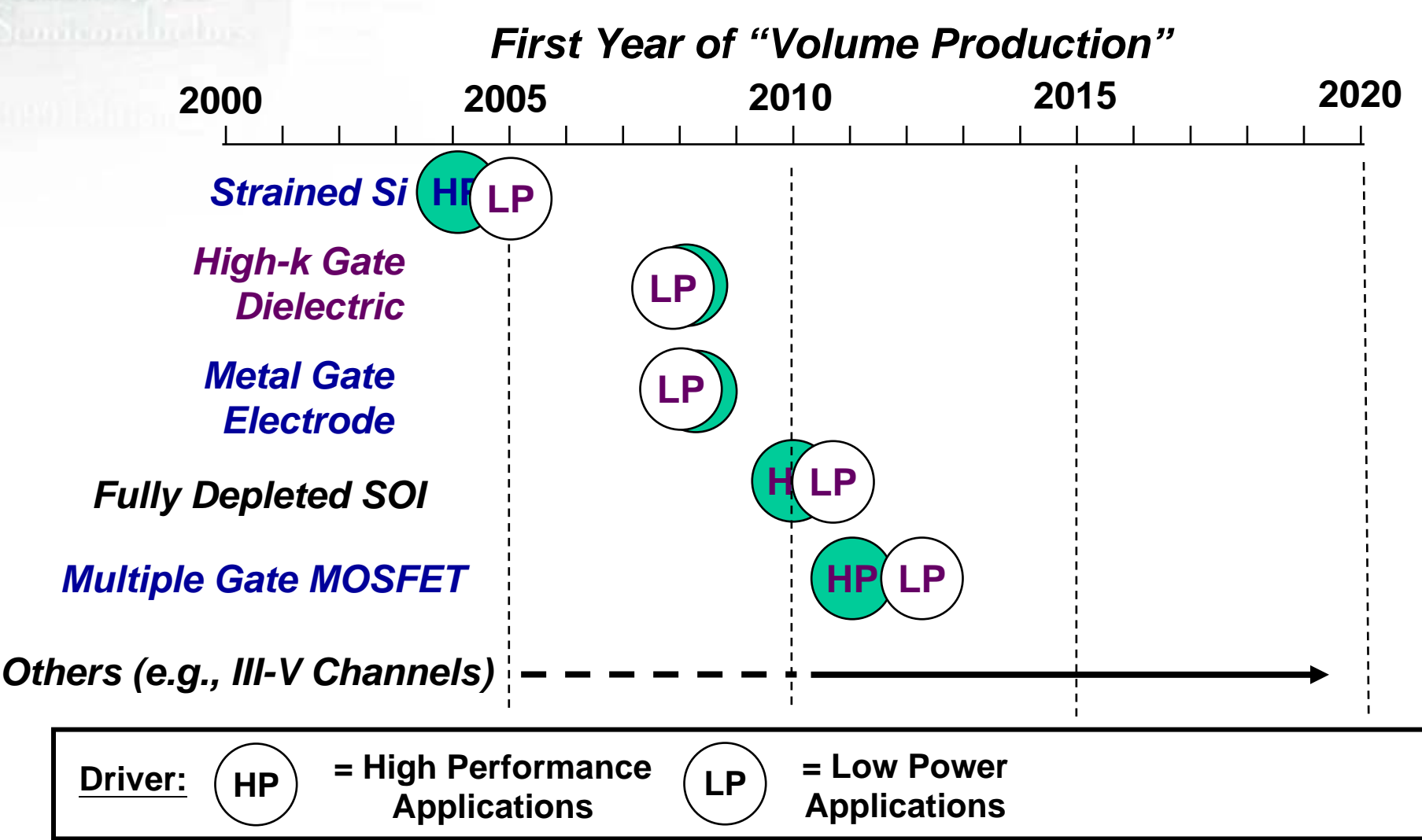
# Outline

- **Scope and Subcategories**
- *Logic*
- **Non-Volatile Memory**
- **DRAM**
- **Reliability**

# Logic: Scaling Approach and Categories

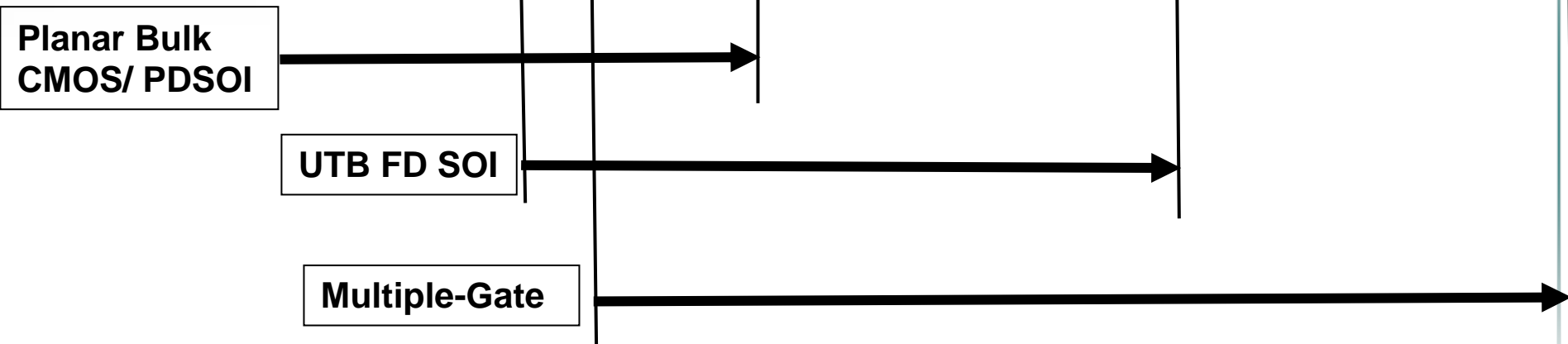
- MASTAR (detailed analytic device model from STM and corporate partners) is used to do device scaling, generate tables
  - MASTAR has been extensively verified against literature and other data
  - Initial choice of scaled MOSFET parameters is made
  - Using MASTAR, MOSFET parameters are iteratively varied to meet ITRS targets → examine tradeoffs
- Types of Logic
  - High Performance (HP) (e.g., MPU): target is historical 17%/year transistor CV/I increase
  - Low Power (for mobile applications): target is specific, low level of leakage current
    - Low Standby Power (LSTP): very low leakage; for lower performance, consumer applications (e.g., cellphone)
    - Low Operating Power (LOP): low dynamic power, rel. high performance (e.g., notebook computer)

# Multiple, Major Technology Innovations Required Over the Next Few Years to Meet Key MOSFET Targets



# Multiple Parallel Paths for High-Performance Logic in ITRS

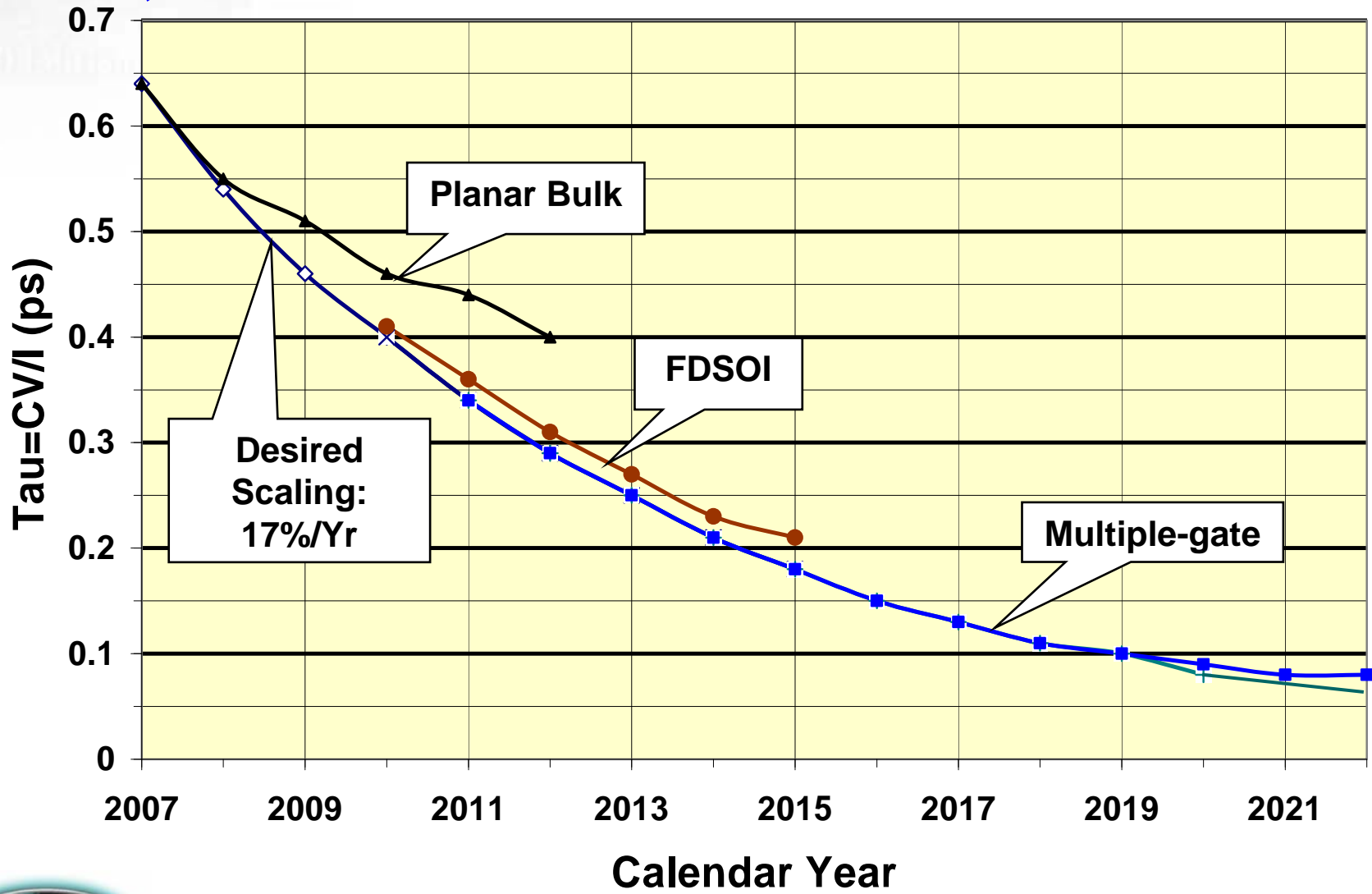
Year in Production		2007	2008	2009	2010	2011	2012	2013	2014	2015	2016	2017	2018	2019	2020	2021	2022
Physical Lgate (High Performance)	nm	32	28	25	22	20	18	16	14	13	11	10	9	8	7	6	5



## Multiple parallel paths reflects most likely scenario:

- Some companies will extend planar bulk CMOS/PDSOI as long as possible
- Others will switch to FDSOI and/or multiple gate earlier
- Ultimate MOSFET is multiple-gate
- Similar multiple paths for low-power logic

# High-Performance Logic: Scaling of Transistor Speed Metric, $CV/I$



# Outline

- **Scope and Subcategories**
- **Logic**
- ***Non-Volatile Memory***
- **DRAM**
- **Reliability**



# NAND Flash Roadmap: F

- F = half-pitch
  - DRAM: Metal 1 (contacted)
  - Flash: Poly (uncontacted)
- Survey completed
  - Flash memory scaling has pulled 2 years ahead of DRAM scaling
    - One year pull-in from 2005 ITRS

	2005	2006	2007	2008	2009	2010
<i>05 NAND Flash</i>	<i>76</i>	<i>64</i>	<i>57</i>	<i>51</i>	<i>45</i>	<i>40</i>
<i>07 NAND Flash</i>			<i>51</i>	<i>45</i>	<i>40</i>	<i>36</i>
<i>05 DRAM 1/2pitch</i>	<i>80</i>	<i>70</i>	<i>65</i>	<i>57</i>	<i>50</i>	<i>45</i>

# PIDS NVM Update

- **Major revisions for 2007 NVM section**
  - **Separate NOR and NAND applications**
  - **NOR includes floating gate and charge trapping storage devices**
  - **NAND will migrate from floating gate to charge trapping and eventually to 3D stacking, per survey results**
  - **Non-charge-storage based NVM table covers PCRAM, MRAM, and FeRAM**
- **Node time line for NAND flash more critical now because NAND may start to drive lithography and other tools**



# Outline

- **Scope and Subcategories**
- **Logic**
- **Non-Volatile Memory**
- ***DRAM***
- **Reliability**

# DRAM Survey Carried Out in Mid-to-Late 2006, Analysis Completed

- ● ● 1. DRAM half pitch (minimum feature size :  $F$ )
- ● ● 2. Cell size :  $A_{cell}$
- ● ● 3. Cell size factor :  $a$  [  $A_{cell} = a F^2$  ]
- ● ● 4. DRAM Product (bit) :  $b$
- ● ● 5. Chip size :  $A_{chip}$
- ● ● 6. Area factor [ =  $A_{cell} \times b / A_{chip}$  ]
- ● ● 7. Retention time
- ● ● 8. Storage Capacitance :  $C_s$
- ● ● 9. Voltage of capacitor
- ● ● 10. Gate oxide thickness of cell transistor
- ● ● 11. Maximum word-line level
- ● ● 12. Effective electric field of gate insulator
- ● ● 13. Negative word-line use
- ● ● 14. Capacitor structure
- ● ● 15. Capacitor insulator material
- ● ● 16. Effective capacitor insulator thickness
- ● ● 17. Physical capacitor insulator thickness
- ● ● 18. Support FET (EOT, Ion,  $V_t$ )
- ● ● 19. Array FET structure

●	Overall Table
●	PIDS Table
●	FEP Table

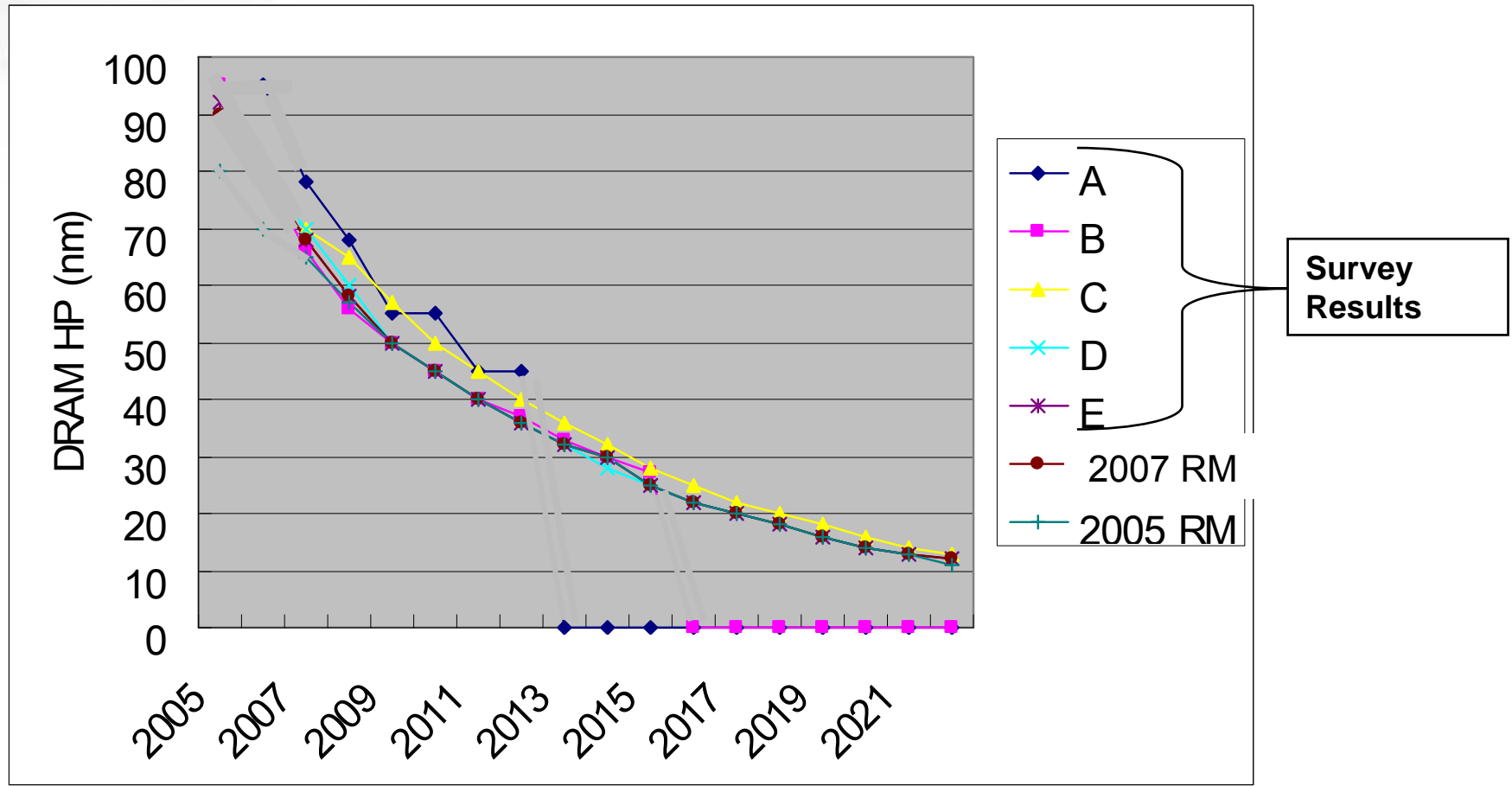


# DRAM: Key Directions for 2007 ITRS, per Survey Results

- **Feature size scaling unchanged from 2005 ITRS**
  - **F = half-pitch of contacted M1 : 3 year cycle**
    - 65nm in 2007, 45 nm in 2010
- **Other results**
  - **Cell size factor,  $a=(\text{cell area})/F^2$** 
    - $a=8$  through 2005,  $a=6$  in 2006 and thereafter
    - 2-years pull-in from 2005 ITRS
  - **DRAM product generation: 1 year delay from 2005 ITRS**
    - 4Gb delayed from 2009 until 2010
  - **Capacitor equivalent oxide thickness,  $T_{eq}$** 
    - $T_{eq}$  is unchanged from 2005 ITRS up to 2010
    - Ultra-high-k dielectric (new material) needed beyond 2010



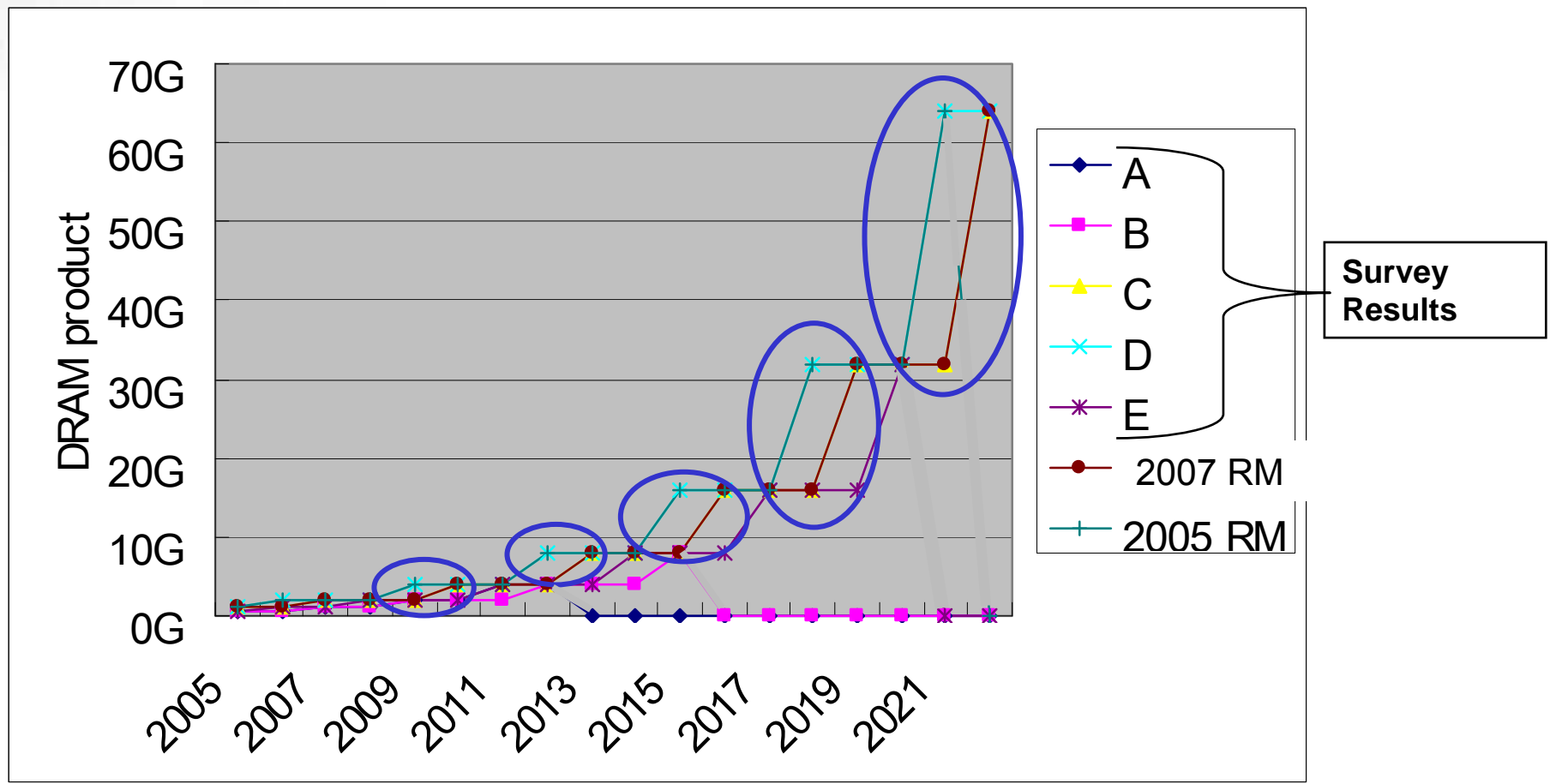
# Scaling of DRAM Half Pitch (F)



**The same as in 2005 version**



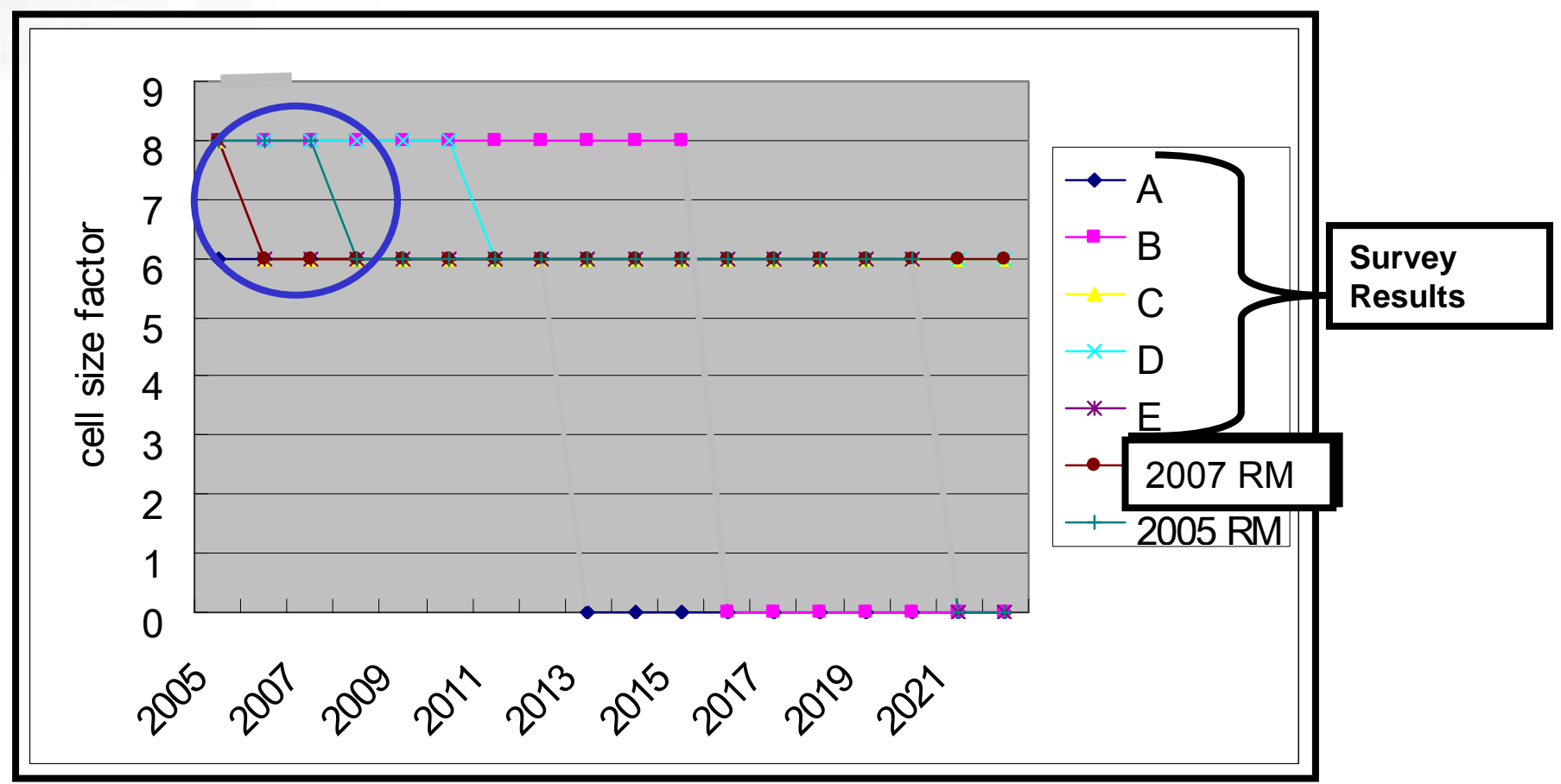
# DRAM Product Generation (in Gb)



**1 year delay against 2005 version**



# Scaling of Cell Size Factor, a



**6F<sup>2</sup> starts in 2006 (two year pull-in)**



# Outline

- **Scope and Subcategories**
- **Logic**
- **Non-Volatile Memory**
- **DRAM**
- *Reliability*

# Reliability: Key Issues

- **Reliability risk is growing**
  - **New materials (e.g., high-k/metal gate; low-k) and new devices (e.g., FDSOI) and new packaging**
    - **Introduce new and/or modified failure mechanisms**
    - **Mechanisms need to be identified, modeled and controlled**
    - **Have less-than-historic time and resources to ensure reliability**
  - **Need new Design for Reliability tools and reliability screens**
- ***Need to sustain current high reliability levels regardless of unprecedented changes***

# Reliability Key Challenges

- *Transistor reliability*
  - TDDDB and NBTI
  - $V_{th}$  shifts due to traps & carrier injection
- *Interconnect reliability*
  - Cu electromigration and stress voiding
  - Electrical breakdown of dielectrics, esp. low-k
- *Packaging reliability*
  - New mechanisms associated with Pb-free solders
  - Electromigration in package traces
- *Reliability in extreme and/or critical applications*
  - Automotive (hot under hood)
  - Military (rugged, shock, dust, and high temperature)
  - Space (rad hard)



# Summary

- **Logic**

- Numerous and rapid technology innovations required
- Metal gate and high-k projected for 2008
- Multiple parallel paths
- Sustaining historical transistor performance scaling will be difficult

- **Memory**

- DRAM: scaling continuing
- Numerous different types of NVM, with unique attributes and scaling scenarios

- **Reliability**

- Ensuring reliability for numerous and rapid technological innovations is a critical challenge
- Nevertheless, need to sustain current high reliability levels

