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**The Fraunhofer  
Center  
Nanoelectronic  
Technologies**

**a new Approach in Cooperation of Research  
and Industry**

**ITRS, Annecy 25.4.2007**

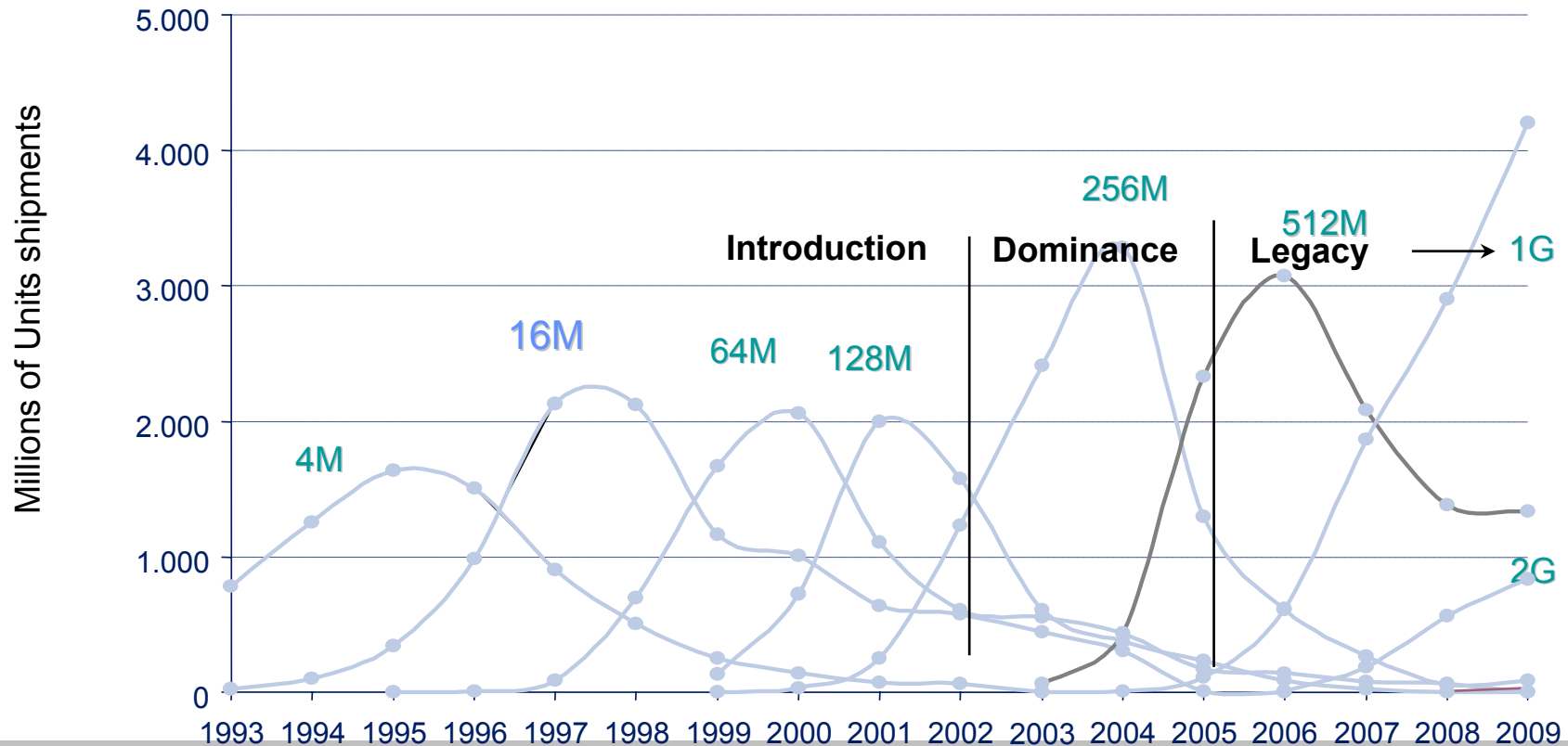
**Peter Kücher**

# Outline

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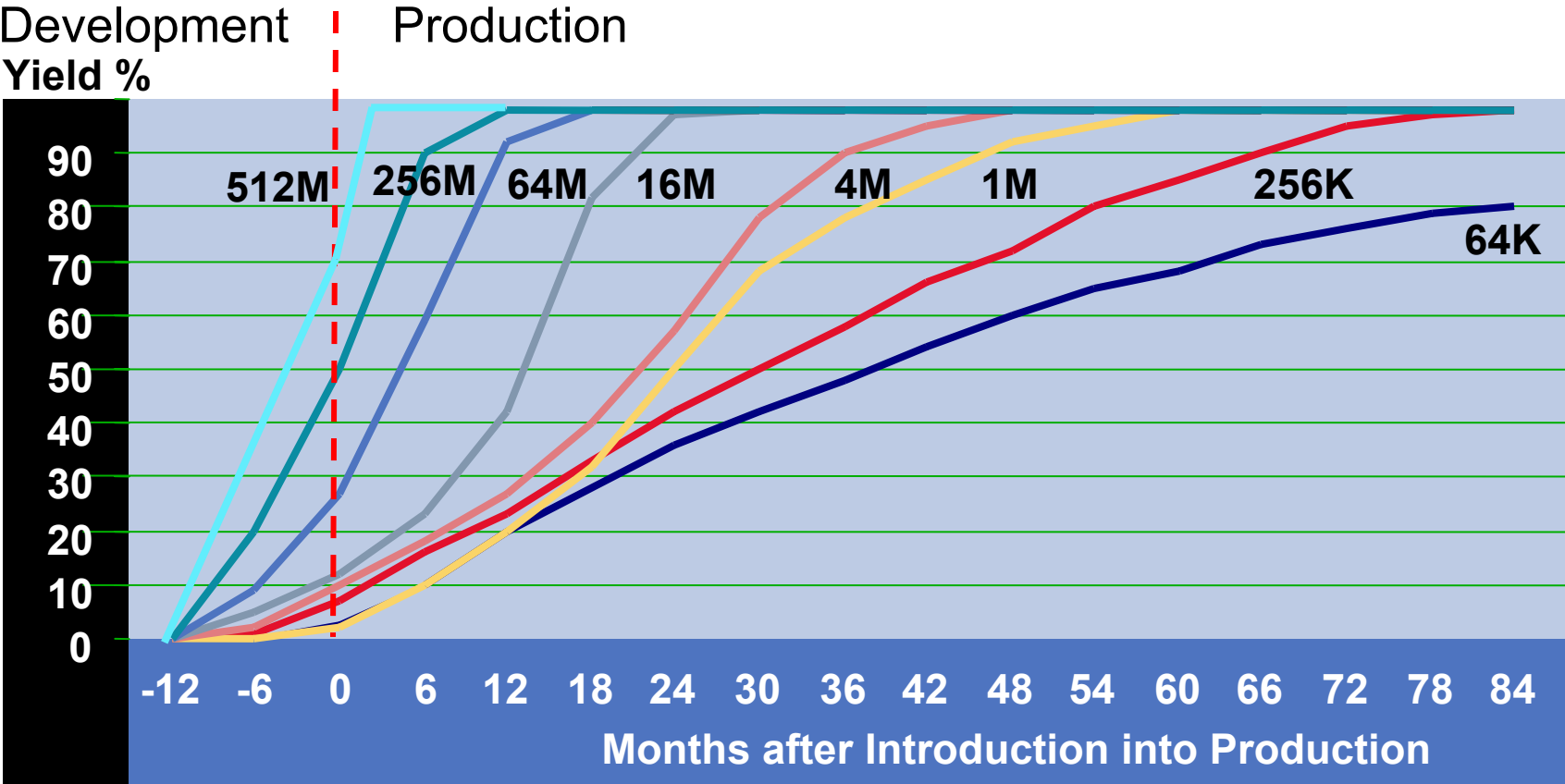
- 1** **Nanoelectronic Challenge**
- 2** **Concept**
- 3** **European Cooperation**
- 4** **Status and Research Areas**

# Product Life Cycle: DRAM (Example 256M)



- **Product Life Cycles:** still 2 – 3 years dominance of leading edge
- **Legacy Products :** stable prices, fewer supplier , shorter life time than in the past
- **Volume:** Higher volume/invest fabs demand driven, higher risk for **process transfer**

# Average Probe Yields & Ramp: DRAM (w/redundancy)



Source: VLSI Research

# Outline

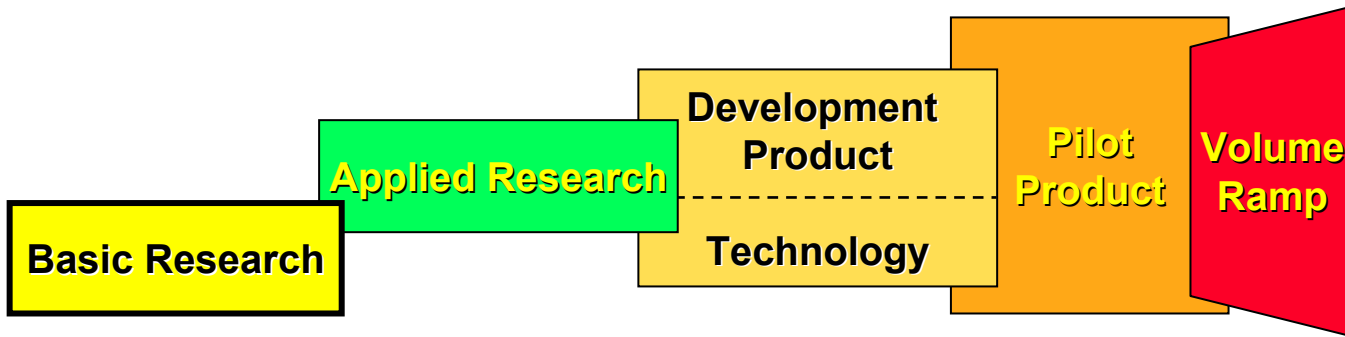
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# Research Challenge: ... Fast Integration of Innovative Processes/Technologies and Equipment into Manufacturing

Sequential

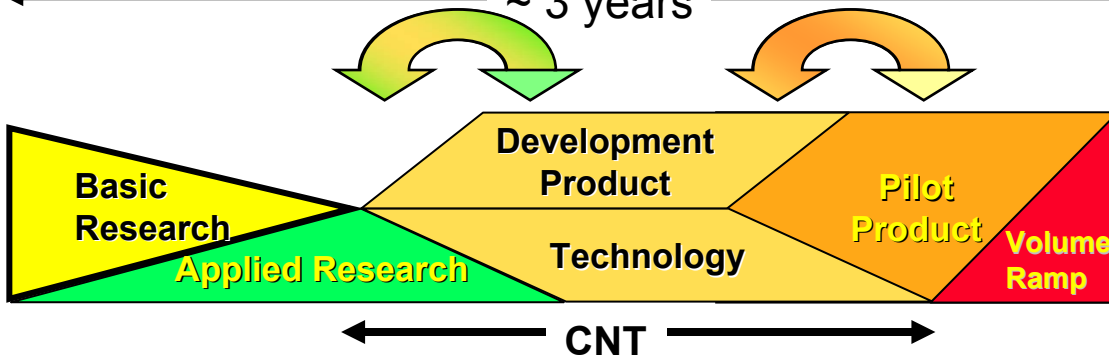
← > 5 years →



- No Feedback
- Independent
- **Technology driven**

Integrated

← ~ 3 years →



- Fast Feedback from market
- Interacting
- **Application driven**

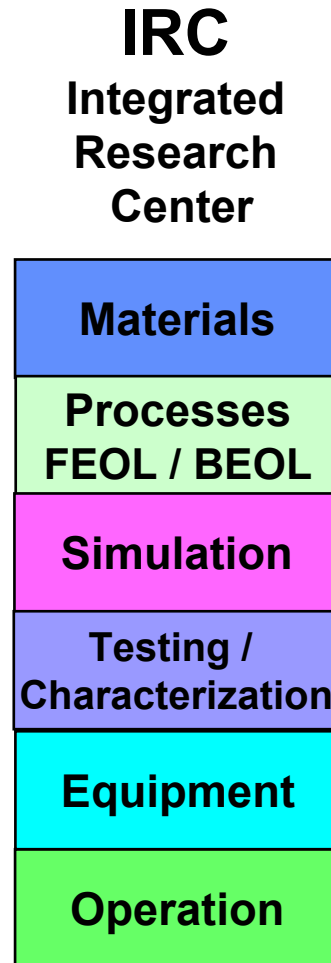


# Research Organisation

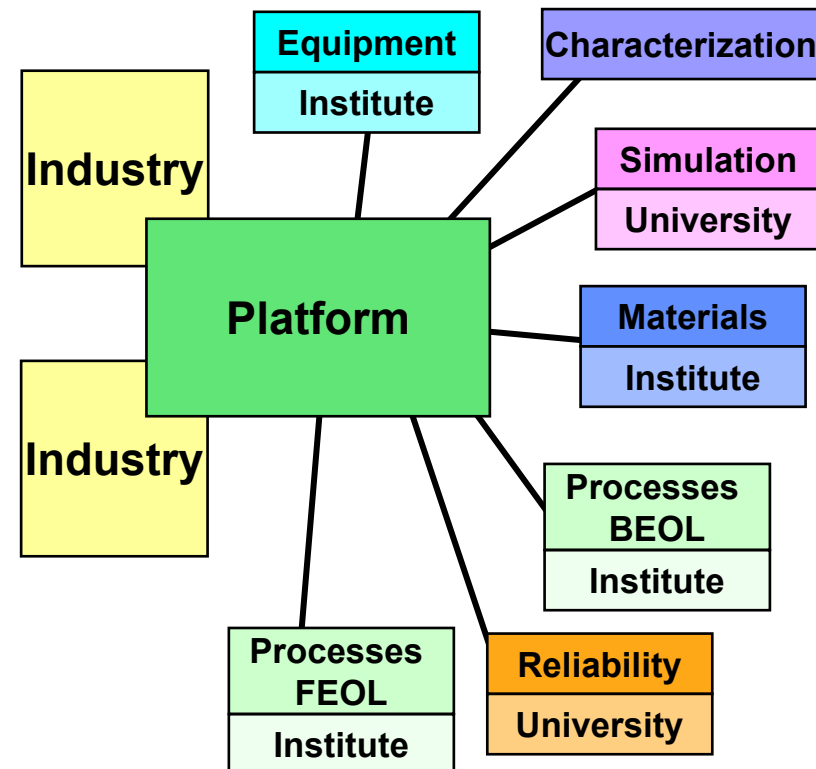
## Competence and Know-how Integration

### Characteristics

- High invest for equipment and infrastructure
- Risk sharing through *multi-partnership*
- Competence through networks and in cooperation with platforms

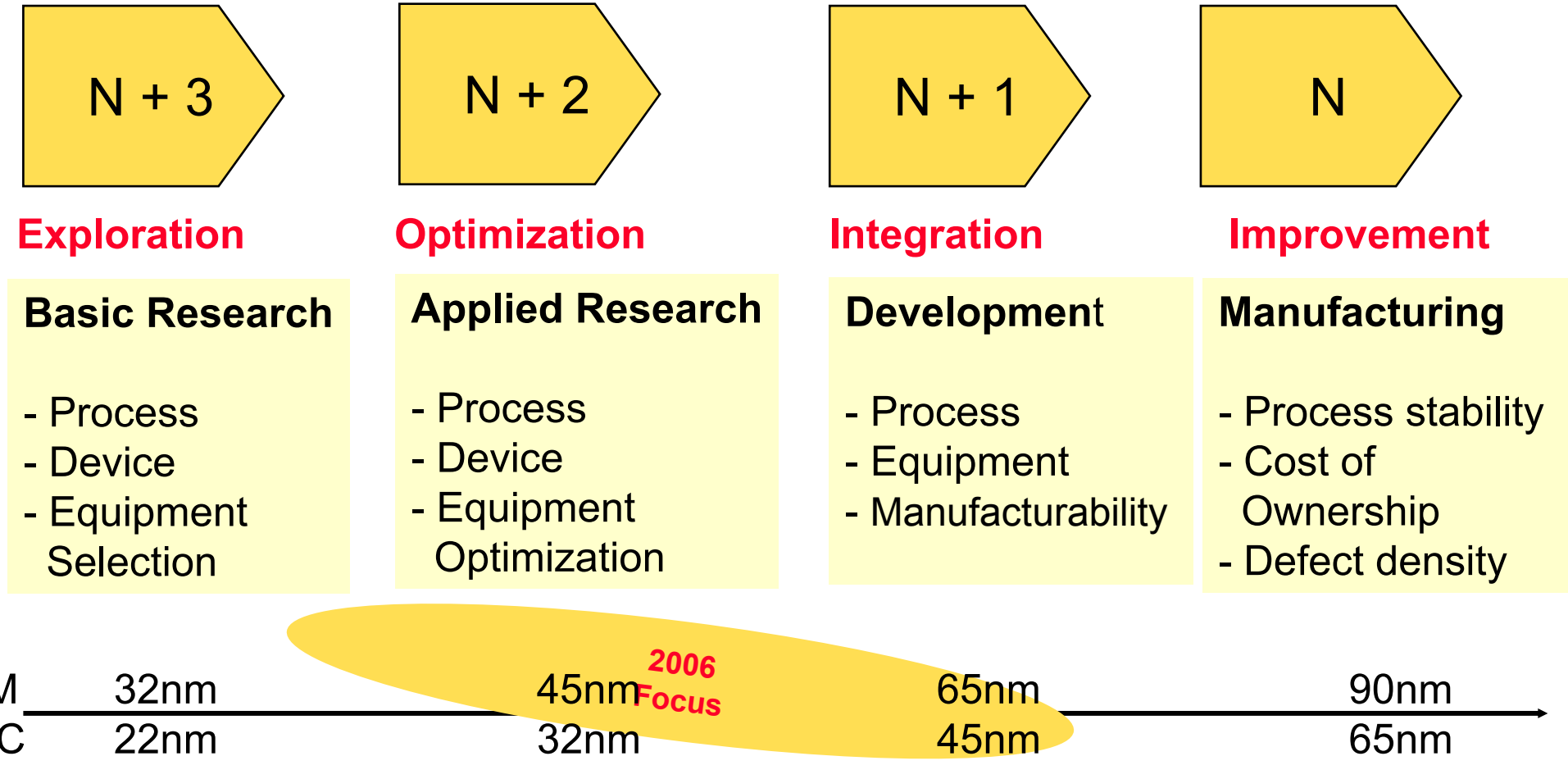


**RP**  
Research Platform – Link to Manufacturing  
of *dedicated partners*

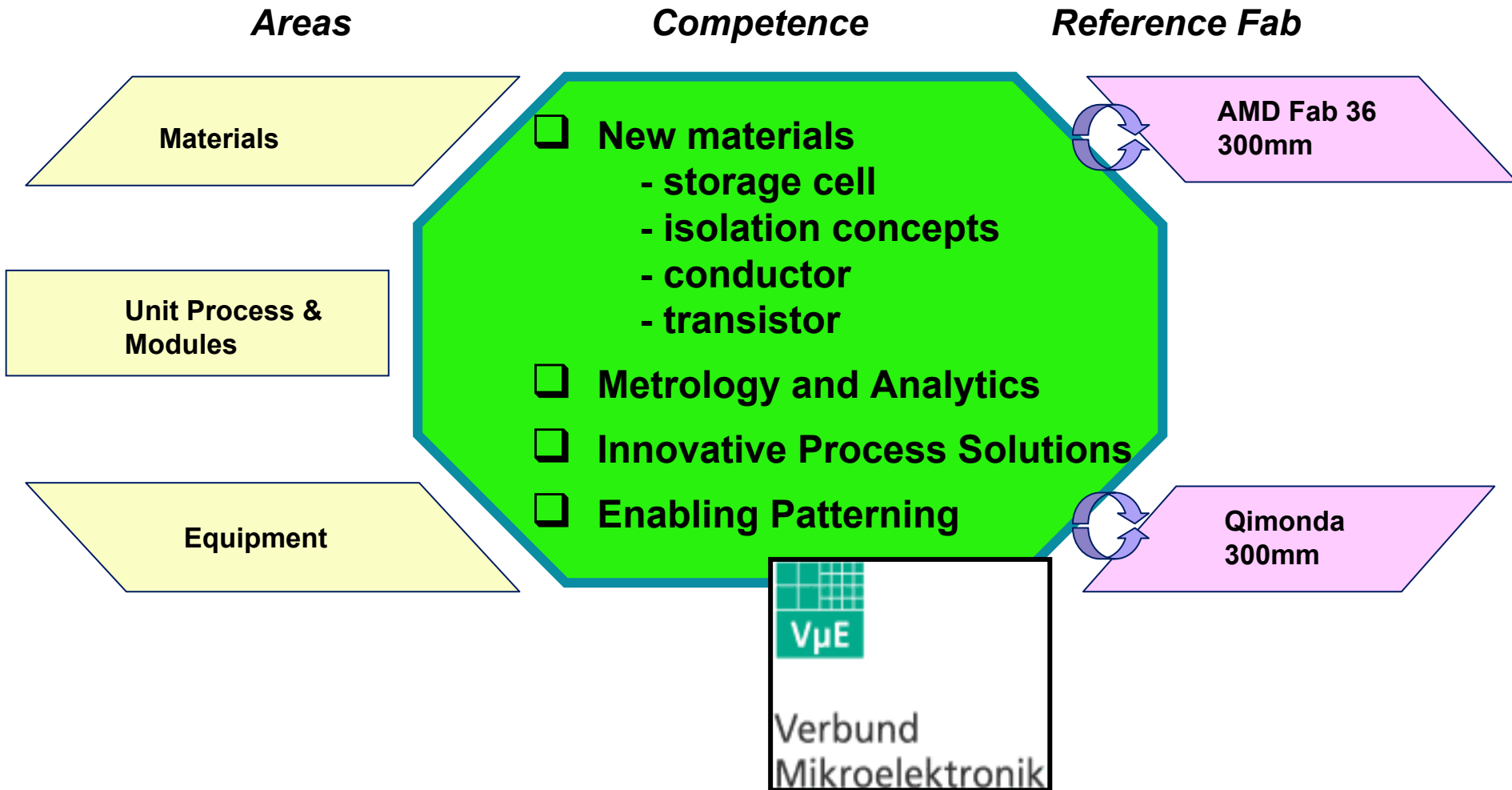


# Timing for Roadmap-related Activities

N: Technology Node in Production



# CNT Competence Areas

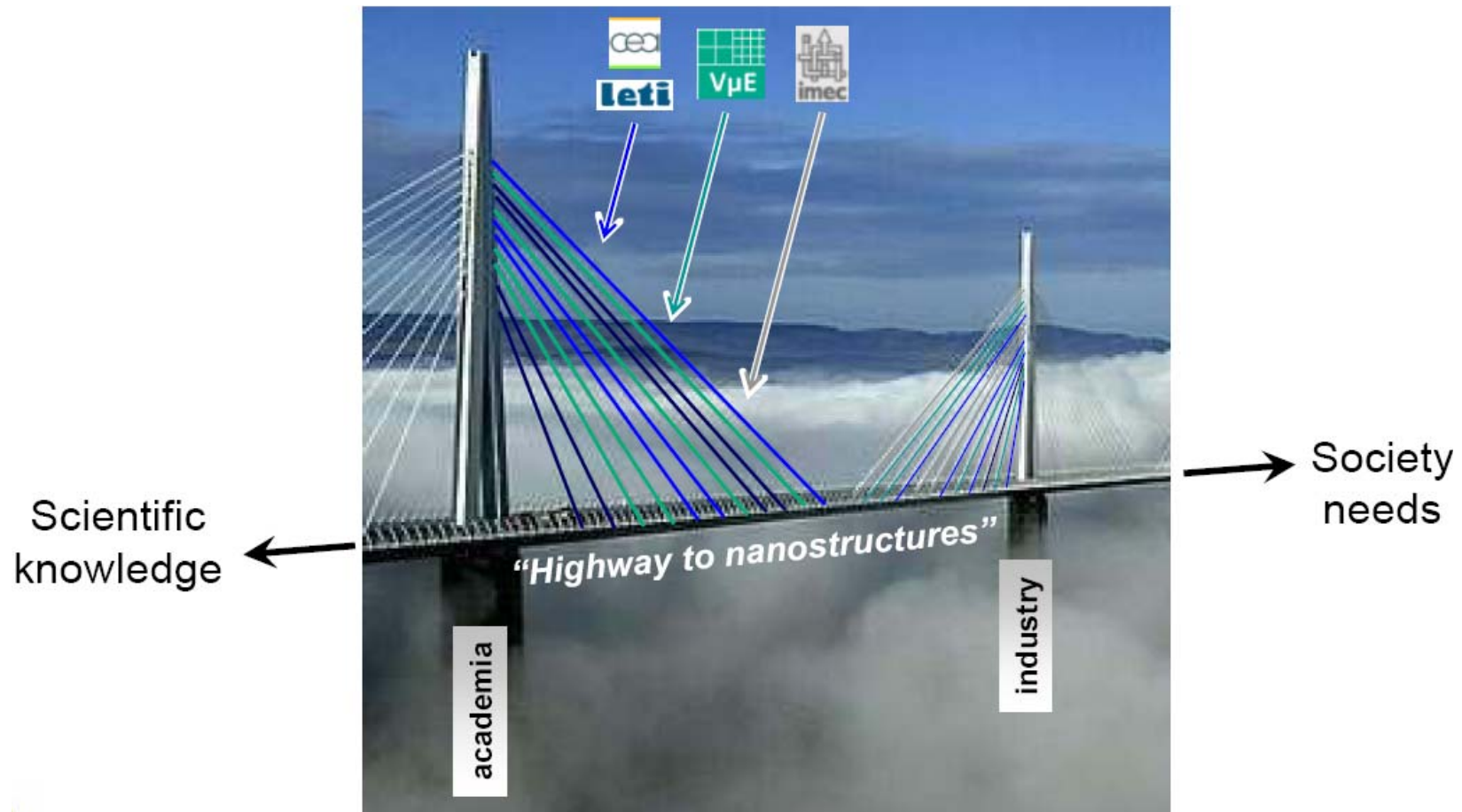


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# The Highway to Nanoelectronics



# Outline

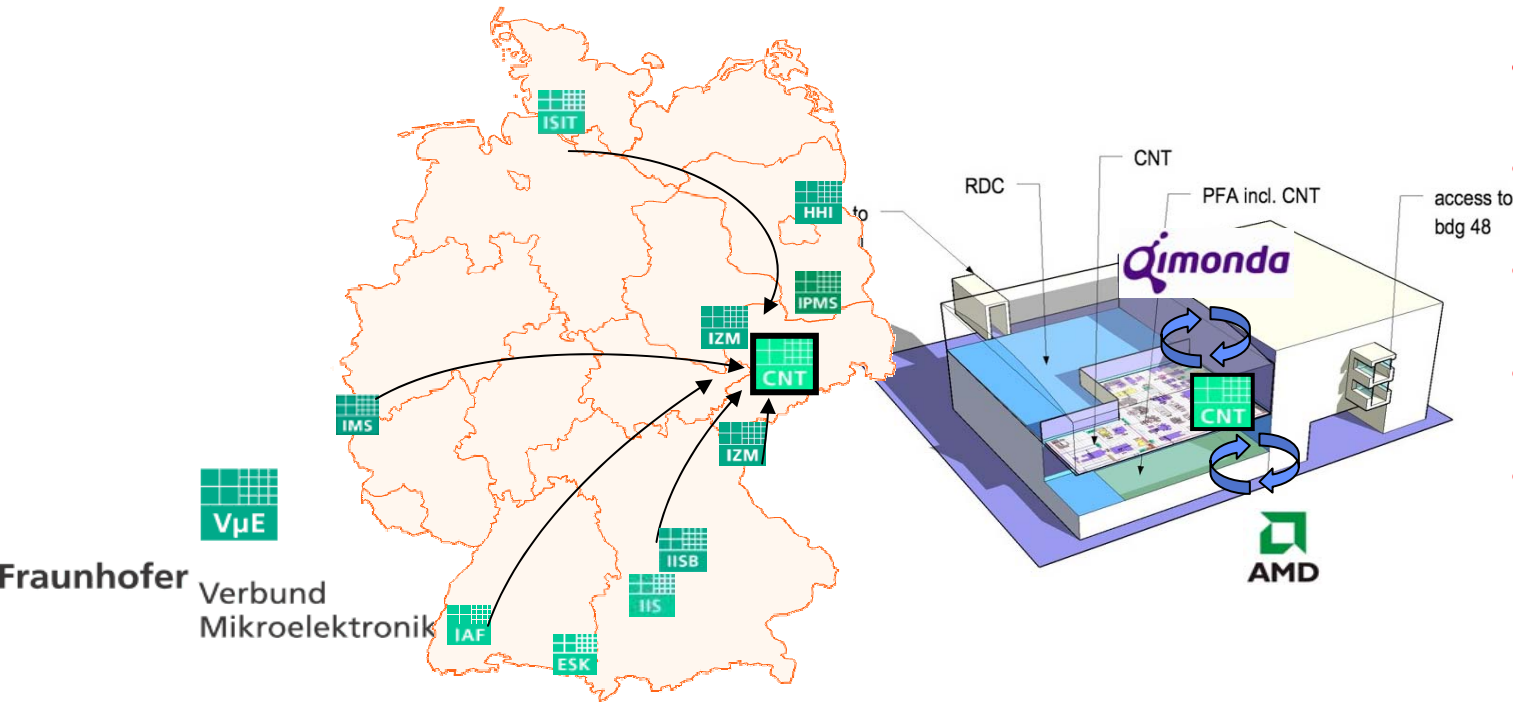
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# The CNT Model

Research docking...

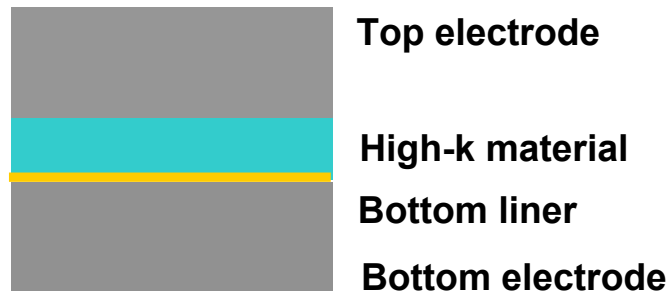
...into Manufacturing



- Significant wafer volume
- Realistic environment
- Cost efficiency
- Fast Feedback
- Learning Speed

# Thermal Annealing: Diffusion Control

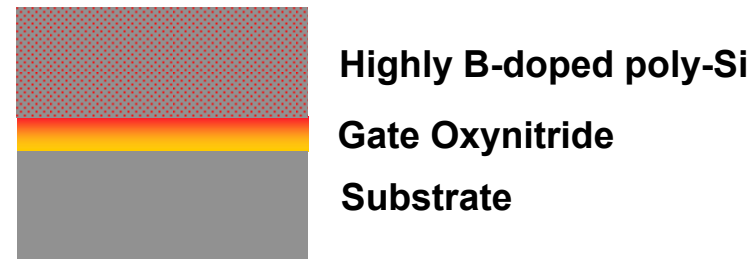
## Capacitor: high – k



- Total EOT of dielectric stack < 2 nm
- Bottom liner thickness < 1 nm
- **No interdiffusion and silicidation**

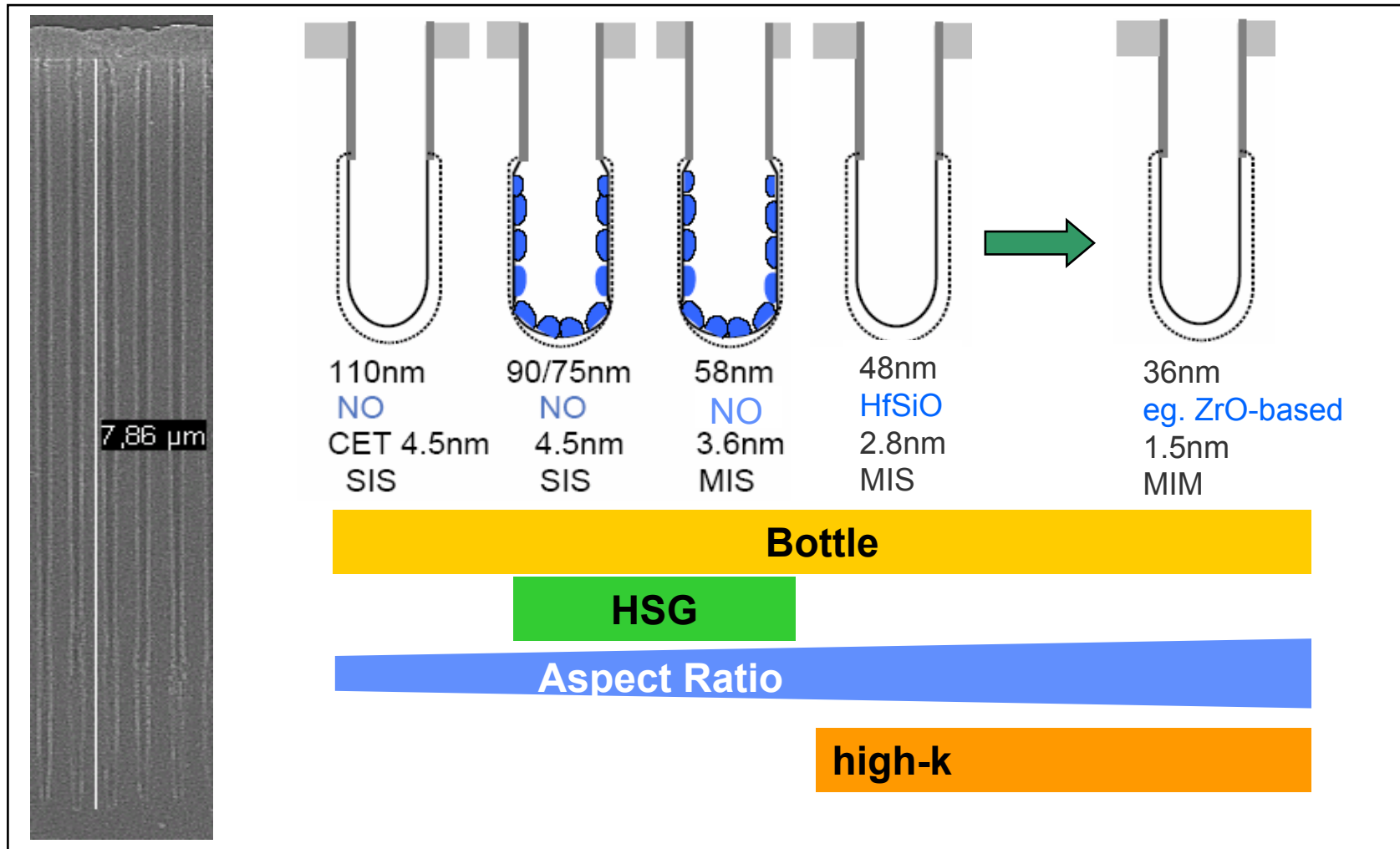
- Shrinking of layer thickness in active area
- Reduced thermal budget
- ultra-short anneal processes to control , reduce or avoid diffusion.

## Transistor: p – FET (DWF)



- Thickness: gate dielectric < 2 nm
- Gate poly-Si electrode: >  $10^{20}$  B / cm<sup>3</sup>
  - Substrate channel: <  $10^{17}$  B / cm<sup>3</sup>
  - **Avoid Diffusion of B from gate to channel**

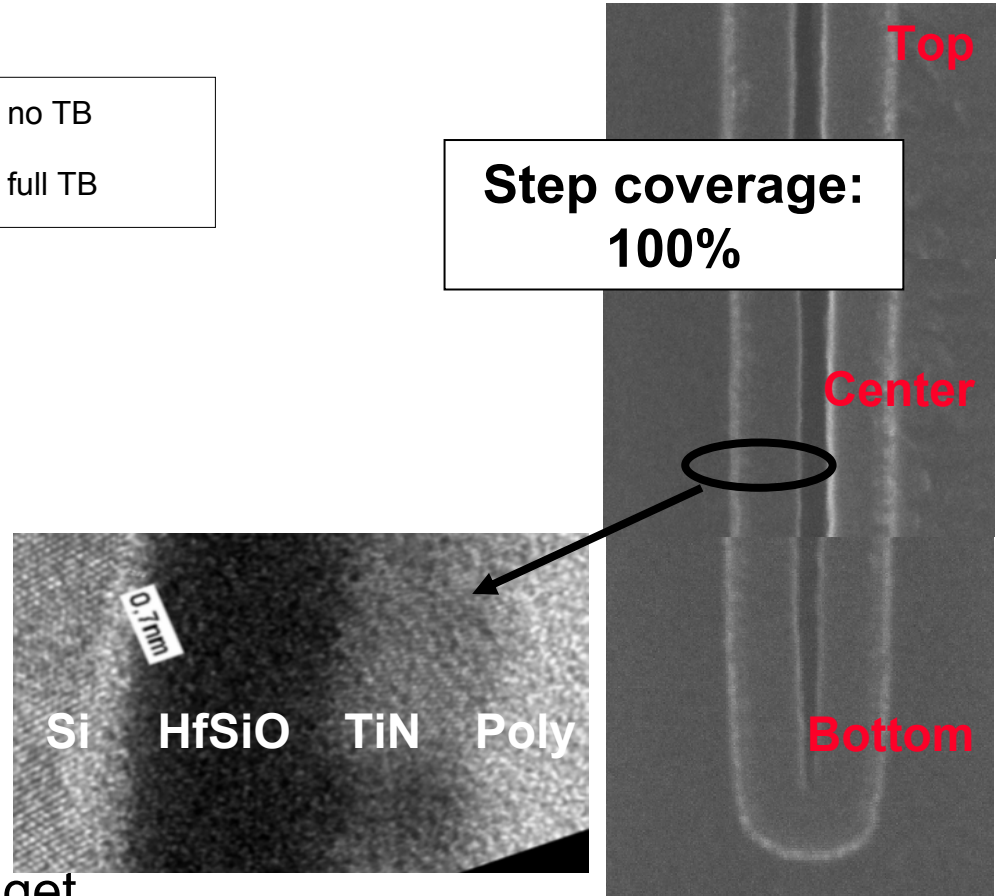
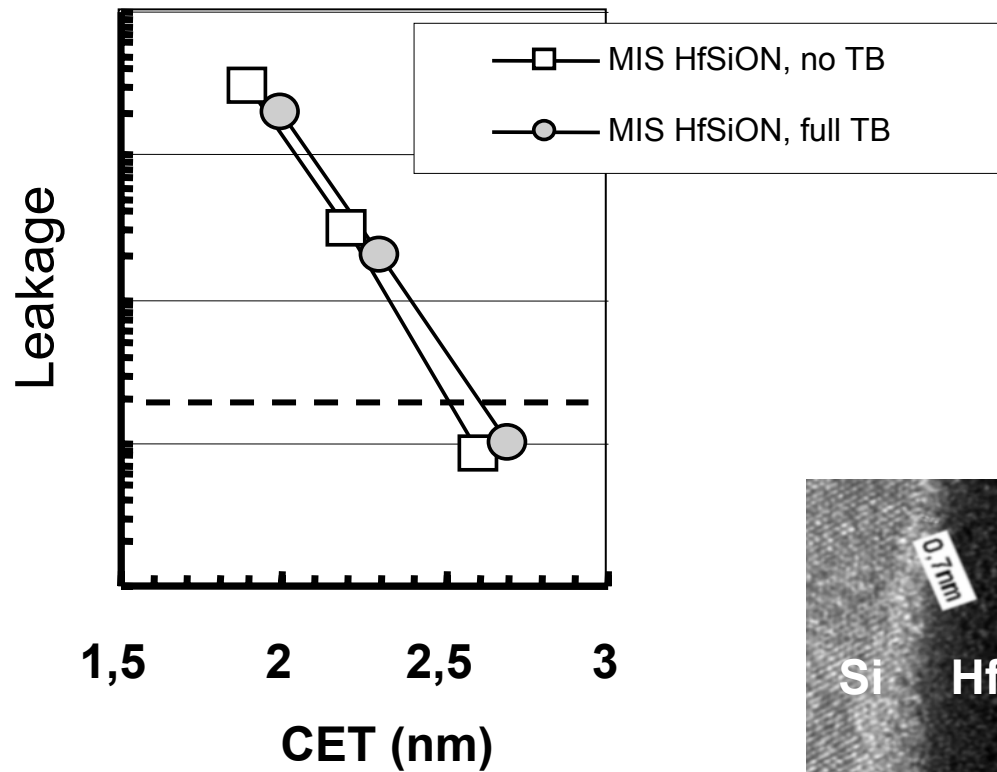
# High k Materials: Trench Capacitor



Material Scaling needed: ZrO based MIM capacitor

# Trench Capacitor Development: MIS w/HfSiO

VLSI TSA W. Mueller

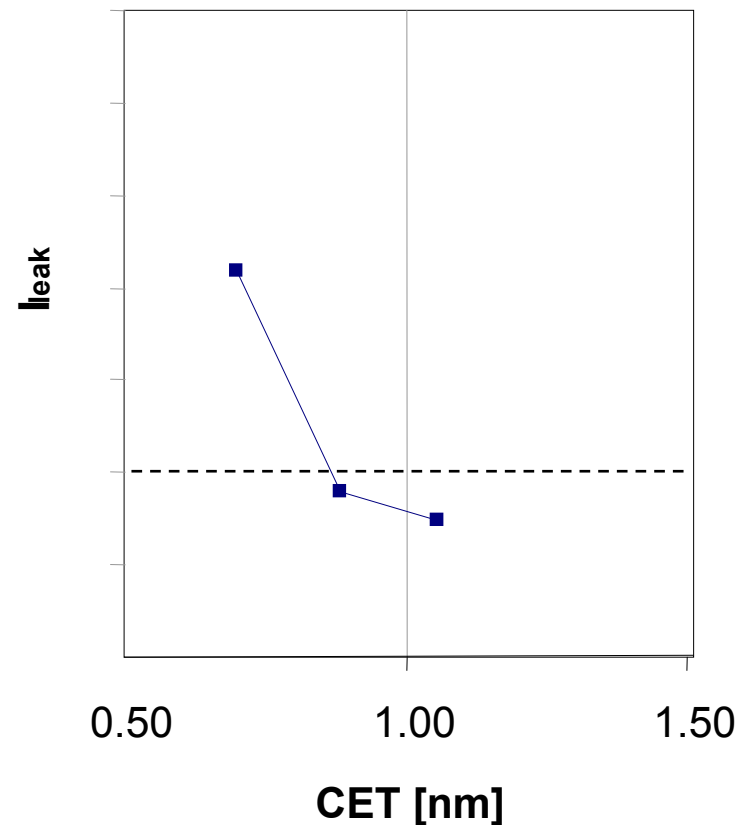
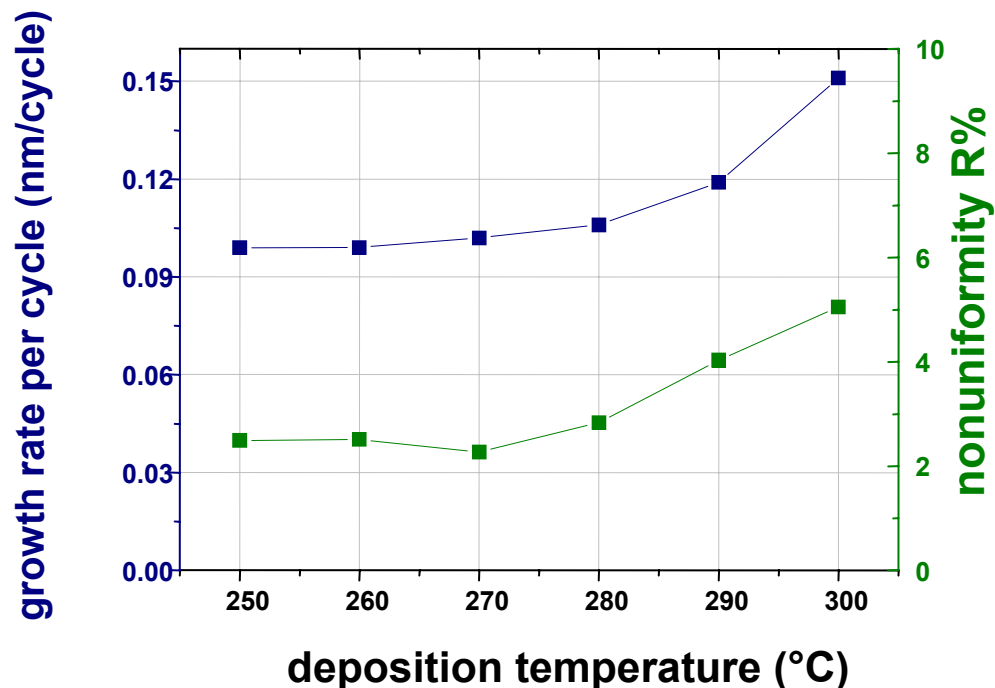


- CET= 2.6nm within full thermal budget

# ALD Production Tool w/high Screening Capability

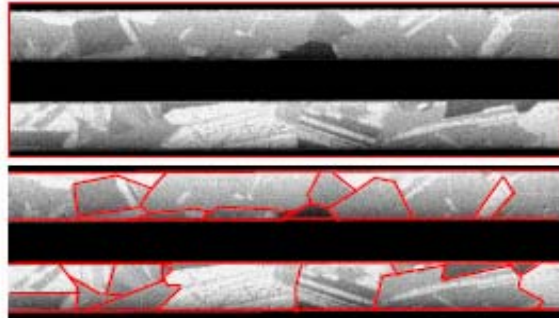
## Example: Zr-based MIM Capacitor Development

### ZrO<sub>2</sub> ALD



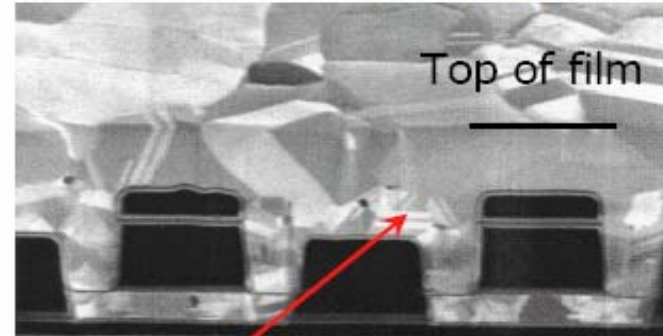


# Cu Metallization: Grain Size Control

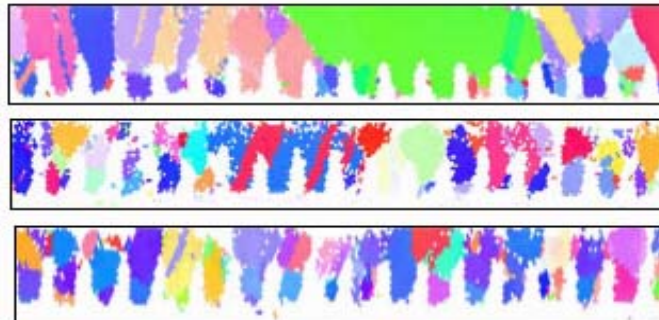


While top down SEM picture still suggest near bamboo structure even for smallest lines

*Besser et al, J. Electronic Materials (2001)*



Cross sections reveal random small grain assembly in narrow features

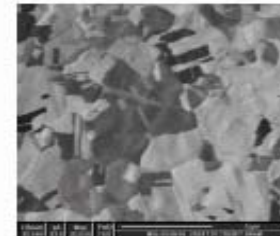


**2x standard**

**standard**

**0.5x standard**

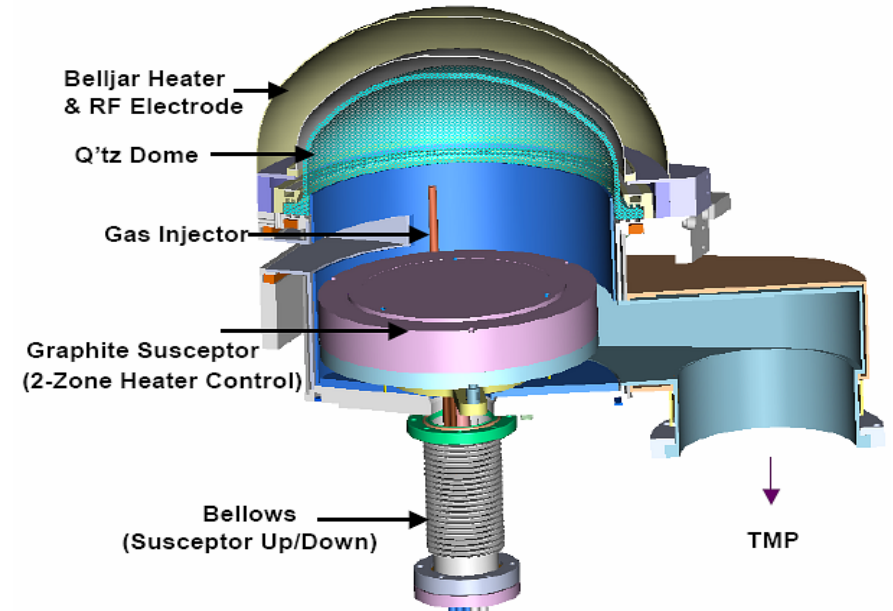
Increase grain size of copper with increased overburden during plating



I. Zienert, MALAB

# Why UHV-CVD ?

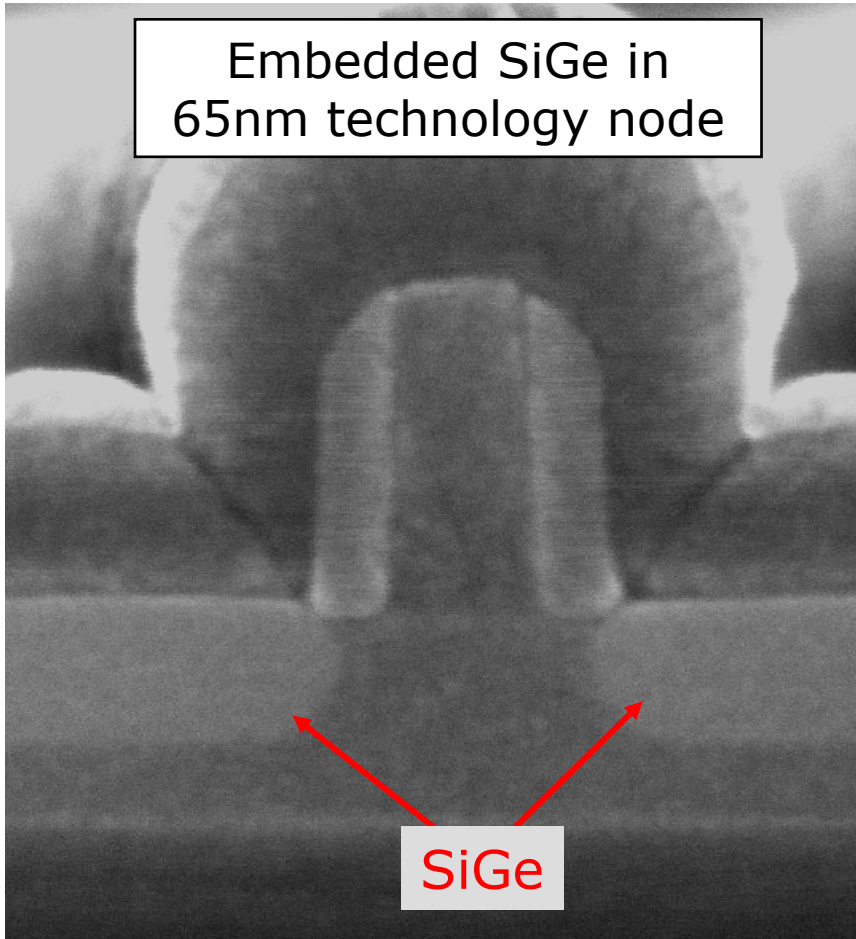
	LPCVD	UHVCVD
Base pressure	10 <sup>-4</sup> torr	10 <sup>-8</sup> torr
Process pressure	1..100torr	3·10 <sup>-4</sup> torr
Gas flow	laminar	molecular (Knudsen)
Preclean	Prebake @ 850C	Plasma @ 200..350C
Process Temp.	550..800C	500..750C



The UHV chamber concept provides:

- minimal pattern loading (due to different precursor flow conditions)
- very low process temperatures including the preclean
- very low gas consumption

Embedded SiGe in  
65nm technology node



Embedded SiGe is an established production process in AMD.

### Advantages of UHV-CVD:

- reduced thermal budget
- SiGe growth is not influenced by the size of the structure (no loading effect)
- bottom up fill (no sidewall growth observed)
- Germanium concentrations up to 40% demonstrated