

A user's guide to MASTAR 4

MASTAR –

- **M**odel for **A**ssessment of **c**mo**S** **T**echnologies **A**nd **R**oadmaps

MASTAR 4 is compatible with Windows 95, 98, NT4, 2000, & XP. Nevertheless, some Windows display setups may be source of corrupted Mastar graphics. If this is the case, we advise to

- setup standard fonts in the Properties/Appearance window (available with the right-button click on the desktop Windows screen)
- adjust the screen resolution to 1024x768 pixels or more in the Properties/Settings window (available with the right-button click on the desktop Windows screen)

The philosophy of MASTAR

Mastar 4 is a computing tool especially conceived for the calculation of the electrical characteristics of advanced CMOS transistors based on different technologies such as planar bulk, Double Gate (DG) or Silicon On Isolator (SOI). The calculation is based on analytical drift diffusion equations, which depend directly on the major technological parameters, such as gate length, channel doping, oxide thickness, etc. This application allows the user to evaluate *immediately* the impact of these technological parameters on the main transistor characteristics such as the threshold behavior, performance values or time delay. Moreover, the influence of “physical” secondary parameters such as mobility, poly depletion and dark space can be visualized giving a deep insight in the physics of CMOS devices. An extension towards ballistic transport is planned and will be included in one of the following releases.

The installation of the MASTAR 4 package

Mastar 4 is delivered as a compressed package of files. After reception, please create a MASTAR folder where you copy the whole stack of files. For execution, just click on the MASTAR3.exe file. Whenever you create or modify files (e. g. *profile* files, *plot* files or result files) within MASTAR 4, these files will be generated or updated in this current folder. In an analogous way, profile or plot files can only be loaded if they are located in this current folder. So make sure that they haven't been moved to a different folder.

Quick starter...

The MASTAR application is made for quick assessment of the impact of the various transistor parameters on the static and dynamic transistor performances. In this introductory chapter we would like to give an insight on the basic functionalities of MASTAR.

We suggest choosing for the first approach the work space “Device”. This gives you a good introduction into how MASTAR 4 works. After accepting the user agreement, please click on the button “Device” on top of your screen. You will open a workspace which looks as illustrated in Figure 1.

You will see on the left side the principle input window displaying the technological choices and parameters: the CMOS technology (Bulk, SOI, DG), the ITRS parameters such as L_g , T_{ox} , N_{ch} , V_{dd} , the booster buttons (e. g. Metal Gate, Strain) and some additional calculation modules on the bottom of the window. On the top of your screen you have the principle output window summarizing all the principle calculation results of the transistor such as performance, threshold, delay, mobility, etc.

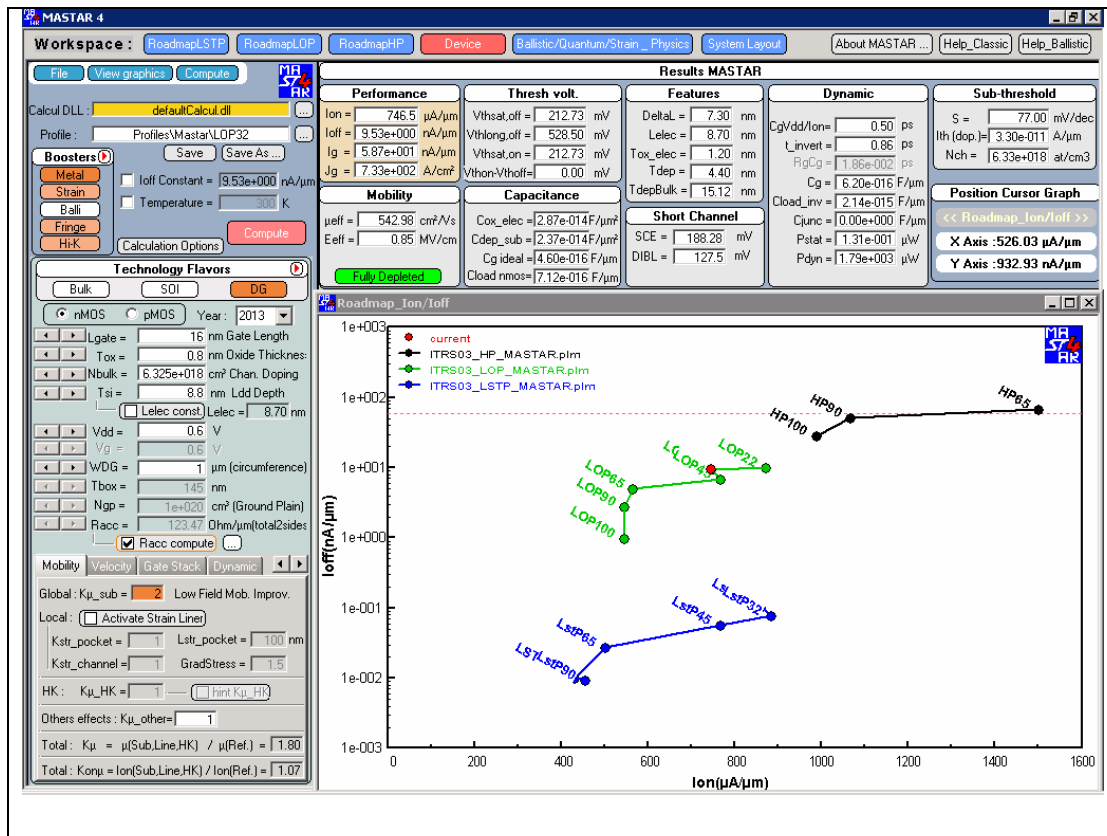


Figure 1: MASTAR 4: global view of the workspace “Device”.

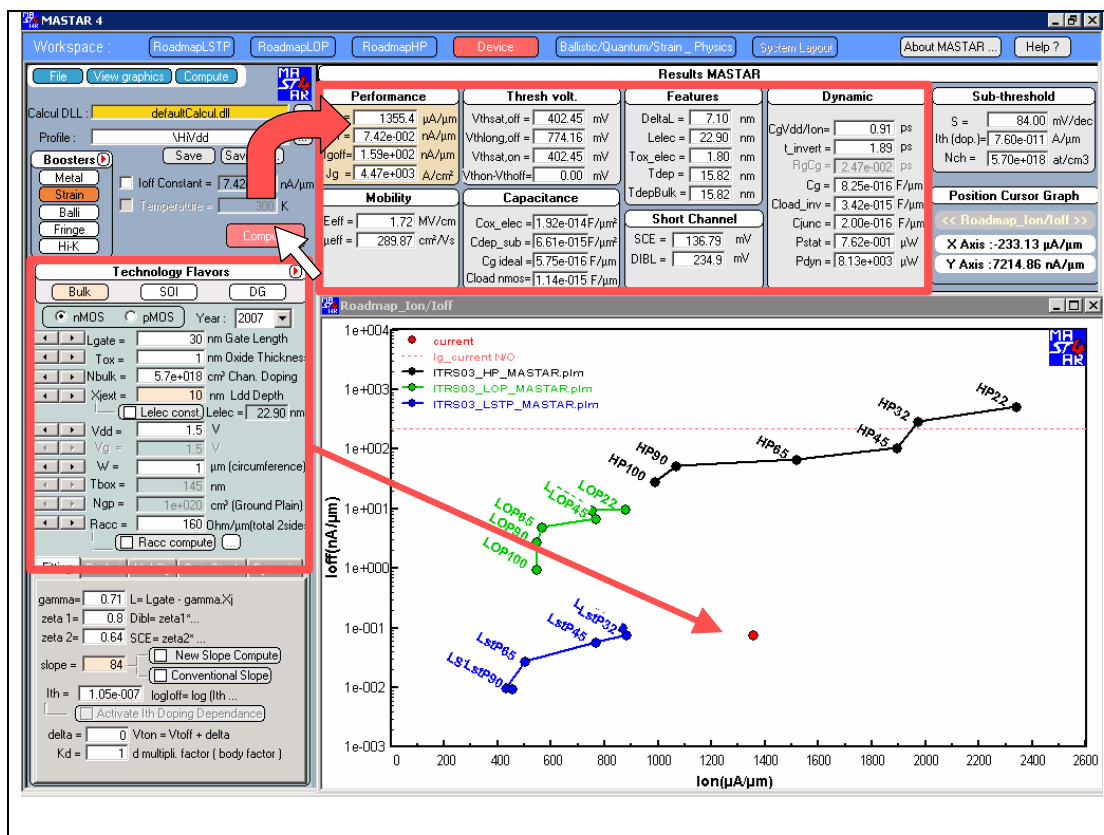
Just below you find the output graphics. By default, the principle output graphics is the so-called Roadmap Ion-Ioff graphics displaying the performance values of the transistor on a log(I_{off}) versus I_{on} chart together with the ITRS 2003 Roadmap targets.

EXAMPLE:

Let's imagine the user first wants to assess the performance value of a (fictitious) bulk transistor with the following features: a gate length $L_g = 30nm$, an ideal (not leaky) SiON oxide with a physical thickness $T_{ox} = 1nm$, ultra-shallow LDDs with $x_j = 10nm$, a channel doping $N_{ch} = 5.7e18cm^{-3}$ and the apply voltage $V_{dd} = 1.5V$. In addition, we switch the Strain Booster button on, which gives us a two-fold

mobility enhancement. In a second time, we might be interested in evaluating the benefit of the replacement of the poly-Si gate by a metal gate electrode with equal work function.

In the first step, we have to enter the input parameters in the input parameter window. Once all values are entered you can read the performance value either in the numerical output window or as a red dot in the Roadmap ion Ioff graphics window (cf. Figure 2).



the Roadmap Ion-Ioff graphics and click on the right mouse button: a submenu pops up giving access to the option Load / Delete Profile.

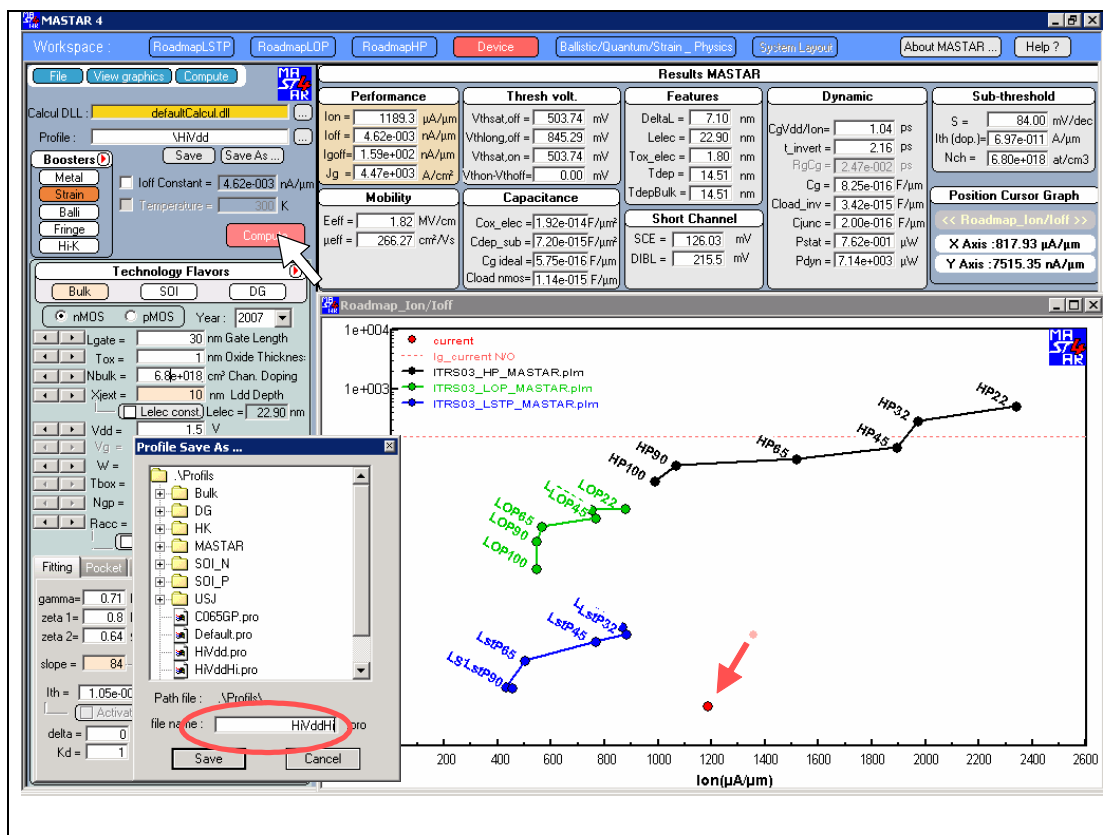


Figure 3: Saving the new profile after decrease of the channel doping.

Now, we have three profiles, which will be used to create an Ion/Ioff plot file. Within MASTAR, a plot file is defined as a set of one or several profiles and is used for graphical presentation of the corresponding performance values on the Roadmap Ion-Ioff graphics. For this purpose, you click on the right mouse button. The submenu pops up and you choose the *Create / Modify Plot...* command. Inside the dialogue window, you will be asked to enter the new plot file name – we call it “baseline” for this example - and to select the profiles, which it should contain. The choice will finally be validated by the *Apply Change* button (cf. Figure 4).

In order to display the content of the plot file in the Roadmap Ion-Ioff window, you have to choose the *Load / Unload Plot...* command from the submenu. The user can now select one or several plot files for display on the Roadmap Ion-Ioff graphics; for our example we choose the plot file “baseline” (cf. Figure 5).

The display of plot files is very useful for comparison reasons. In our case we like to assess the benefit of the substitution of the poly-Si gate by a metal gate. For this purpose, we reload the “HiVdd” profile and click on the metal gate booster button. The performance data point is now shifted to the right of our baseline indicating the performance enhancement due to the poly-depletion suppression. Note that in this case both Ion and Ioff are modified as the resulting CET value acts directly on the threshold voltage (cf. Figure 6). In order to get rid of threshold voltage changes the user could have also activated the feature *Ioff=Constant* in the input parameter window. The channel doping would be now automatically adjusted to keep the off

current constant giving however rise to mobility changes due to higher or lower channel doping levels.

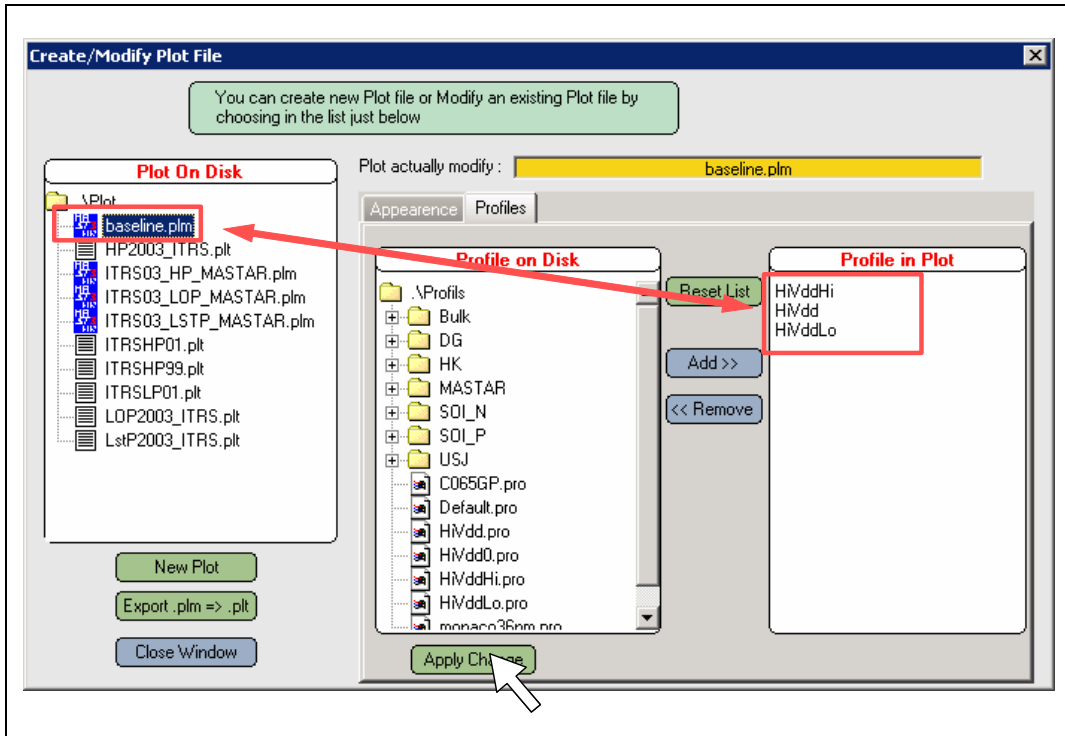


Figure 4: Creation of a new plot file for display in the Roadmap Ion-Ioff graphics.

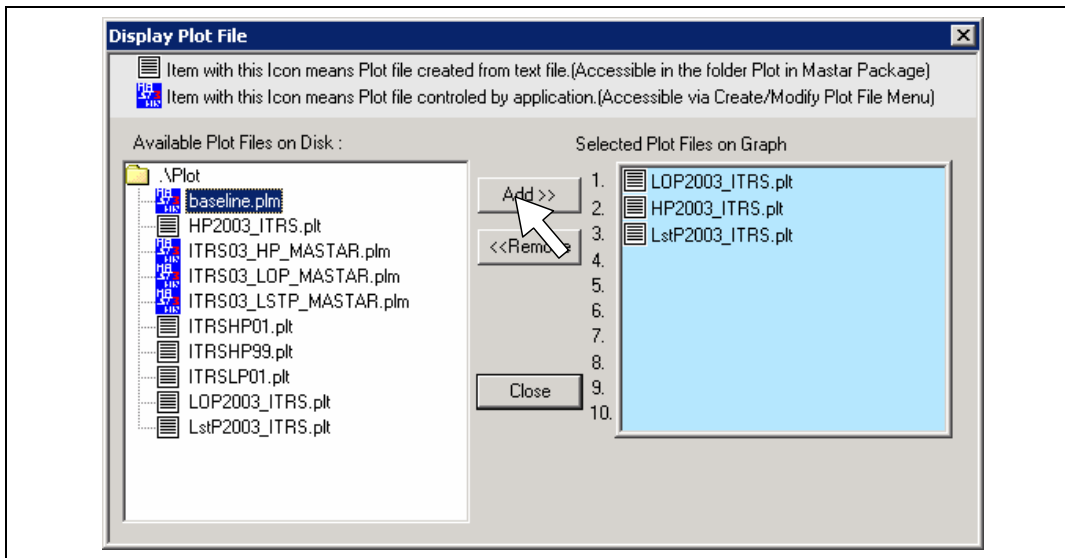


Figure 5: Selecting the plot file for display in the Roadmap Ion-Ioff window.

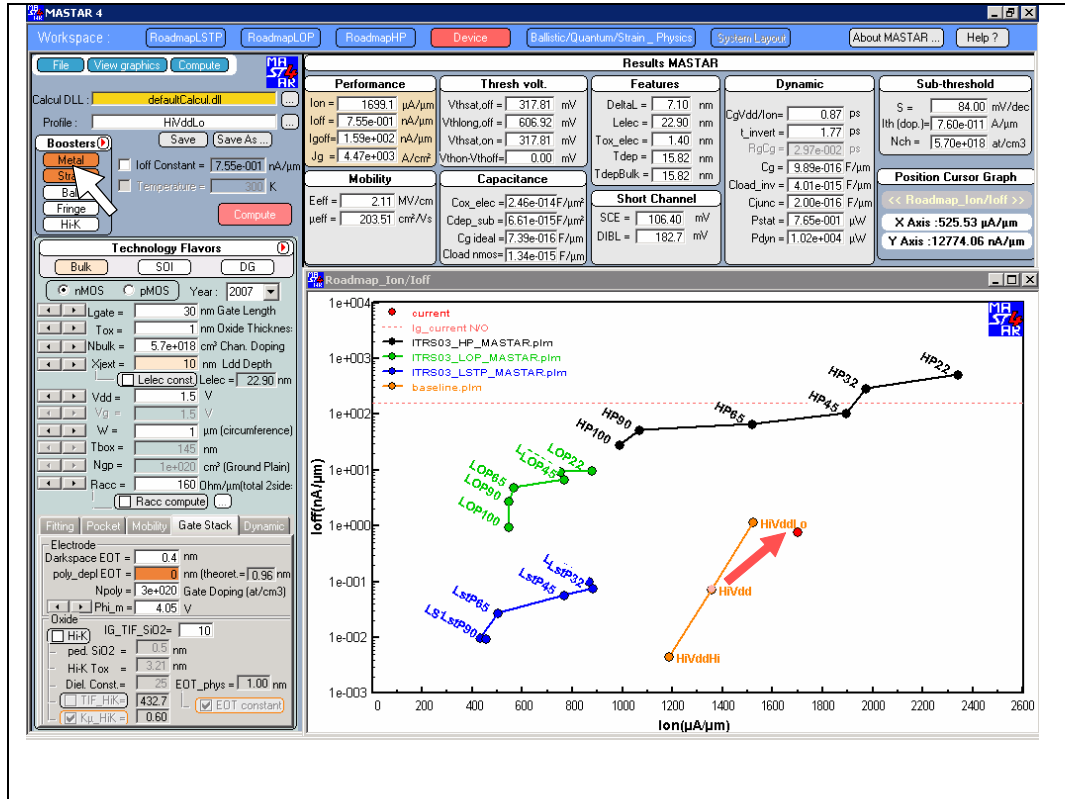


Figure 6: Example: the benefit from the substitution of poly-Si by metal as a gate electrode for a 65nm LSTP technology.

MASTAR's principal functionalities

Now let's have a more complete picture of the MASTAR 4 functionalities. Having started MASTAR 4 the user will be asked to choose between the workspaces "Device" and "Roadmap". The workspace "Device" is useful for the understanding of the physics of one given technology whereas the menu "Roadmap" is especially conceived for constructing CMOS roadmaps composed of different "technology flavors" (Bulk, SOI, DG, etc) per node.

The working space "Devices"

The main dialogue window: a global view

After clicking on the "Devices" button the main dialogue window will appear displaying the principal technological parameters and computational choices.

You will be first asked to choose between different CMOS technologies: bulk, Double Gate (DG) and Silicon on Insulator (SOI).

The corresponding main technological input parameters such as gate length, oxide thickness, extension depth are listed below. These parameters can be directly entered or modified starting from a given value using the adjacent buttons. The input parameters for each technology are listed and explained in Table 1.

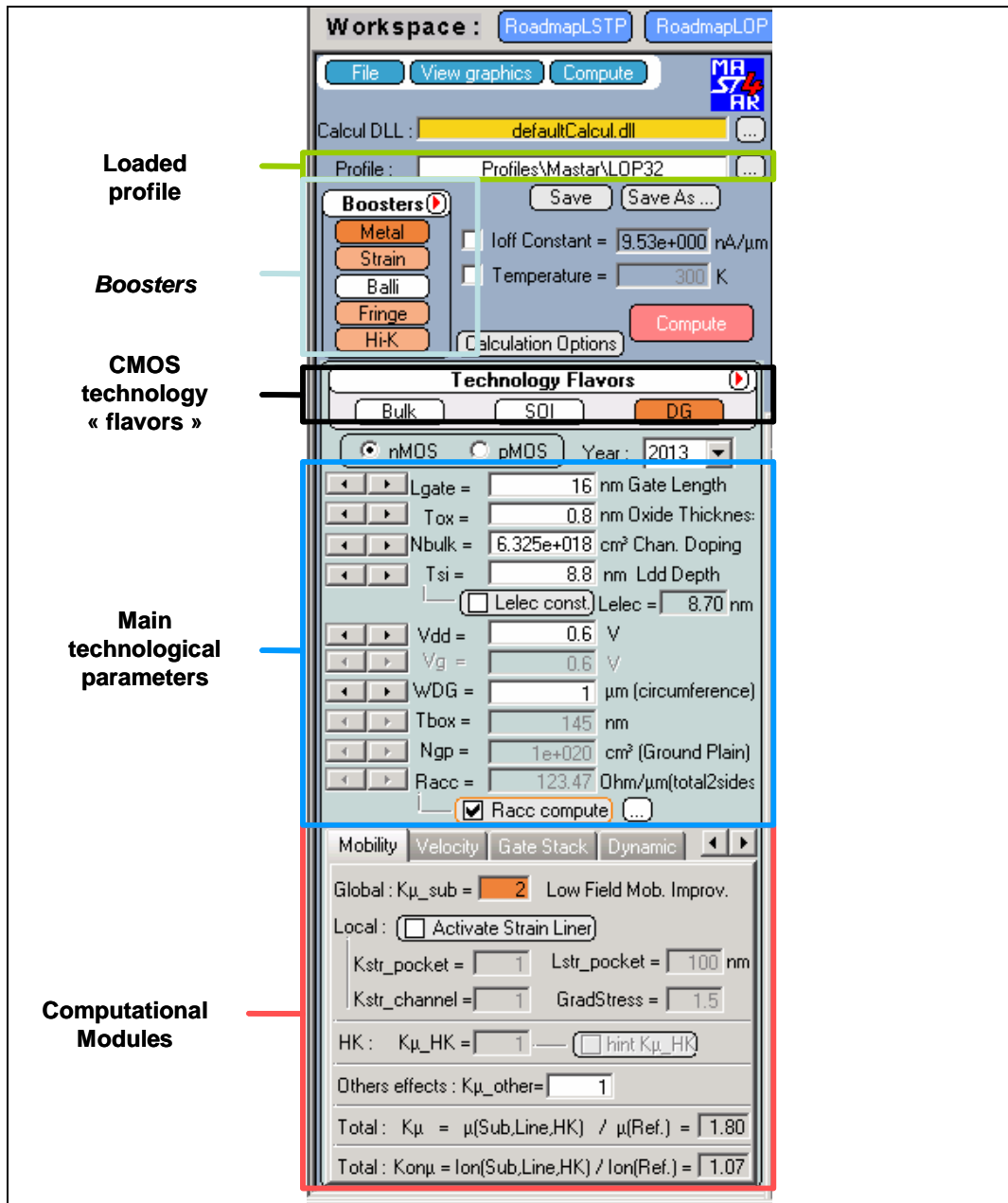


Figure 7: The MASTAR main dialogue window of the Devices application. The content of this window constitutes what is called (and can be saved as) the CMOS node profile.

The technology flavors

A very important feature is the choice of the CMOS technology between Bulk, DG or SOI. According to the choice of the “technology flavor”, some of the “bulk” parameters and equations are replaced in the calculations. The complete set of the equations for bulk and the alternative technologies can be seen in the annex.

The major changes are:

SOI:

In the MASTAR application, SOI stands for Fully Depleted SOI. A warning appears in the *Results* window when ever the conditions for Fully Depleted SOI are not fulfilled. Again, the main input parameter X_{jext} is replaced by the film thickness T_{si} . Furthermore the Buried Oxide Thickness T_{box} and the ground plain doping level N_{gp} are introduced as they play an important role for the effective SCE and DIBL values. The SOI equations are derived from the bulk equations. Notable differences lie in the expressions for T_{dep} (T_{si}) and for the DIBL as electrostatical couplings through the BOX occur. For more details, please refer to Annex E.

Parameter	Description	Dimension
Common		
L_{gate}	Physical Gate Length	nm
T_{ox}	Physical Gate Oxide Thickness	nm
N_{bulk}	Channel Doping (w/o Pockets)	atm/cm ³
V_{dd}	Operation Voltage (Gate and Drain Voltage)	V
W	Width	μm
Bulk		
X_{jext}	Extension depth	nm
DG		
T_{si}	Channel depth	nm
W_{DG}	Circumference (cf. Annexe D)	μm
SOI		
T_{si}	Channel depth	nm
T_{box}	Buried Oxide Thickness	nm
N_{gp}	Ground Plain Doping level	atm/cm ³
Resistance		
R_{acc}	Total Series Resistance (S and D)	none

Table 1: Description of the main input parameters from the main dialogue window for each CMOS technology.

DG:

In the MASTAR application, DG stands for a symmetrical double gate structure with common gate bias. The most important change is that the main input parameter X_{jext} is replaced by half of the film thickness T_{si} . The calculations are derived from the bulk equations based on a model of superposition of two planar CMOS transistors. However, corrections occur for the calculation of the depletion depth (T_{si} limited) and the threshold voltage (due to coupling effects between the two gates). Note that within the DG module the parameter W is replaced by W_{DG} which is the sum of all gate - channel interfaces and thus different from W_{layout} . So for a conventional planar DG structure $W_{DG} = 2 * W_{layout}$. For more details, please refer to Annex D.

Default Technology Flavor Parameters:

By clicking on the adjacent triangular button, the Technology Flavor Characteristics window opens and gives access to the fitting parameters of the different technologies (cf. Figure 8). For more detail on these parameters, please refer to the fitting parameter paragraph and to the corresponding annexes.

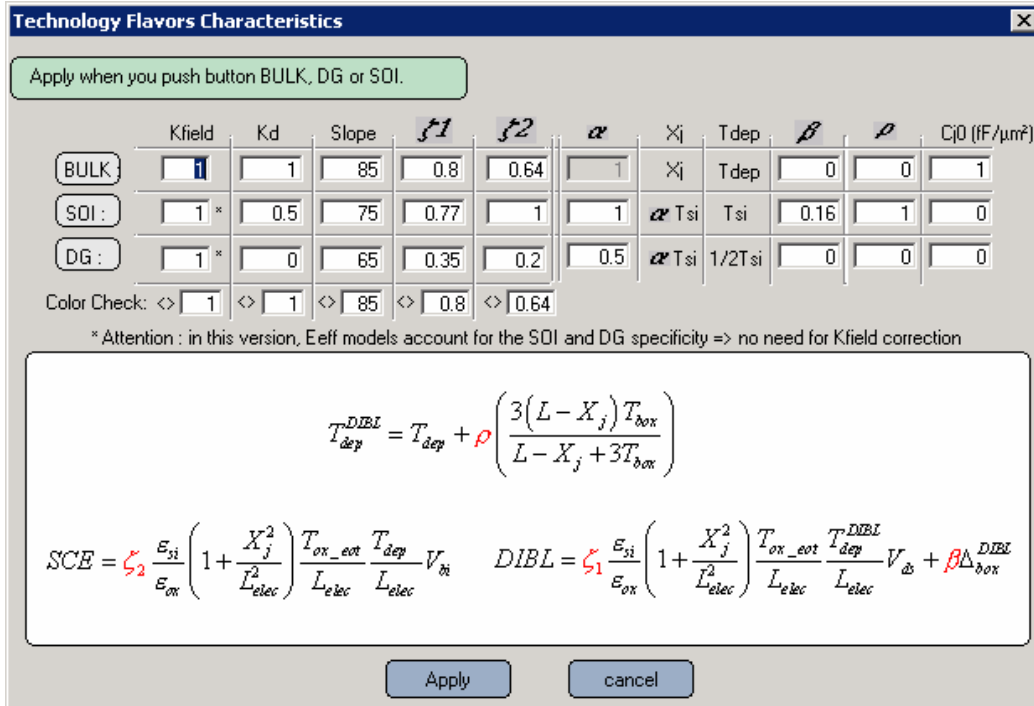


Figure 8. Content of the Technology Flavor Characteristics window.

Computational Modules

On the bottom of the dialogue window you have access to more computational parameters, which are grouped into **Fitting**, **Pocket**, **Mobility** and **Gate Stack** and **Dynamic** modules. Note that some of the default parameters are technology specific and are modified when switching from one technology choice to another.

Parameter	Description	Dim.	Default		
			Bulk	DG	SOI
<i>Gamma</i>	Scaling Factor for the Lateral Diffusion: $L_{elec} = L_{gate} - \text{gamma} * X_j$	none	0.8		
<i>Zeta1</i>	Scaling Factor for the DIBL (Drain Induced Barrier Lowering)	none	0.8		
<i>Zeta2</i>	Scaling Factor for the SCE (Short Channel Effect)	none	0.64		
<i>Slope</i>	if none of the calculation options is activated slope takes the entered value (for calculation details refer to Annex G)	mV/dec	-	65	75
<i>I_{th}</i>	I_d at the threshold voltage used to calculate S I_{thnew} activates the doping dependence of Ith calculation.	A	$5e-7$		
<i>delta</i>	Shift between V_{th} "on" and V_{th} "off" Is replaced by a QM estimation when "Vthon QM confin. hint" is activated	V	0.03		
<i>K_d</i>	Reduction factor of the d-coefficient Kd = 1: Bulk theoretical bulk value of d is used Kd = 0: body-effect for SOI and DG	none	1	0	0.5

Table 2: Description of the fitting parameters.

Fitting

Table 2 lists the parameters which can be found in the Fitting module. These parameters are used for the evaluation of the short channel effect, the DIBL, the subthreshold slope etc. The default values have been adjusted to fit the most recent planar CMOS technologies (CMOS 90 and 65 nm) and literature data (IEDM'03 and VLSI '04). Note that most parameters are technology dependent and change when switching from bulk to SOI. For the subthreshold slope, the user can choose between using the entered value and two different calculation methods (cf. Annex G). In the case of High-K oxides, the effective coefficients for the DIBL and SCE are enhanced by an additional factor, which takes into account the electrostatic coupling via a thicker oxide (cf. Annex F). The delta value has been added in order to take into account the difference between the effective threshold voltage for the calculation of the off and the on current. Indeed, the creation of the quantum well when going to strong inversion shifts the basic energy level of the carrier towards higher energies leading to an increase of the threshold voltage. This value can be added manually or calculated when checking the box "V_{th}on QM confin. Hint". For more details, please refer to the annex I.

Pocket

The Pocket module enables to take into account a non-uniform lateral doping distribution in the channel due to pocket implant. The module is activated by checking the corresponding box. This module can be used to fit properly experimental V_{th}(L_{gate}) curves. To do this the user must indicate the implanted ion species, the implantation angle and energy. Via a table based on SRIM-2003-calculations, the implantation depth and the (initial) ion distribution width are then entered into the calculation. Finally, the effective channel doping is obtained after definition of the activation factor α (from 0 no activation to 1 full activation) and the diffusion factor d , which ranges from 1 (no diffusion) to 30 (= 30 times initial distribution width). For more details, please refer to the annex C.

Parameter	Description	Dimension	Default
<i>Dose</i>	Pocket Implantation Dose	<i>atm/cm²</i>	<i>2e13</i>
<i>Angle</i>	Pocket Implantation Angle	<i>degrees</i>	<i>25</i>
<i>Species</i>	Implantation Species		<i>{B, BF2, In; As, P, Sb}</i>
<i>Energy</i>	Implantation Energy	<i>eV</i>	
<i>Activation</i>	Activation coefficient	<i>None</i>	<i>0 < a < 1</i>
<i>Diffusion</i>	Diffusion coefficient	<i>none</i>	<i>d ≥ 1</i>

Table 3: Parameters used in the Pocket Module, see Annex E for more details on the pocket-related parameters.

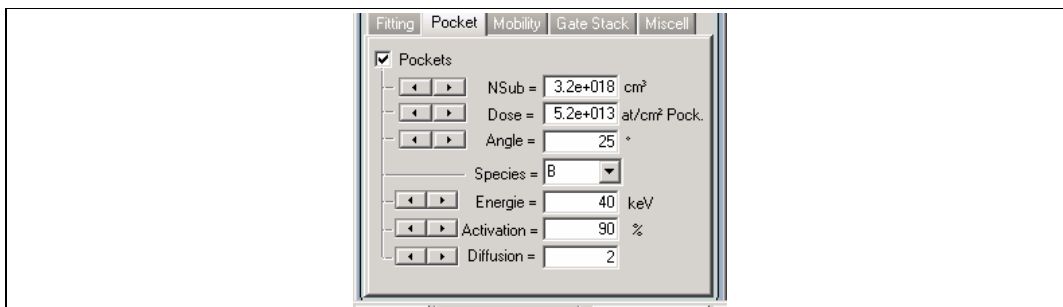


Figure 9: The pocket module.

Mobility

In the mobility module, a global I_{on} -enhancement factor $K_{on\mu}$ is calculated which takes into account the different factors that influence the mobility: substrates induced stress, process induced stress due to dielectric liners and possible mobility loss due to the use of High-K oxides. In the calculations, the mobility enhancement of the components gives an I_{on} -enhancement factor for the nominal gate length. Finally, the resulting factor K_{onMob} is the product of all these factors.

Input Parameters	Description	Dimension
K_{μ_sub}	Mobility enhancement through substrate strain	none
K_{str_pocket}	Stress enhancement on pocket region	none
$L_{st_pockets}$	Typical length of stress enhanced portions of the channel	nm
$K_{str_channel}$	Stress enhancement on channel region	none
$GradStress$	Degree of stress	none
K_{μ_HiK}	High-K Mobility Scaling Factor	none
Output Parameters		
K_{μ_HiK}	High-K Mobility Scaling Factor	none
K_{μ_othero}	Additional Mobility Scaling Factors	none
K_e	Total Mobility scaling factor due to dielectric stressors	none
$K_{on\mu}$	Total I_{on} -Scaling factor of a nominal device taking into account all mobility enhancements effects	none

Table 4: Description of the parameters used in the mobility computation.

The factor K_{field} acts on the value of the effective field, which can be reduced in thin film architectures. Note that in MASTAR 4, the default values for some of the parameters, e. g. K_{field} , change automatically with the choice of the CMOS technology Bulk, SOI or DG (for more details, please refer to the Technology Flavor paragraph and in the corresponding annexes).

Velocity

In the velocity module, we have regrouped three parameters which are the ballistic Ion-factor K_{bal} , the saturation velocity enhancement K_{vs} and the effective field reduction factor K_{field} . In this MASTAR pack, a ballistic transport module has been included. The user can enter the enhancement value himself and compare it then – by clicking on *Simplified Hint on Ballistic* – by the truly calculated enhancement factor : he can now decide to keep this new value or to return to the originally entered value by removing the cross. The functionalities of this calculation module are explained in the separate instructions for Quantum Ballistic Mاستار.

Input Parameters	Description	Dimension
K_{bal}	Ballistic I_{on} improvement	none
K_{vs}	Saturation velocity factor	none
K_{field}	Effective electric field reduction	none
Output Parameters		
K_{bal}	High-K Mobility Scaling Factor	none

Table 5: Description of the parameters used in the mobility computation.

The factor K_{field} acts on the value of the effective field, which can be reduced in thin film architectures. Note that in MASTAR 4, the default values for some of the parameters, e. g. K_{field} , change automatically with the choice of the CMOS technology Bulk, SOI or DG (for more details, please refer to the Technology Flavor paragraph and in the corresponding annexes).

Gate Stack

The Gate stack module enables to define all parameters which concern the transistor gate stack such as the width of the dark space, the poly-depletion and the gate leakage improvement factor for SiO₂-based gate oxides. Moreover, the user can switch to a High-K gate oxide stack with a bottom silicon oxide of thickness $Ped. SiO_2$ and a High-K layer of thickness $Hi_K T_{ox}$ and a dielectric constant $Diel. Const.$. Note that the fitting parameters ζ_1 and ζ_2 , which are used for the calculation of DIBL and SCE, are slightly increased when activating the High-K module. The use of High-K oxides has a direct impact on the gate leakage current and also on the effective mobility. These dependences can be defined in the High-K booster window by entering the gate Leakage Improvement Factors for low and high EOT and by entering the mobility reduction factor for thin and thick pedestal oxide. For more details, please refer to the Annex F. These latter functionalities can be switched on or off by marking a cross in the corresponding case. Another feature is the calculation for $EOT_{phys} = const.$. In this mode the physical thickness of the complementary layer is recalculated whenever $ped.SiO_2$ or T_{ox_High-K} is changed to keep the physical EOT-value constant.

Input Parameters	Description	Dimension
<i>Darkspace</i>	Extension of the Dark Space (in EOT). If QM Darkspace is activated the field shows the calculated value (Annex I), otherwise user can enter a chosen value	nm
<i>Poly-Depl.</i>	Extension of the poly-depletion (in EOT)	nm
N_{poly}	poly-Si doping level	cm ⁻³
<i>Phi_m</i>	Metal Gate Workfunction	eV
<i>IG TIF / SiO2</i>	Gate Leakage Improvement Factor wrt SiO ₂	none
<i>Ped. SiO2</i>	Interfacial oxide thickness (if Hi-K is activated)	Nm
<i>Hi_K T_{ox}</i>	Physical Thickness of the High-K oxide	none
<i>Diel. Const.</i>	Relative Dielectric Constant ϵ_r (if Hi-K is activated)	none
Output Parameters		
k_{HiK}	mobility degradation factor	none
<i>TIF HiK</i>	Effective Gate Leakage Improvement Factor for High-K wrt SiO ₂	none
<i>IG TIF / SiO2</i>	Gate Leakage Improvement Factor wrt SiO ₂ (= <i>TIF HiK</i> if activated)	none
<i>EOT_Phys</i>	Physical Equivalent oxide Thickness	nm

Table 6: Input and Output Parameters of the Gate Stack module.

Dynamic

In this computational module, the user can adjust several parameters, which are used for the calculation of the dynamical characteristics of the transistor, such as switching delay etc. Among these parameters we find the metal 1 pitch, the gate resistance, the total fringing and overlap capacitance.

Parameter	Description	Dimension
<i>Total Fring Cap.</i>	Total Fringing Capacitance	F/μm
<i>C_{overlap}</i>	Gate – LDD Overlap Capacitance	% C _{g-ideal}
<i>M1 pitch</i>	Periodicity of the Metal 1 wires	nm
<i>R_g</i>	Gate Resistance	Ω
<i>K_{load}</i>	Fitting parameter for the inverter delay	none

Table 7: The parameters of the Dynamic module.

The Booster Template

The buttons in this field allow the user to switch one or several performance boosters, which are Strained Silicon, Metal Gate, Ballistic Transport, High-K oxide and Reduced Fringing Capacitance. Once the performance booster is activated, a set of predefined parameters – accessible by clicking on the adjacent triangle - is loaded. In order to trace the changes, the parameter modifications with respect to the situation without boosters are highlighted in the main window. By default, MASTAR suggests the following set of parameters when activating the Booster Buttons (cf. Table 8).

Booster Button	Physical Parameter	Deactivated	Activated
Metal Gate	Poly-depletion	4 Å	0
Strained Silicon	<i>K_{mu}</i> (μ enhancement)	1	2
Ballistic	<i>K_{vsat}</i> (sat. velocity enhancement)	1	1.3
High-K	<i>TIF_{Hi-K}</i> (gate leakage improvement) <i>K_{HiK}</i> (mobility degradation)	Not active 1	User defined User defined
Fringe	Total fringing Capacitance	2.4e-16 F/μm	1.3e-16 F/μm

Table 8 : Action and default values of the booster buttons.

The assumptions for the gate leakage improvement and the mobility degradation in the case of High-K oxides is described in detail in Annex F.

CAUTION : the values of Kfield, Kd, Poly_dep, Kmu, Kvs and Fring used in the ITRS 2003 profiles take often some intermediate values between the standard and boosted ones. This results from how they were defined in the PIDS Excel spread-sheet – we have used the same values for having a full compatibility between the two tools. The consequence of that is, however, that once having loaded for example the HP45nm node (that is defined as Bulk) and pushing the Bulk button you will not obtain the same results. **We advise you therefore to save an unaltered copy of the package as-sent before all manipulation, so as to be able to retrieve the original profiles in case of un-cautious over-writing.**

Modification of the Booster Default Values

The default values for the default boosting parameters can be visualized and modified after clicking on the adjacent triangular button (cf. Figure 10). For the Gate leakage improvement factor and mobility.

Calculation @ constant Ioff

A special feature is the **button *Ioff_c***, which is located in the upper part of the main dialogue window. When this button is activated, the Nbulk value will appear grey. Indeed, the bulk doping (and thus the threshold voltage) will be automatically adjusted to a level, which keeps the Ioff-value constant despite changes on technological parameters such as *Tox*, *Lgate*, etc. This feature is very useful for the evaluation of technological options as you can get rid of threshold variation effects.

Calculation @ constant Lelec

A new feature is the **button *Lelec const.***, which is located right below the X_{jext} value in the main dialogue window. When this button is activated, the L_{gate} value will appear grey. When changing the extension depth the gate length will be automatically adjusted in order to keep the electrical gate length constant.

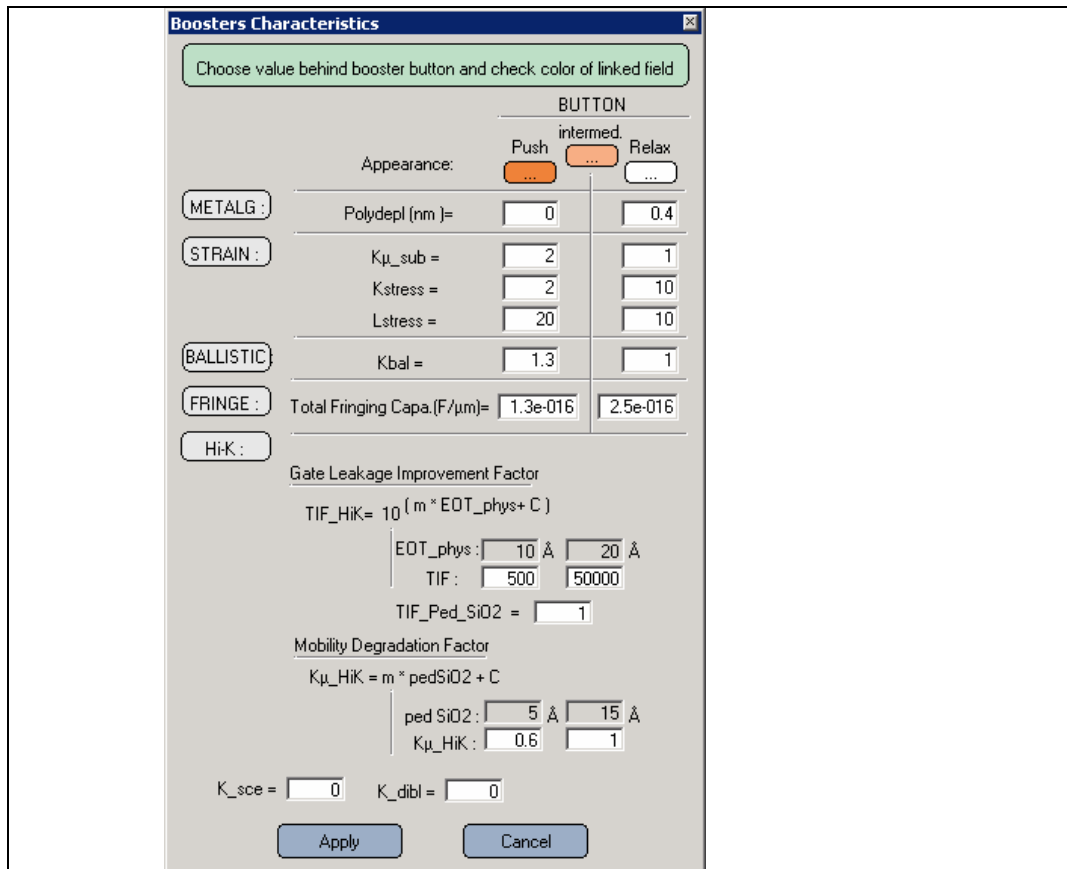


Figure 10: Display window of the default values of the MASTAR boosters.

Saving Profiles

A *profile* is defined as a *complete set of input parameters*. It is saved as a hidden file with the extension *.pro* and is only accessible via the MASTAR interface. Profiles can be created by the buttons “Save” and “Save as” in the main dialogue window.

The Menu Bar

In the menu bar several submenus are accessible: the *File* menu gives access to the Log File displaying all calculated parameters. The *View Graphics* menu enables to modify the data selection and their presentation in the main graphics. Finally, the *Compute* menu allows the user to update the graphics. For maximum user friendliness most options can be equally accessed placing the cursor on the object you want to modify and clicking on the right mouse button.

The main output windows: numerical values and the Ion-Ioff graphics

The calculations are executed via the *Compute* button from the main dialogue window. The principal electrical characteristics will be displayed numerically in the output window named *MASTAR 3 Results*.

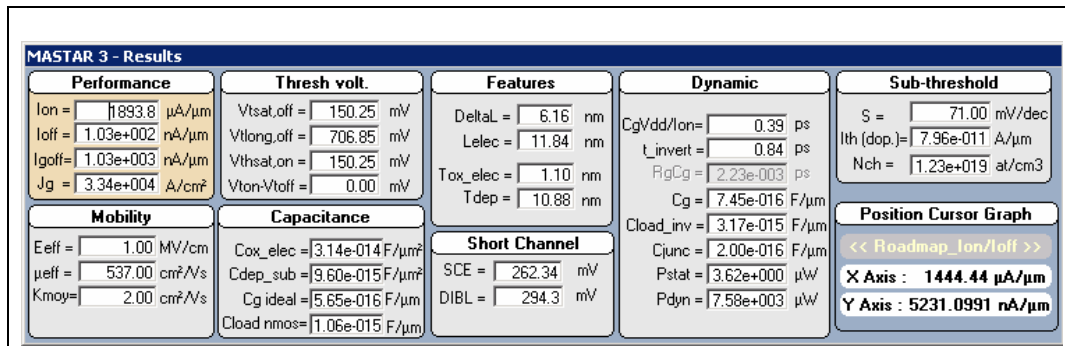


Figure 11: The output window MASTAR 3 Results.

Output Parameter	Description	Dimension
Performance		
I_{on}	Drain Current for $V_{gate} = V_{drain} = V_{dd}$	$\mu A/\mu m$
I_{off}	Channel Leakage Current for $V_{gate} = 0$ and $V_{drain} = V_{dd}$ (= $I_{s,off}$)	$nA/\mu m$
I_{gon}	Gate Leakage Current “On” $I_g = J_g * L_g$	$nA/\mu m$
I_{goff}	Gate Leakage Current “Off” $I_g = J_g * \Delta L/2$	$nA/\mu m$
J_g	Gate Leakage Current Density ($V_{gate} = V_{dd}$)	A/cm^2
Thresh. Volt.		
$V_{tsat,off}$	Saturated Threshold Voltage ($V_{gate} = V_{drain} = V_{dd}$) used for the extrapolation of I_{off}	mV
$V_{tLong,off}$	Saturated Threshold Voltage for infinite gate length	mV
$V_{tsat,on}$	Saturated Threshold Voltage used for the I_{on} calculation ($V_{tsat,on} > V_{tsat,off}$)	mV
$V_{ton} - V_{toff}$ (used)	Used Shift between the two Threshold Definitions	mV
Features		
ΔL	$\Delta L/2 =$ Lateral LDD Diffusion	nm

L_{elec}	Electrical gate length: $L_{elec} = L_{gate} - \Delta L$	nm
T_{ox_elec}	CET	nm
T_{dep}	Depletion depth	nm
Dynamic		
$C_g V_{dd}/I_{on}$	Gate Delay	ps
t_{invert}	Inverter Delay	ps
$R_g C_g$	RC-term	ps
C_g	Gate capacitance	F
C_{load_inv}	Load Capacity of the inverter	F
C_{junc}	Junction capacitance	F
P_{stat}	Static dissipated power	μW
P_{dyn}	Dynamic dissipated power	μW
Mobility		
E_{eff}	Effective Field used for the Mobility Calculation	MV/cm
μ_{eff}	Effective Mobility	cm^2/Vs
K_{mov}	effective inversion layer μ enhancement	cm^2/Vs
Capacitance		
C_{ox_elec}	Gate Oxide Capacity in Inversion	$F/\mu m^2$
C_{dep_sub}	Depletion Capacity in the Substrate	$F/\mu m^2$
C_{gideal}	Ideal Gate Capacitance	$F/\mu m$
C_{load_nmos}	Loading capacity of the nmos device	F
Short Channel		
SCE	Short Channel Effect	mV
$DIBL$	Drain Induced Barrier Lowering	mV
Subthreshold		
S	Sub-threshold Slope	mV/dec
I_{th_new}	Current at threshold	$A/\mu m$
N_{ch}	Average Channel Doping (w/ Pockets)	atm/cm^3

Table 9: Description of the parameters of the output window.

The central output window is the Ioff/Ion chart (cf. Figure 12). The current performance data point is shown as a red point in this window. In addition, predefined *plot files* - lists of Ion-Ioff values – can be displayed. Note that in this chart, the Ioff value is given by the channel leakage, i. e. the source current for $V_g = 0$. The off state gate leakage current is plotted as a horizontal dashed line for comparison.

Master for advanced users: description of the menus

The File Menu

The file menu contains only “Open Log File”; this command opens a text file listing all intermediate calculation results. Note that many of the former sub-menus are now directly accessible from the graphics by a right mouse button click.

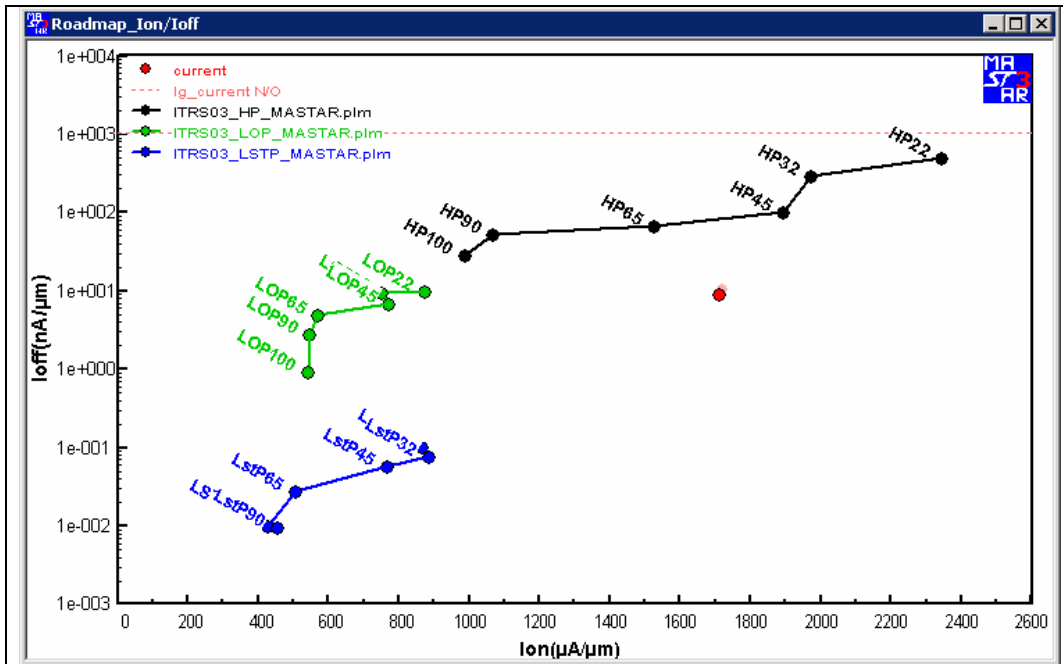


Figure 12: The principal graphical output window, the Ion-Ioff Graph displaying the “current data point” and some user selected data.

The View Graphics Menu

This menu allows the user to select the graphics which appear in the MASTAR frame. The following graphics can be visualized: Roadmap Ion-Ioff, graphics cloud Ion-Ioff, Ion-CV/I and DIBL-L and the auxiliary graphics $V_{th}(L)$, Ion-Ioff(L), Ion(L), Ion(Tox), $\mu_{eff}(E_{eff})$, CV/I(L), S(L) and Ion Improvement (L). For any modification on the graphics please refer to the “Modification of the graphics” chapter.

Ion-Ioff Cloud:

The Ion-Ioff Cloud graphics is a useful tool in order to explore the performance limits for a given transistor generation (cf. Figure 13). Clouds of performance data points can be generated and displayed on an Ion-Ioff graphics by simply imposing intervals and incremental steps for the main technological input parameters, such as gate

length, oxide thickness, supply voltage etc. within a given technology. Note that for the I_{off} , the user can choose between a calculation of the channel leakage current, i. e. the source current, and the complete off current including thus gate and junction leakage.

On this graphics, you have the possibility to display in addition to the generated data user defined I_{on} - I_{off} data, e.g. recent literature performance data, for comparison reasons. The corresponding files are stored with the extension .per. For more details, please refer to the “Modifications on the I_{on} - I_{off} graphics” section.

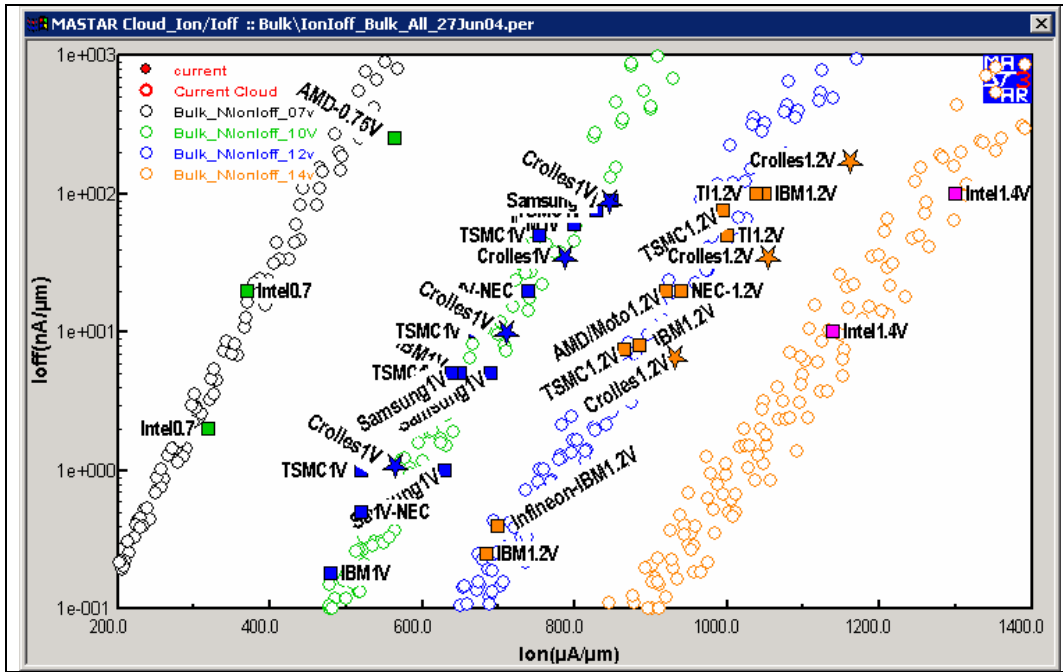


Figure 13: The “cloud” graphics: this presentation allows the user to explore the performance domain spun up by user-defined intervals of the main technological parameters such as gate length, oxide thickness, junction depth etc and compare it with recent literature data.

Generic Auxiliary

In this graphics, the evolution of a variety of output and intermediate transistor parameters can be calculated over an interval of the ITRS parameters L_{gate} , T_{ox} , N_b , x_j (T_{si}) or V_{dd} . The graphical presentation can be made either versus the ITRS parameters or versus a second calculated parameter. The accessible parameters are listed in Table 10. Optionally, the off-current ($I_{s, off}$) can be set constant for better comparison.

X&Y-axis parameters	Description	Dimension
I_{on}	Drain Current for $V_{gate} = V_{drain} = V_{dd}$	$\mu A/\mu m$
J_g	Gate Leakage Current Density ($V_{gate} = V_{dd}$)	A/cm^2
$K_{on\mu}$	Total I_{on} -Scaling factor of a nominal device taking into account all mobility enhancements effects	$K_{on\mu}$
L_{elec}	Electrical gate length: $L_{elec} = L_{gate} - \Delta L$	nm
J_g	Gate Leakage Current Density ($V_{gate} = V_{dd}$)	A/cm^2
P_{dyn}	Dynamic dissipated power	μW
P_{stat}	Static dissipated power	μW

SCE	Short Channel Effect	mV
S	Sub-threshold Slope	mV/dec
t_{invert}	Inverter Delay	ps
T_{dep}	Depletion depth	nm
$V_{tLong,off}$	Saturated Threshold Voltage for infinite gate length	mV
$V_{tsat,off}$	Saturated Threshold Voltage ($V_{gate} = V_{drain} = V_{dd}$) used for the extrapolation of I_{off}	mV
$V_{tsat,on}$	Saturated Threshold Voltage used for the I_{on} calculation ($V_{tsat,on} > V_{tsat,off}$)	mV

Table 10: List of the possible output parameters in the Generic Auxiliary Graphics.

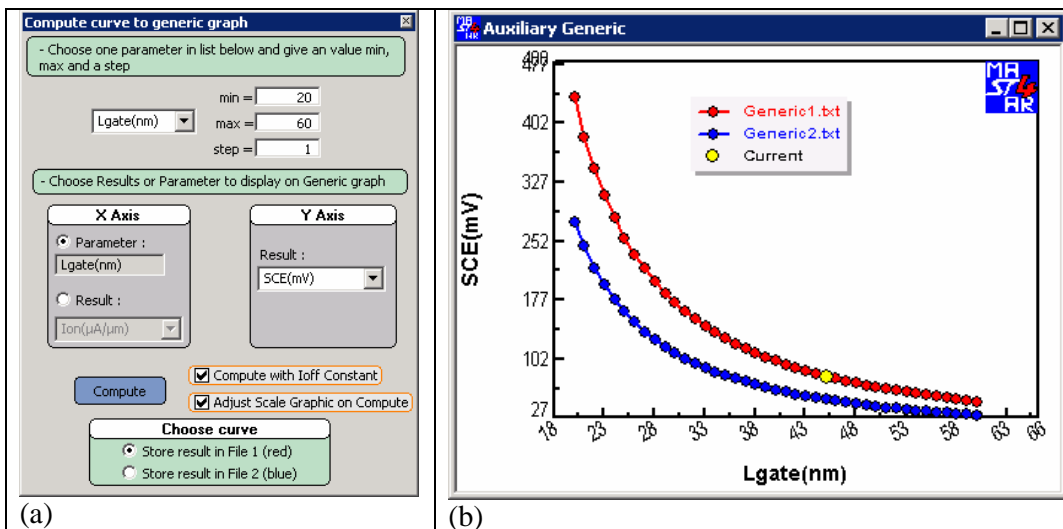


Figure 14: The compute window for the generic auxiliary graphics and one example of application showing a SCE versus L_{gate} plot for two different technologies.

Vth(L): threshold over gate length

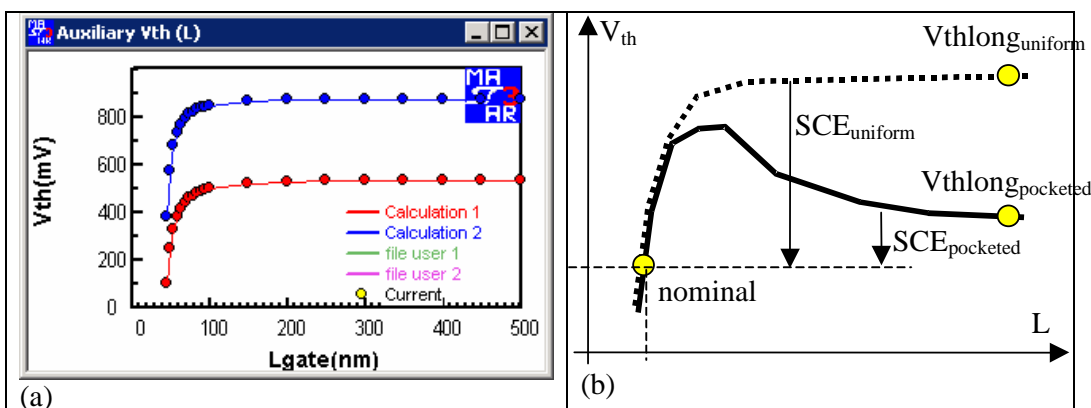


Figure 15: The $V_{th}(L)$ graphics: an example of the MASTAR V_{th} - L plot with and without activating the pocket module.

The $V_{th}(L)$ graphics shows the dependence of the threshold at $V_{drain} = V_{dd}$ on the physical gate length L_{gate} . Two curves are presented in this graphics, which can be calculated independently allowing the user to compare the impact of the different

technological input parameters. By default, the saturated threshold voltage $V_{tsat,off}$ is calculated. In order to obtain the linear threshold voltage, please choose $V_{dd} = 0.1$ V in the main dialogue window.

Pocket effects on the threshold curve can be reproduced when activating the pocket window. In this case, the channel doping N_{ch} refers to the doping of a long channel device.

I(L): I_{on} over gate length @ $I_{off} = \text{const}$

The I(L) graphics shows the dependence of the on-current I_{on} on the gate length L_{gate} . For better comparison, I_{off} is kept constant during the calculations via a simple threshold voltage adjustment by channel doping correction.

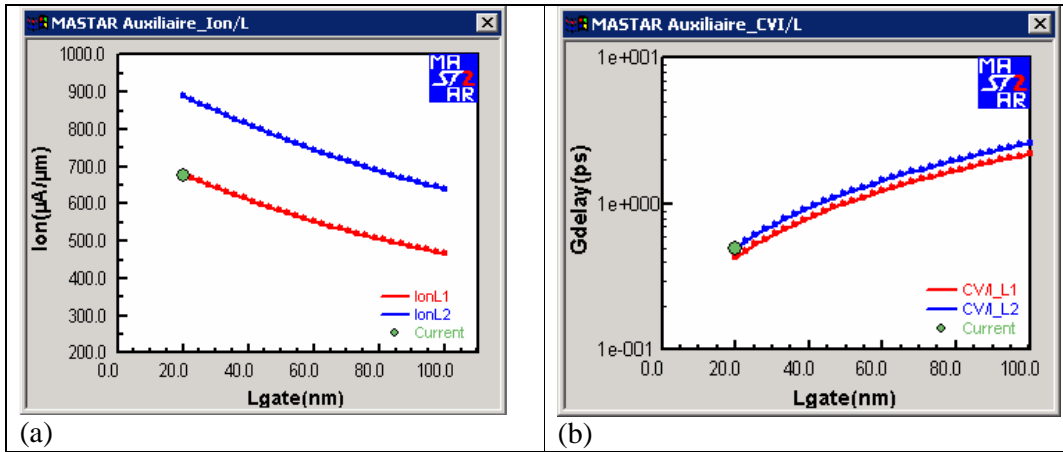


Figure 16: The Ion(L) graphics (a) and the CVI_L graphics (b).

CV/I(L): gate delay over gate length @ $I_{off} = \text{const}$

The CV/I(L) graphics indicates the gate delay, calculated by $\tau = CV/I_{on}(L_{gate})$. Also for this presentation, I_{off} is automatically kept constant during the calculation to enable a better comparison.

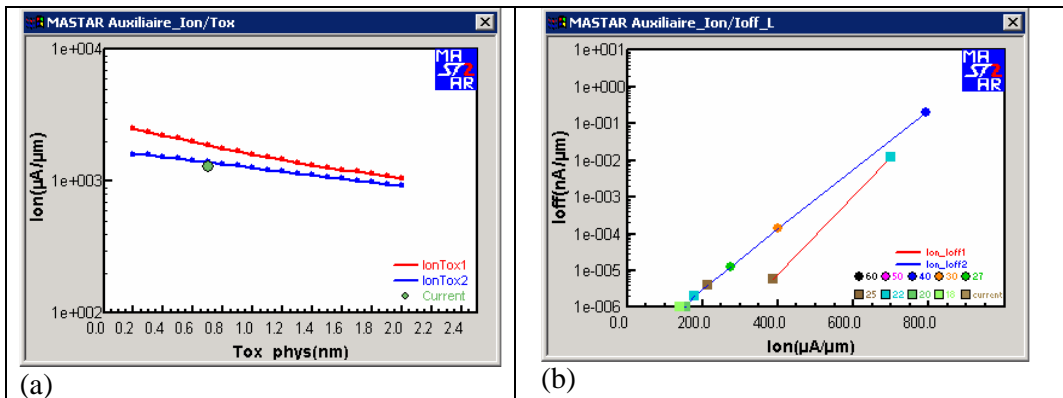


Figure 17: The Ion(Tox) graphics (a) and the Ion-Ioff(L) graphics (b).

Ion(Tox): I_{on} over gate oxide thickness @ $I_{off} = \text{const}$

The Ion(Tox) graphics shows the evolution of the on-current I_{on} (at $I_{off} = \text{constant}$) over the gate oxide thickness. Two curves are presented in this graphics, which can be calculated independently.

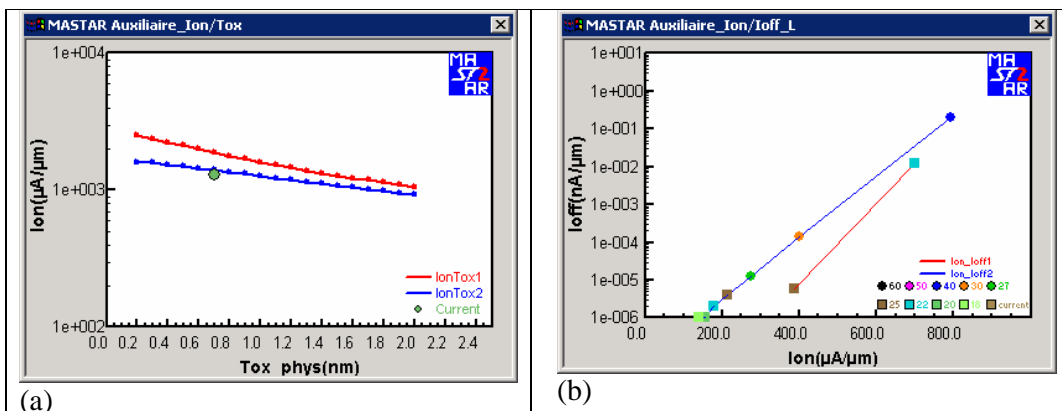


Figure 18: The Ion(Tox) graphics (a) and the Ion-Ioff(L) graphics (b).

Ion-Ioff(L): performance over gate length

The Ion-Ioff(L) graphics presents the performance data points calculated for a set of physical gate lengths: $L_{gate} = 9, 13, 18, 25, 35, 45, 65\text{nm}$.

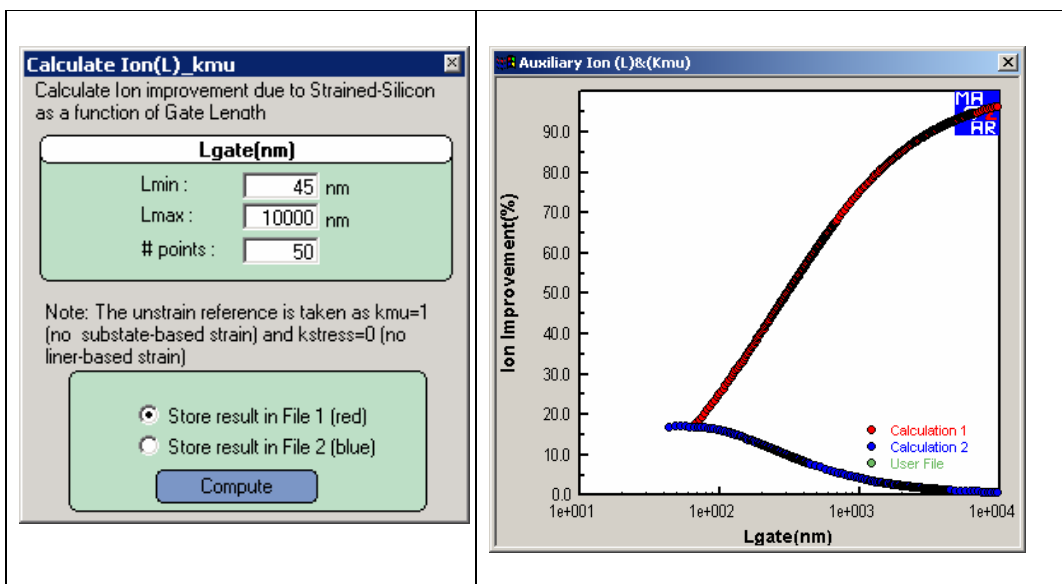


Figure 19: The Ion improvement as a function of the gate length, for global and local stress.

Ion Improvement (L):

By this type of graphics the effect of mobility enhancement on Ion(L) can be analyzed. For this purpose, the improvement of Ion in % is plotted as a function of the gate length in the presence of long channel mobility enhancement ($k_{mu} > 1$) or stress induced by liners (see annex J) (cf. Figure 19). Both models were fitted on experimental data Note that if you choose to cumulate both substrate based strain and liner-based strain, the reference for calculation is still totally unstrained (i.e. NO substrate effect and NO liner effect).

Modification on the graphics

Modifications on the Ion-Ioff graphics

If the cursor is placed on the Ion-Ioff graphics, a click on the right mouse button opens a submenu containing the following options: "Modify Scale", "Copy to Clipboard", "Cursor Position", "Load / Delete Profile", "Load / Unload Plot", "Create / Modify Plot File", "Delete Plot", "Ghost" and "Enable Info Popup".

Modify Scale: By default an autoscaling function guarantees that the current performance data points are centrally positioned in the Ion-Ioff graphics window. Disabling this feature, the x-and y axes can be scaled manually. Moreover, it is possible to switch from linear to logarithmic presentation.

Copy to Clipboard:

This command loads the current graphics into the clipboard. It can be pasted in any document using the Ctrl + V function.

Load / Delete Profile: opens a dialogue window to load or delete profiles. A *profile* is defined as a complete *set of input parameters* as listed in Table 1. It is saved as a hidden file with the extension *.pro* and is only accessible via the MASTAR interface. After opening the dialogue window you can choose one of the available profile files. Its content will then be visualized in the lower part of the window (cf. Figure 20). Clicking on *Load* will transfer the parameters into the main dialogue window. The numerical and graphical results will be updated automatically. You can delete a profile by clicking on it and then using the right mouse button: you can now choose the *Delete* option.

Load / Unload Plot: This submenu enables to *add or remove Plot files* from the Roadmap Ion-Ioff graphics. Plot files with the extension *.plt* contain a series of *performance data points*, those with the extension *.plm* are *linked to a list of profiles files*. Both types are used for display on the Ion-Ioff graphics and enable performance comparisons with the current data point. For creation, please refer to the explanations of the *Create/Modify Plot* command. If the plot file already exists just click on *Load / Unload Plot*: the *Display Plot File* Dialogue Window is then activated. To add or remove plot files, click on the corresponding *plot file* in the list on the left / right side, then click on *Add* or *Remove*.

Create / Modify Plot: Command enabling the creation and modification of Plot Files. Within MASTAR a *plot file* is defined as an output file containing or linked to a *list of Ion-Ioff values*. *Plot files are usually created from* using a set of previously defined *profile* files; in this case they have the extension *.plm*. Note that the change of an underlying profile changes immediately the plot file. If you choose the *Create / Modify Plot File* command, the corresponding dialogue window is opened. On the left side the existing plot files are listed. When clicking on one of them, the underlying profiles are displayed in the right window. By means of the *Add* and *Remove* buttons profiles can be added or removed from the plot file.

Alternatively, the user can create plot files by editing a text file containing a list of Ion [$\mu\text{A}/\mu\text{m}$] and Ioff [$\text{nA}/\mu\text{m}$] values using the following sequence:

[name1]
 Ion=900
 Ioff=10.0
 [name2]...

This text file must be saved with the extension *.plt* and be available in the sub-folder *Plot*.

Delete Plot: Opens a window which enables to delete an existing plot file.

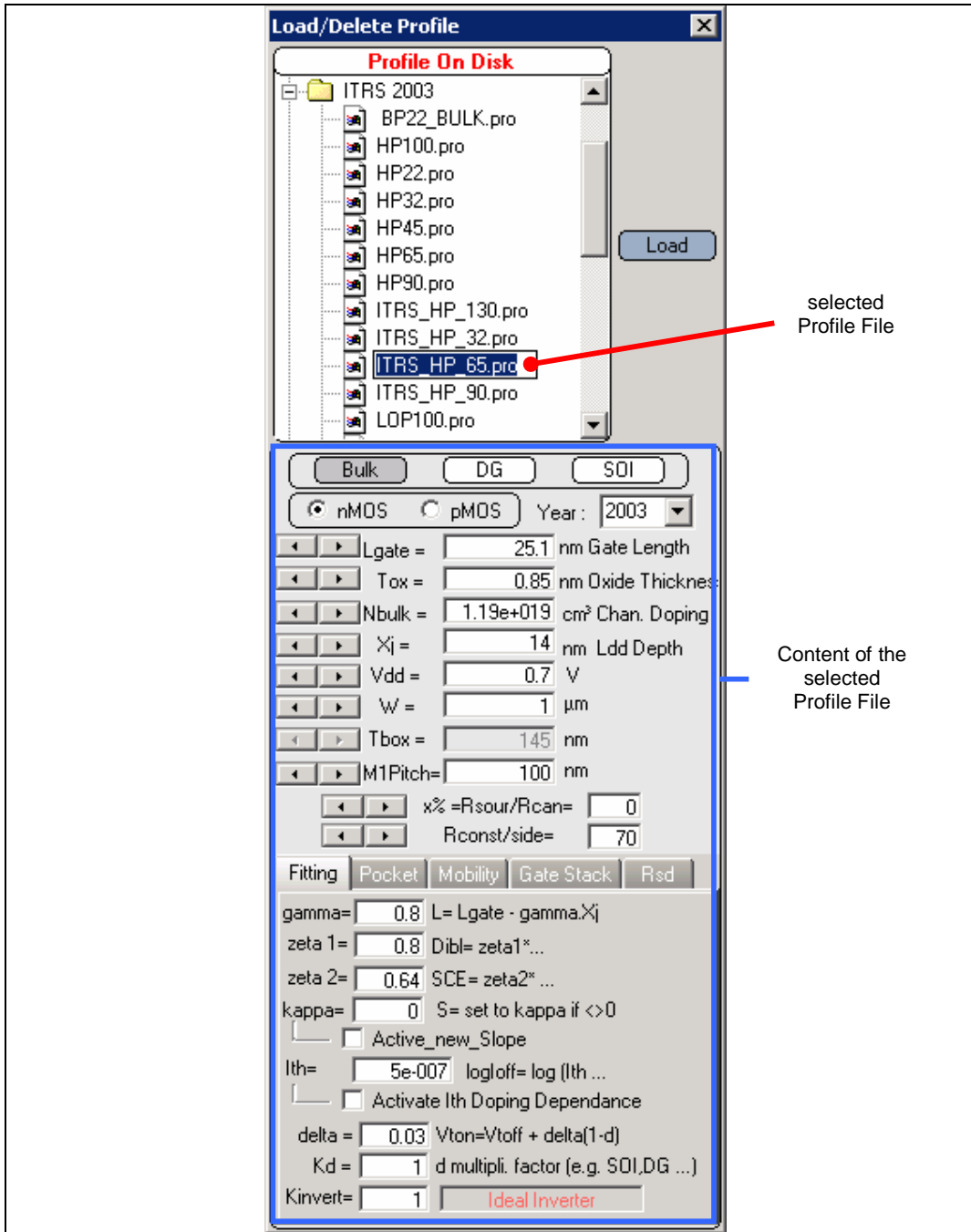


Figure 20: The Load Profile dialog window from the File menu.

Enable Info Pop-up: A pop-up window displaying the values is shown when you point on a data point of the graph. It contains a short-cut to the *Load Profile* command: clicking on the triangular symbol on the upper left part of the pop-up window injects the corresponding profile directly into the input parameter window.

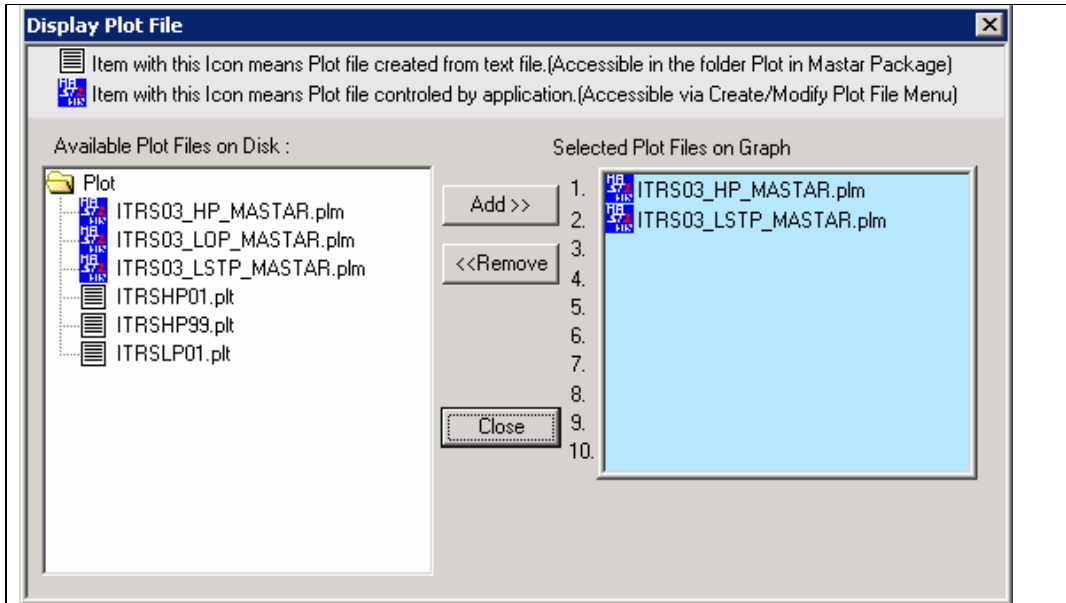


Figure 21: The Display Plot File Dialogue Window.

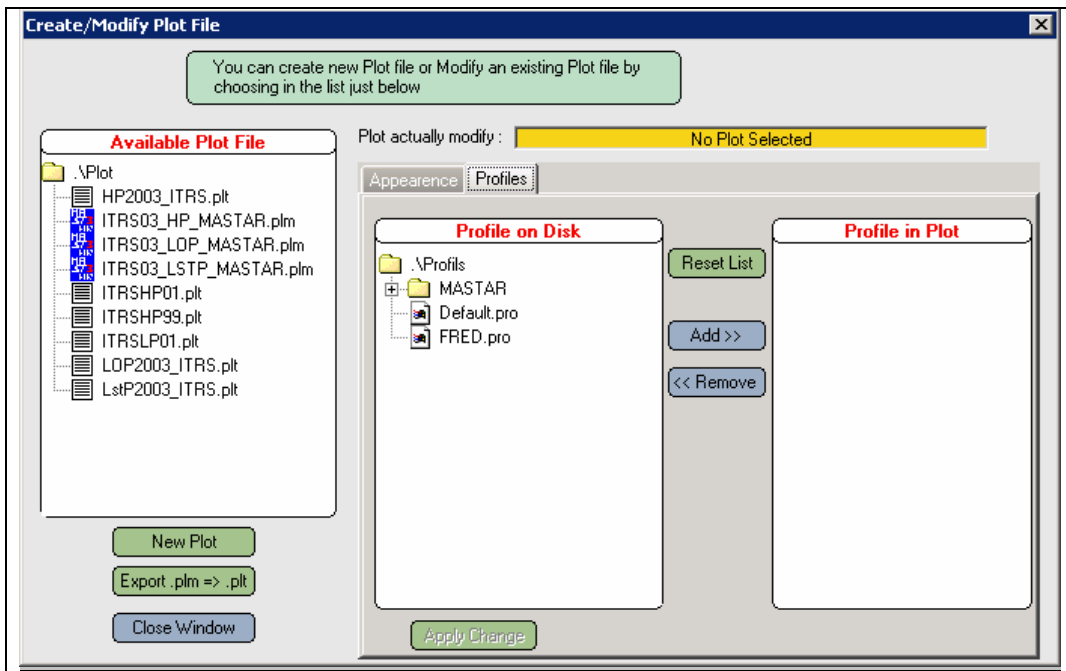


Figure 22: Dialogue window for the creation of a plot file.

Modifications on the Cloud graphics

Once the cursor placed on the graphics a click on the right mouse button opens the submenu with the following options: “Modify Scale”, “Copy to Clipboard”, “Cursor Position”, “Load / Delete Profile”, “New Cloud”, “Load / Unload Cloud”, “Purge Cloud”, “Change .per file”, “Edit / Modify .per File” and “Enable Info Popup”. Some of the functions being equal to those commented for the Ion-Ioff graphics, we just comment on the new options:

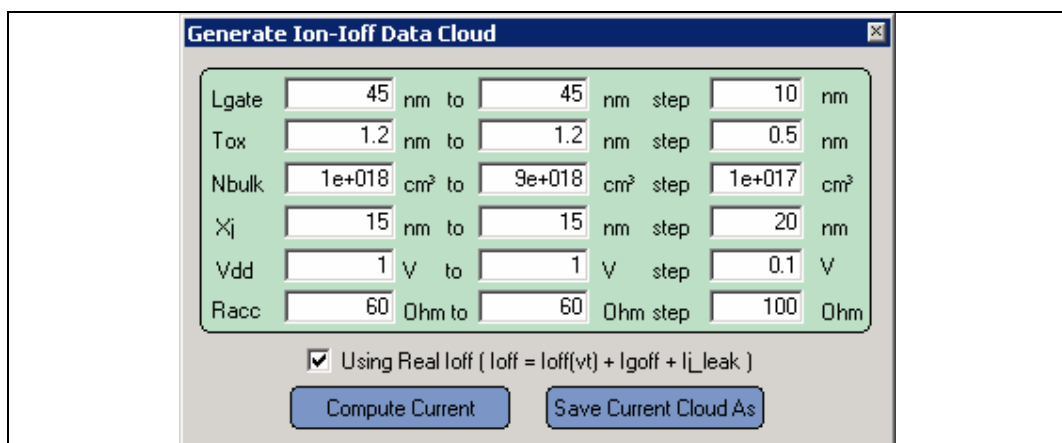


Figure 23: The Ion-Ioff Data Cloud parameter window.

New Cloud: opens the Generate Ion-Ioff Data Cloud window (cf. Figure 23) which contains the lower and upper limit and the incremental step of the main technological parameters on which the calculation of the data cloud will be based upon. In addition, the user can choose between the channel leakage current, i. e. the source leakage current, or an estimation of the complete off current, i. e. including the gate leakage and the junction leakage, for presentation of I_{off} on the y-axis. The generated data can be stored by clicking on the “Save Current Cloud As” button. This will save the cloud data and also generate a corresponding profile which can be reloaded for later use.

Load / Unload Cloud: opens a window in which the user may select the data clouds to be shown in the graphics window.

Purge Current Cloud: This command will erase the last generated cloud from the graphics.

Change .per file: Command which enables to change the user defined literature data that is displayed on the graphics. MASTAR offers the possibility to create files with the extension .per containing lists of data points defined by a label name, the values of Ion, Ioff, CV/I, DIBL and additional information for the graphical presentation (label orientation, symbol, color, etc.). These files are organized as work sheets with one line per data point as shown in Figure 24. Note that when changing the .per file MASTAR automatically loads all clouds that were displayed at the last utilization of the .per file (cf. Figure 26); they are memorized in the header of the .per file.

Literature Editor

File LPP actually open: Bulk\Nonloff Bulk: All 27Jun04.p

Open Save Save as ... Insert row Delete row

	Ion(μA/μm)	Ioff(nA/μm)	Name	Orien...	CV I(ps)	Orien...	Lgate(...)	DIBL(...)	Orien...	Shape	Color	Comments
0	690	5	Samsung1V	SW			80	50	SE	Square	Blue	
1	630	1	Samsung1V	SW			15	100	SW	Square	Blue	
2	370	2.00E+01	Intel0.7							Square	Magenta	
3							50	100	SE	Diamond	Magenta	
4	320	2.00E+00	Intel0.7	W						Square	Magenta	
5	564	254	AMD-0.75V	NW						Square	Magenta	
6	480	1.80E-01	IBM1V							Square	Blue	
7	650	5.00E+00	IBM1V	NW						Square	Blue	
8	800	6.00E+01	IBM1V	W						Square	Blue	
9	740	20	1V-NEC	W						Square	Blue	
10	520	0.5	1V-NEC							Square	Blue	

Figure 24: The presentation of the .per file.

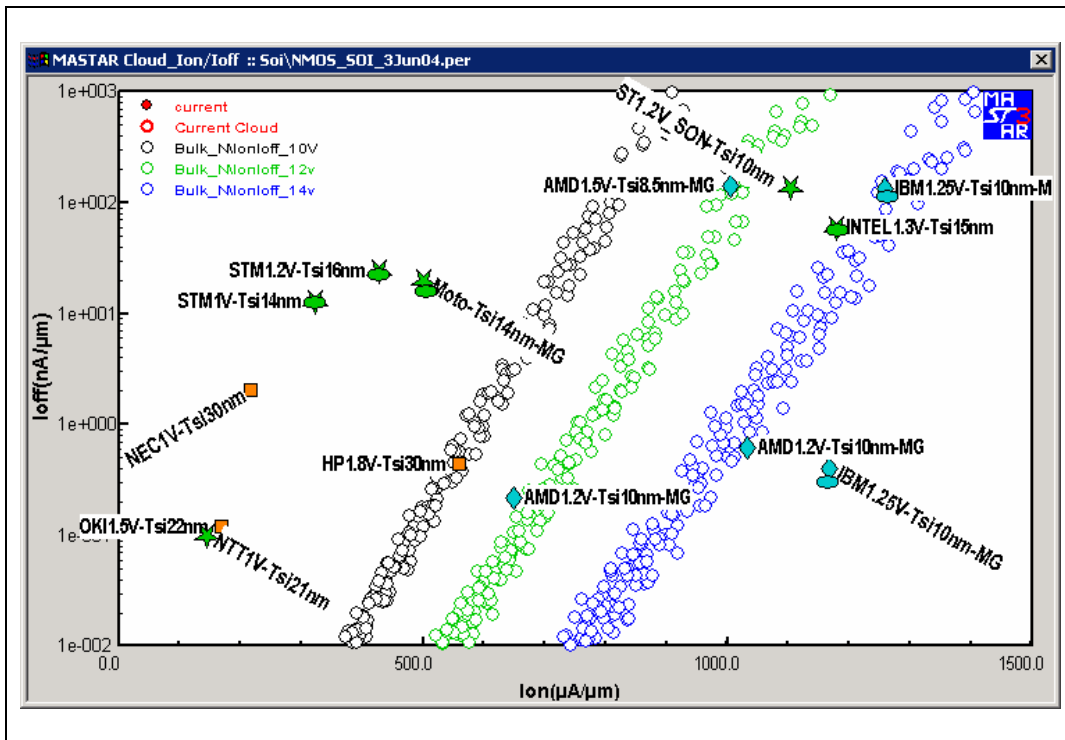


Figure 25: FDSOI NMOS .per file and its associated clouds.

Edit / Modify .per File: Command which opens the currently shown .per file. In the work sheet one line corresponds to one data point. Note that the box left to the data must be checked if you want to visualize the data point on the graphics. All cells can easily be edited by selecting them with the cursor and typing in the desired information. Note that this table can be directly copied from or pasted to Microsoft EXCEL. If you place the cursor on a data point of the .per file on the graph, a pop-up window opens indicating the numerical Ion-Ioff data. Clicking on the triangular symbol on the upper left part opens the active .per file and highlights the corresponding data point line.

Useful Shortcuts:

Quick access to the cloud calculation conditions is given when placing the cursor on the corresponding symbol appearing in the legend. A pop-up window appears displaying the calculation parameters. On its upper part, you can see the corresponding cloud and profile file names. A triangular symbol is situated in the upper left corner of the appearing window (cf. Figure 26). By simply clicking on it you can inject these parameters directly into the Generate Ion-Ioff Cloud window. Moreover you will be asked if you want to load the corresponding profile in the main dialogue window.

A right mouse button click on a user defined data point will open the current .per file and high-light the corresponding line for quick editing.

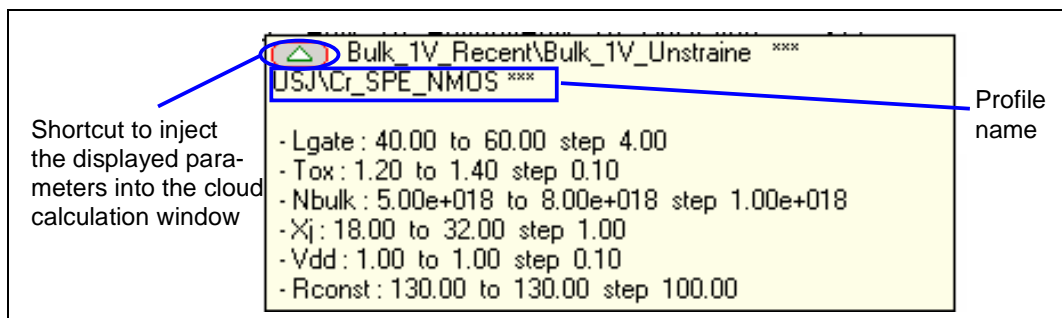


Figure 26: Data cloud Pop-Up-Window.

Auxiliary graphics

On the auxiliary graphics, the following options are accessible by a right mouse button click: “Modify Scale”, “Copy to Clipboard”, “Cursor Position”, “Curve X_(Y)”, “Open File Results1” and “Open File Results2”.

Curve X_(Y): opens the window for new calculation of the current graphics. On can enter the calculation limits and select one curve for a new calculation.

Open File Results1: opens a text file containing the data of the corresponding graphics.

User files

All auxiliary graphics have a link to two so-called *user files* which can be helpful to display (experimental) data for comparison reasons. To open the file editor, please place the cursor on the symbol *user file i* on the lower right corner of the auxiliary graphics and click on the right mouse button. The corresponding file opens and can be edited.

The Compute Menu

This menu contains all computational commands concerning the auxiliary graphics and the cloud graphics:

Clouds	calculation of a performance data cloud
Vth(L) & S(L)	threshold / subthreshold slope over gate length
CV/I(L) and Ion(L)	gate delay over gate length and on current for $I_{off} = \text{const.}$
Ion(Tox)	I_{on} current over oxide thickness for $I_{off} = \text{const.}$
Ion-Ioff(L)	Performance over gate length
DIBL(Tbox)	SOI specific: DIBL versus Tbox thickness
Ion Strain Improvement	Ion improvement by long channel mobility enhancement through strain effects

All...

Clicking on *All...* will open the *Compute All* window. This window allows the user to update the presented data points in all auxiliary graphics windows. The newly computed data will be applied on the selected (red or blue) curve.

Vth(L) and S(L)

Via this dialogue window it is possible to update the displayed data points in the graphics *Vth(L)* and *S(L)* while all other auxiliary graphs remain unchanged. Again, the user can decide whether the new generated data should be applied for the red (*Vth_1*) or the blue curve (*Vth_2*). Moreover, the user can define the interval used for calculation and display (cf. Figure 27).

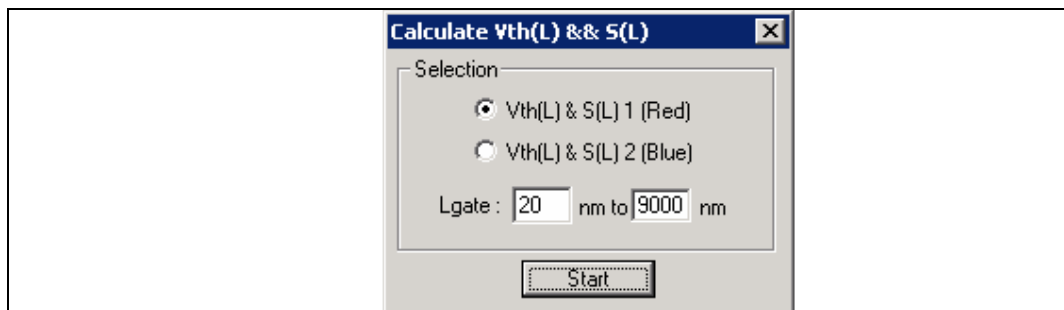


Figure 27: The *Vth(L)* calculation window.

CV/Ion(L) and I(L)

The submenu *CV/Ion(L)* and *I(L)* from the *Compute Menu* will open the corresponding dialogue window. The user can now select which curve he wishes to be updated and define the corresponding computational window. The *CV/Ion(L)* and *I(L)* graphics are simultaneously updated when clicking on the *Start* button. Note that I_{off} is kept constant during the calculation of the I_{on} values.

Ion(Tox)

This submenu allows the user to update the *Ion(Tox)* graphics. Choose the curve by clicking on the corresponding button and update by clicking on *Start*. Note that I_{off} is kept constant during the calculation of the I_{on} values.

Ion-Ioff(L)

In the dialogue window, select one curve and click on *Start* to update the graphics. The performance data is calculated on a fixed series of gate lengths ($L_{\text{gate}} = 25, 30, 40, 50, 60, 70, 80, 90$ et 100 nm).

Ion-Ioff Data Cloud

The *Ion-Ioff Cloud* submenu opens the dialogue window called "*Generate Data Ion-Ioff Cloud*". You can enter the lower and upper limit and the incremental step of the main parameters and start the calculations.

The workspaces “Roadmap”

The workspaces “Roadmap” – a global view

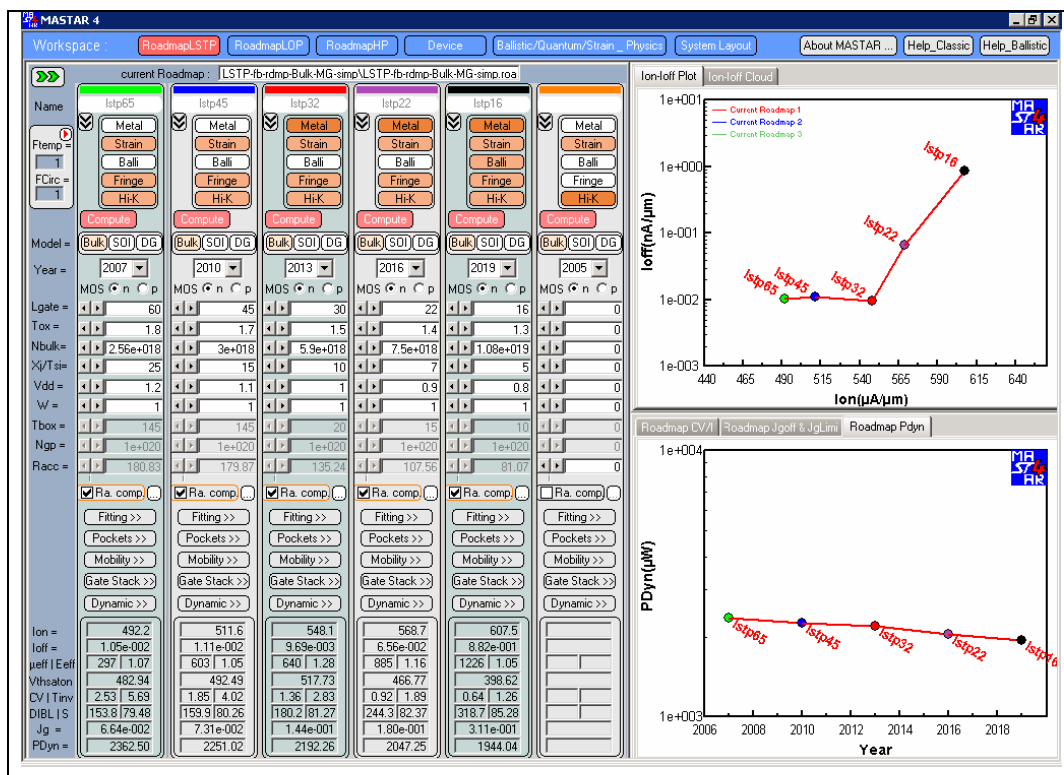


Figure 28: Global view of the workspace “Roadmap”.

The workspaces “Roadmap” have been created for the ITRS PIDS Working Group to enable the conception of CMOS Roadmaps. It can also be very useful for the comparison between different CMOS technologies or technological options within a CMOS technology. For this purpose the workspace is subdivided in three different application families, which are: LSTP (Low Standby Power), LOP (Low Power) and HP (High Performance).

Each workspace is separated in two functional parts: on the left side, up to 6 different profiles can be loaded, visualized and modified independently. For example, we can use it to trace the evolution of the roadmap from the node 100nm down to 22nm by choosing the most appropriate technology.

On the right side, some graphics are shown: on the top, the performance values in terms of Ion-Ioff-data points are plotted. Below, the user can choose between the graphics Roadmap CV/I , Roadmap J_g & J_{gLimit} and Roadmap $Pdyn$.

Loading and modifying profiles

Profile files can be loaded in the window by clicking on the yellow button and by choosing the desired profile file from the list. Once loaded in the window, all input

variables can be modified. If you want the changes to be permanent just click on the green button, the profile file will then be updated.

The following features can be chosen:

- Load Profile:** loads a profile
- Save Profile:** saves a profile
- Save Profile As:** saves the profile under a different name
- Close Profile:** closes the profile in the corresponding window
- Label Display:** allows the user to change the position of the data label with respect to the data point
- Include into:** allows the user to insert a data point into a line

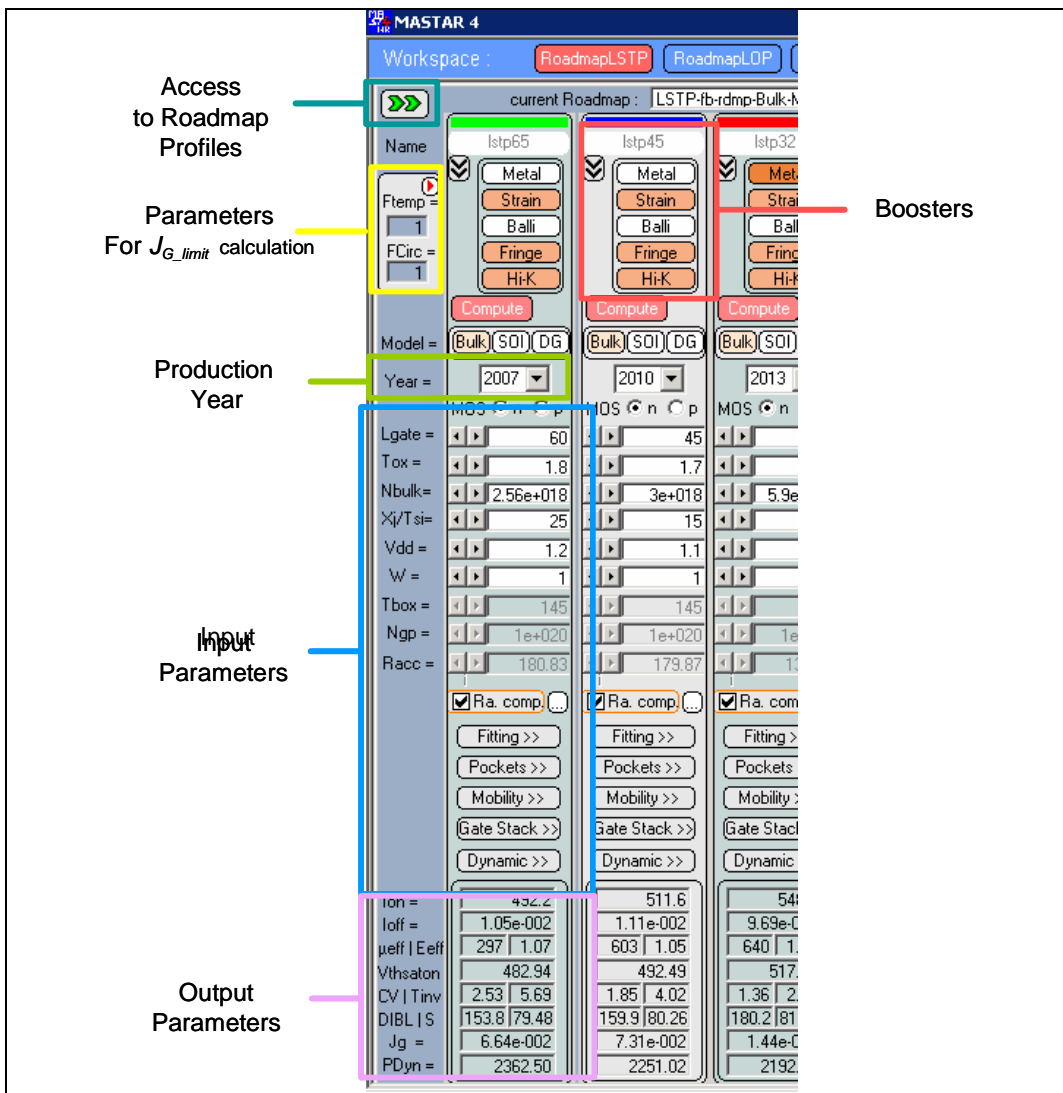


Figure 29: Description of the profile window in the workspace "Roadmap".

The double arrow symbol

You can also save all “Roadmap” profiles at once by using the menu behind the green double arrow at the upper left side of the working space. The following features can be chosen:

- Load Roadmap Profile:** loads a set of Roadmap Profiles
- Save Roadmap Profile:** saves a set of Roadmap Profiles
- Save Roadmap Profile As:** saves a set of Roadmap Profiles under a different name

Moreover, the calculation software can be changed (*Change Dll file*) and the option of calculation at constant I_{off} can be chosen.

Two other commands may be useful in order to export data to other applications:

- Snapshot Roadmap Window:** loads the Roadmap window into a clipboard, from where it can be pasted in any document by the combination Ctrl+V
- Copy Data to Clipboard:** loads all Roadmap parameters into the clipboard from where it can be pasted in a Excel sheet by the combination of Ctrl+V

Calculation options and display of the numerical results

On the bottom of every profile column, the basic electrical characteristics are displayed such as I_{on} , I_{off} , E_{eff} , μ_{eff} , V_{tsat} , CV/I , T_{inv} , $DIBL$, S , I_g and P_{dyn} . The values are updated whenever you confirm the changes done on an input parameter with the “Compute”-button.

For performance comparisons, you might wish to keep the I_{off} -value constant during the modification of parameters. To do this, click on the button with the green symbol on the upper left side of the window and activate “Keep Ioff constant”. In this case, the channel doping and thus the threshold voltage is automatically adjusted to keep the off current constant.

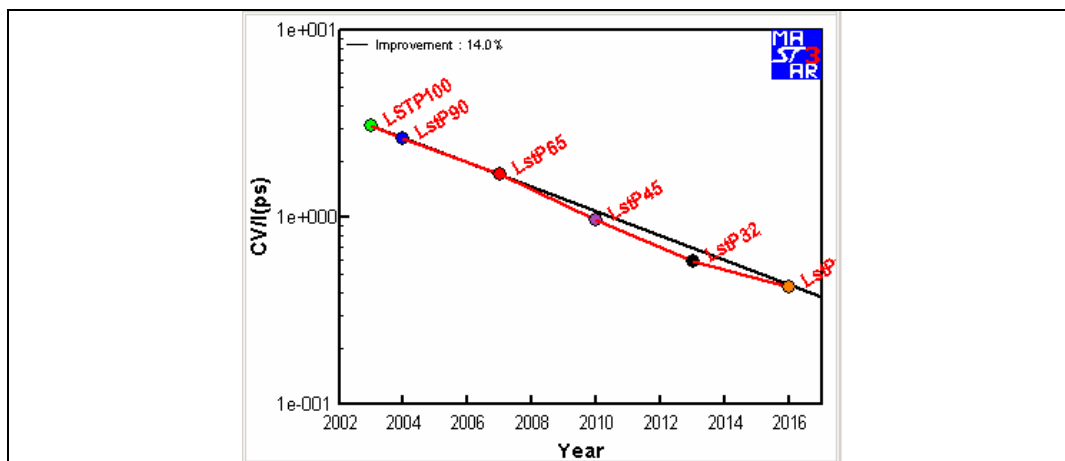


Figure 30: The CV/I versus year of introduction graphics.

Graphical output

The graphical output of all loaded profiles is automatically displayed on the graphics on the right side. The upper graph shows the Ion-Ioff. Clicking on the right mouse button, you can carry out some modifications on the plot, such as changes in the scaling (“Modify Scale”), copy the graphics into a clipboard for future use in documents (“Copy to Clipboard”) and the selection or presentation of the data points (“Load and Unload Plot” and “Create / Modify Plot”).

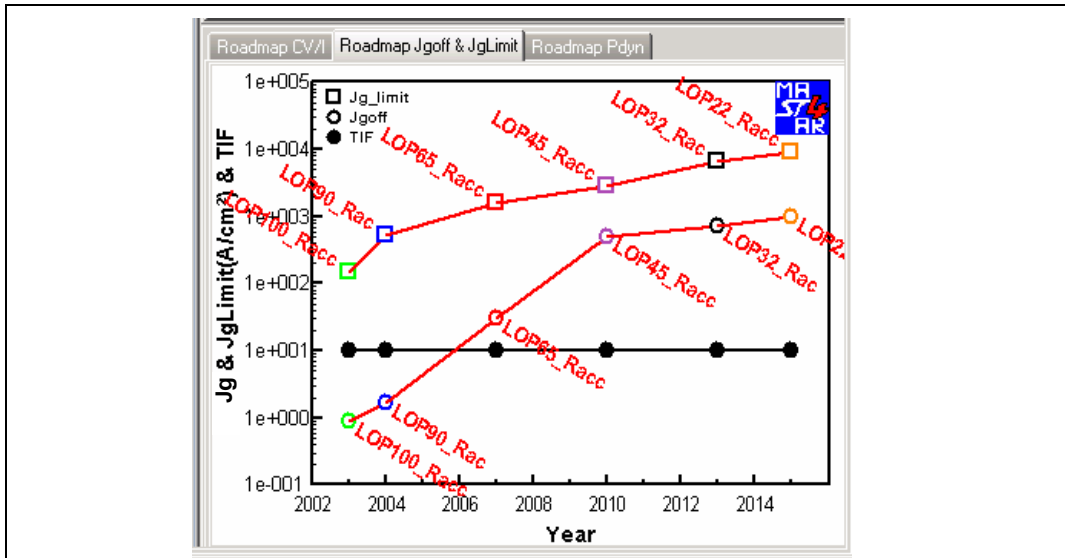


Figure 31: The J_g and $J_{g,Limit}$ -roadmap versus the year of introduction.

The lower graphics has three presentations: you can choose between the presentations of the gate delay CV/I , J_g & $J_{g,Limit}$ or the dynamic Power versus the year of introduction. In order to monitor the performance improvements from one generation to another in a convenient way, you can switch between frequency and delay presentation. Note that you can disable the plotting of the introduction year on the x-axis: just use the right mouse button and deactivate “Enable year”. In the graphics window, the data points are now ordered from the left to the right as they appear in the profile frames.

For the second graphics, J_g & $J_{g,Limit}$, the parameter $J_{g,Limit}$ shows the upper limit, which is acceptable for the gate leakage. It is derived from the source-drain leakage current I_{off} and the gate length L_g using the following formula:

$$J_{g,Limit} = \frac{TempFactor}{CircuitFactor} \cdot \frac{I_{off}}{L_g} \cdot InitialFactor$$

where $TempFactor$, $CircuitFactor$ and $InitialFactor$ are adjustable factors taking into account the temperature dependence of the I_{off} leakage current, the spread of the individual device characteristics within a circuit and the use of different types of transistors within the same chip and are by default different for LSTP, LOP and HP applications. The default values are listed in Table 11.

	LSTP	LOP	HP
Temp Factor	1	5	10
Circuit Factor	1	1	1
Initial Factor	1	1	0.1

Table 11: Default values for the $J_{g,Limit}$ calculation factors TempFactor, CircuitFactor and InitialFactor for the different application families.

The $J_{g,Limit}$ calculation factors are accessible via the red triangular symbol on the upper left part of the Roadmap Window (cf. Figure 29): the preference window will be opened, where the default values can be changed manually. In addition to that, the TIF value in use, i. e. the improvement factor with respect to a pure SiO₂ gate oxide, is indicated for every node.

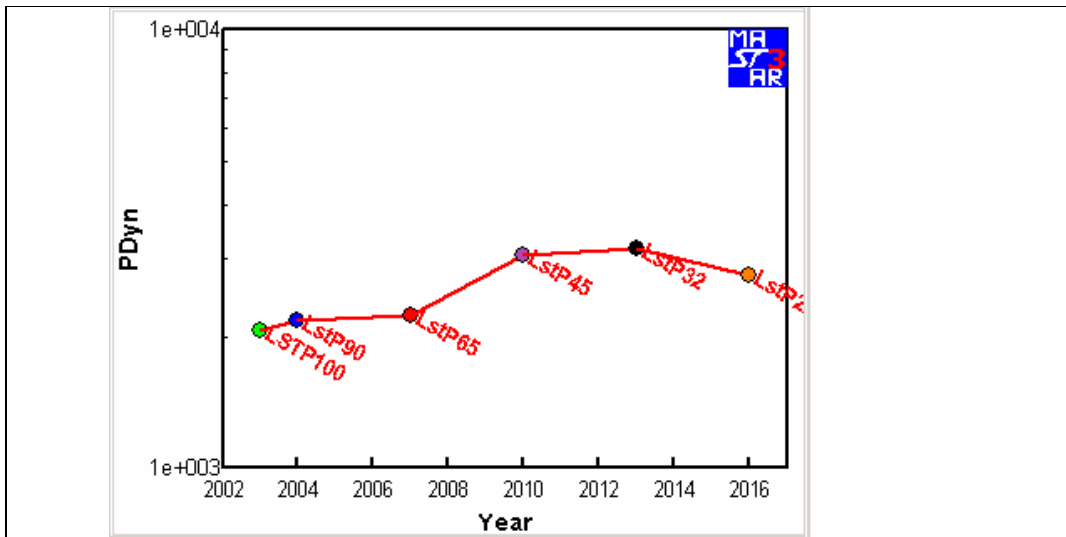


Figure 32: The Pdyn graphics.

Mastar On-Line Service

If you have any questions or suggestions, please send an e-mail to:

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- frederic.boeuf@st.com
- markus.muller@philips.com

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3. T. Skotnicki, G. Merckel et T. Pedron « Analytical Study of Punchthrough in Buried Channel p-MOSFETs », *IEEE Transaction On Electron Device*, Vol 36, N°4, 1989
4. T. Skotnicki, G. Merckel et A. Merrachi, « New Physical Model For Multiplication Induced Breakdown in MOSFETs », *Solid State Electronics*, Vol 34, N°11, pp1297-1307, 1991
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7. T. Skotnicki, « Heading for decanometer CMOS – is navigation among icebergs still a viable strategy? » *ESSDERC 2000*, Invited Paper
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9. T. Skotnicki, *Encyclopédie Technique de l'Ingénieur*, « Circuits intégrés CMOS sur silicium » Cahier E 2 432, février 2000
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10. T. Skotnicki and F. Bœuf, « CMOS Technology Roadmap – approaching uphill specials », chapter in proceedings of the 9th Intl. Symp. On Silicon Materials Science and Technology, Editors H. R. Huff, L. Fabry and S. Kishino, pp. 720-734, ECS Volume 2002-2
11. T. Skotnicki and F. Bœuf, « Introduction à la Physique du Transistor MOS », *EGEM « Physique des dispositifs pour circuits intégrés silicium »*, edited by J. Gautier, Editions Lavoisier, Paris 2003

ANNEX A:
The Mastar Equations (after Refs 6-9)

$\Delta L = 0.8X_j, L = L_g - \Delta L$	$N_{ch} = N_B + 2N_{poches} \frac{\min(L, L_{poches})}{L}$
$\phi_d = \frac{kT}{q} \ln \left(\frac{N_{ext} N_{ch}}{n_i^2} \right)$	$N_{poches} = \frac{1}{2} \frac{C_{poches}}{R_p + 2\Delta R_p}$ $L_{poches} = (R_p + 2\Delta R_p) \sin \theta + 2\Delta R_l \cos \theta - \frac{\Delta L}{2}$
$2\phi_F = \frac{kT}{q} \ln \left(\frac{N_{ch}}{n_i} \right)^2$ $NCE = \frac{\epsilon_{Si}}{\epsilon_{ox}} \frac{T_{ox} T_{dep}}{W^2} \sigma$	$SCE = 0.64 \frac{\epsilon_{Si}}{\epsilon_{ox}} \left(1 + \frac{X_j^2}{L^2} \right) \frac{T_{ox_el}}{L} \frac{T_{dep}}{L} \phi_d$ $DIBL = 0.8 \frac{\epsilon_{Si}}{\epsilon_{ox}} \left(1 + \frac{X_j^2}{L^2} \right) \frac{T_{ox_el}}{L} \frac{T_{dep}}{L} V_{DS}$
$RSCE = \frac{\sqrt{2\epsilon_{Si} q N_B (2\phi_F - V_{BS})}}{C_{ox}} \left(\sqrt{\frac{N_{ch}}{N_B}} - 1 \right)$	$V_{th\infty} = V_{FB} + 2\phi_F + \frac{1}{C_{ox_eot}} \sqrt{2\epsilon_{Si} q N_B (2\phi_F - V_{BS})}$ $V_{th,off} = V_{th\infty} + RSCE - SCE - DIBL - NCE$
If Kappa=0, then $S = \frac{kT}{q} \ln 10 \left(1 + \frac{\epsilon_s}{\epsilon_{ox}} \frac{T_{ox_el}}{T_{dep}} \right)$ else S=Kappa	$\log I_{off} = \log(I_{th}) - \frac{V_{th,off}}{S}$ $I_{th} = 5 \times 10^{-7} [A] \frac{W}{L}$ $I_{th_new} = 5 \times 10^{-7} [A] \frac{W}{L} 8 \times 10^8 N_{ch}^{-0.4865} [cm^{-3}]$
$T_{dep} = \sqrt{\frac{2\epsilon_s}{qN_{ch}} (2\phi_F - V_b)}$	$T_{ox_el} = T_{phys} \frac{\epsilon_{SiO2}}{\epsilon_{actual}} + D_{ark_space} + P_{oly_depl}$
$\mu_{eff} = K_{mu} \frac{\mu_{sr} \mu_{ac}}{\mu_{sr} + \mu_{ac}}$	nMOS: $\mu_{ac} \left[\frac{cm^2}{Vs} \right] = 330 E_{eff}^{-0.3} \left[\frac{MV}{cm} \right]$ pMOS: $\mu_{ac} \left[\frac{cm^2}{Vs} \right] = 90 E_{eff}^{-0.3} \left[\frac{MV}{cm} \right]$
nMOS: $\mu_{sr} \left[\frac{cm^2}{Vs} \right] = 1450 E_{eff}^{-2.9} \left[\frac{MV}{cm} \right]$ pMOS: $\mu_{sr} \left[\frac{cm^2}{Vs} \right] = 140 E_{eff}^{-1} \left[\frac{MV}{cm} \right]$	nMOS: $E_{eff} = K_{field} \left(\frac{V_G + V_{th,on}}{6T_{ox_el}} - 2 \frac{V_{FB} + 2\phi_F}{6T_{ox_el}} \right)$ pMOS: $E_{eff} = K_{field} \left(\frac{V_G + 2V_{th,on}}{9T_{ox_el}} - 3 \frac{V_{FB} + 2\phi_F}{9T_{ox_el}} \right)$
$V_{th,on} = V_{th,off} + \Delta$	$V_{gt} = V_{gs} - V_{th,on}$
$C_{ox_el} = \frac{\epsilon_{SiO2}}{T_{ox_el}}$	$I_{dsat0} = \frac{1}{2} \mu_{eff} C_{ox_el} \frac{W}{L} V_{gt} V_{dsat}$
$V_{dsat} = \frac{1}{\frac{1}{L E_c} + \frac{1}{V_{gt}}}$; $E_c = K_{vs} \frac{2V_{sat}}{\mu_{eff}}$	$d = K_d \frac{K_B}{2\sqrt{2\phi_F - V_b}}$

$K_B = \frac{qN_{ch}T_{dep}}{C_{ox_el}\sqrt{2\phi_F - V_b}}$	$I_{dsat} = \frac{I_{dsat0}}{1 + \frac{2R_s I_{dsat0}}{V_{gt}} - \frac{R_s I_{dsat0}}{V_{gt} + L_{el}E_c(1+d)}}$
Dark_space \cong 2-4 Å EOT (electrons) et 3-5Å EOT (holes)	Poly_dep \cong 4Å EOT (n ⁺ -gate), 6Å EOT (p ⁺ -gate), EOT= $T_{phys} \epsilon_{SiO2} / \epsilon_{actuel}$
$I_G = \frac{1}{2} \Delta LW \times ae^{(bV_g^2 + cV_g)} e^{-dT_{ox_phys}}$ Parameters for J _g : a=1.44.10 ⁵ A/cm ² , b=-4.02 V ⁻² , c=13.05 V ⁻¹ , d = 1.17 Å ⁻¹	

ANNEX B: Delay and Power Consumption

The MASTAR equations are the following:

$C_{g_ideal} = \frac{\epsilon_{SiO2}}{T_{ox_el}} L_{gate}$ $C_g = \left[\frac{\epsilon_{SiO2}}{T_{ox_el}} L_{gate} + C_{total_fringing} \right] W$ $C_{g_load} = \left[\frac{\epsilon_{SiO2}}{T_{ox_el}} L_{gate} + C_{total_fringing} + C_{overlap} \right] W$ $C_{load_nmos} = C_{g_load} + C_{junction}$ $C_{load_inv} = 3(C_{g_load} + C_{junction})$ $t_{invert} (NMOScase) = 0.25k_{load} C_{load_inv} V_{dd} \left(\frac{2}{I_{on}W} \right) 10^6$ $t_{invert} (PMOScase) = 0.25k_{load} C_{load_inv} V_{dd} \left(\frac{2}{I_{on}2.2W} \right) 10^6$	$P_{stat} = 3.2WV_{dd} (I_G + I_{off}) 10^{-9}$ $P_{dyn} = \frac{2}{t_{invert}} C_{load_inv} V_{dd}^2$ <div style="border: 1px solid black; padding: 5px; margin-top: 10px;"> <p style="text-align: center;">Dynamic</p> <p>CgVdd/Ion= 2.18 ps</p> <p>t_invert = 4.37 ps</p> <p>RgCg = 3.55e-002 ps</p> <p>Cg = 1.18e-015 F/μm</p> <p>Cload_inv = 4.71e-015 F/μm</p> <p>Cjunc = 2.00e-016 F/μm</p> <p>Pstat = 3.44e-003 μW</p> <p>Pdyn = 2.16e+003 μW</p> </div>
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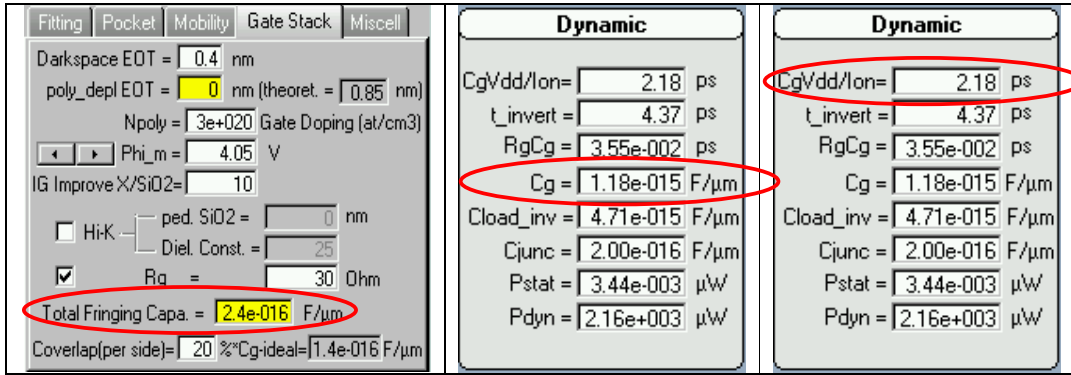
C_g, C_{load_inv}, C_{junc} and C_{load_nmos} are calculated in F. For W=1μm, the this is equal to F/μm.

The delay equations:

- 1) The Intrinsic Delay of the transistor $t = C_g V_{dd} / I_{on}$:

$$t = \frac{C_g V_{dd}}{I_{on}}, \text{ where } C_g = \left[\frac{\epsilon_{SiO2}}{T_{ox_el}} L_{gate} + C_{total_fringing} \right] W$$

C_{total_fringing} is defined in the booster window and appears in the gate stack menu. The value can be manually adjusted. A common value is C_{total_fringing} = 3C_{fringe} = 3*0.08 fF/μm = 0.24 fF/μm.

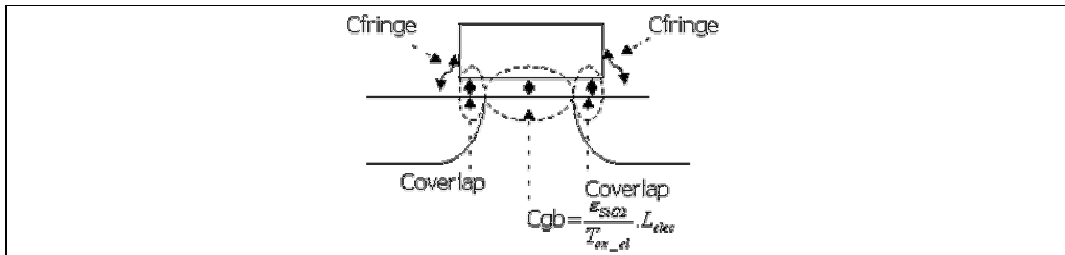


Loading gate capacitance:

$$C_{g_load} = \frac{\epsilon_{SiO2}}{T_{ox_el}} L_{elec} + 2C_{fringe} + 2C_{overlap} + \underbrace{C_{fringe} + C_{overlap}}_{Miller_capacitance} = \frac{\epsilon_{SiO2}}{T_{ox_el}} \cdot L_{gate} + \underbrace{3C_{fringe}}_{C_{total_fringing}} + C_{overlap}$$

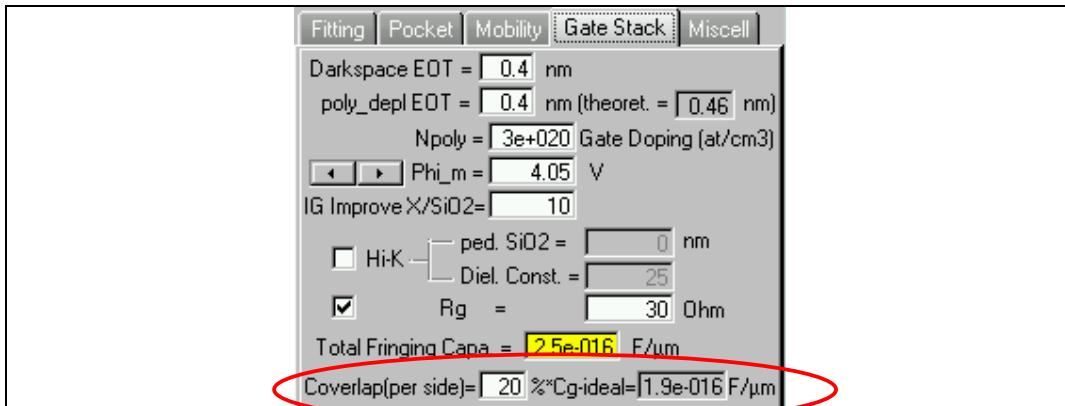
In the calculation, $C_{g_load} (F) = C_{g_load} (F/\mu m) \cdot W(\mu m)$

(after Japanese PIDS ITRS Working Group).



(illustration after the Japanese PIDS ITRS Working Group)

We consider here that the overlap capacitance is a percentage of the ideal gate capacitance. The value is adjusted in the gate stack menu.



2) The inverter delay t_{invert}

Dynamic	
CgVdd/lon=	2.18 ps
t_invert =	4.37 ps
RgCg =	3.55e-002 ps
Cg =	1.18e-015 F/ μm
Cload_inv =	4.71e-015 F/ μm
Cjunc =	2.00e-016 F/ μm
Pstat =	3.44e-003 μW
Pdyn =	2.16e+003 μW

For the calculation, we use the following formulae:

$$t_{invert} = 0.25k_{load} C_{load_inv} V_{dd} \left(\frac{2}{I_{on} \cdot W} \right) 10^6, \text{ with}$$

$$C_{load_nmos} = C_{g_load} + C_{junction}$$

$$C_{load_pmos} = 2C_{load_nmos}$$

$$C_{load_inv} = C_{load_nmos} + C_{load_pmos} = 3C_{load_nmos} = 3(C_{g_load} + C_{junction})$$

$$C_{junction} = 4C_{j0}W \left(\frac{Metal1pitch}{2} \right)$$

Capacitance	Dynamic	Dynamic
Cox_elec = 1.44e-014 F/ μm^2	CgVdd/lon= 2.18 ps	CgVdd/lon= 2.18 ps
Cdep_sub = 4.46e-015 F/ μm^2	t_invert = 4.37 ps	t_invert = 4.37 ps
Cg_ideal = 9.34e-016 F/ μm	RgCg = 3.55e-002 ps	RgCg = 3.55e-002 ps
Cload_nmos = 1.57e-015 F/ μm	Cg = 1.18e-015 F/ μm	Cg = 1.18e-015 F/ μm
	Cload_inv = 4.71e-015 F/ μm	Cload_inv = 4.71e-015 F/ μm
	Cjunc = 2.00e-016 F/ μm	Cjunc = 2.00e-016 F/ μm
	Pstat = 3.44e-003 μW	Pstat = 3.44e-003 μW
	Pdyn = 2.16e+003 μW	Pdyn = 2.16e+003 μW

Fitting Pocket Mobility Gate Stack Miscell
 Next = 1e+020 LDD doping in at/cm3
 M1Pitch = 100 nm

The Metal1 pitch is manually adjusted in the “miscell” window, as it depends of the technology node.

The junction capacitance can be adjusted in the “technology flavor” menu: it is $C_{j0}=1$ fF/ μm for bulk and can be manually reduced for SOI or DG choice.

K_{load} is a fitting parameter and can be manually adjusted in the Fitting parameter window as a function of the connection capacitances and of the architecture (bulk, SOI, DG...). A good value is between 5 and 10.

Depending of the chosen K_{load} value, t_{invert} gives the inverter delay of an ideal inverter, a non-ideal inverter and a heavy loaded inverter.

$K_{load}=1$ corresponds to an ideal inverter	Kload = <input type="text" value="1"/> Ideal Inverter
---	---

3) The inverter delay for a non-ideal inverter:

$1 < K_{load} < 10$ corresponds to a low loaded inverter (Ring Oscillator type)	Kload = <input type="text" value="5"/> Low Load IRQ type1
---	---

4) The inverter delay for a heavily loaded inverter:

$K_{load} > 10$ corresponds to a heavily loaded inverter	Kload = <input type="text" value="10"/> Heavy-loaded Inverter
--	---

5) The total inverter delay including the interconnect delay:

Finally, a total inverter delay is calculated taking into account the resistance and capacity of the interconnects. For this purpose, the user can adjust in the gate stack window the gate resistance. The inverter delay is then corrected by the $R_g \cdot C_g$ term:

$$T_{invert} = t_{invert} + R_g \cdot C_g$$

This $R_g \cdot C_g$ additive term is taken into account only if the gate resistance is activated. In that case, the user has to enter the gate resistance value, calculated with the following:

R_g (Ohms) = Gate resistance(Ohms/square)*Number of squares, and has to be calculated by the user (depends on the layout).

Fitting	Pocket	Mobility	Gate Stack	Miscell
Darkspace EOT = <input type="text" value="0.4"/> nm				
poly_depl EOT = <input type="text" value="0.4"/> nm (theoret. = <input type="text" value="0.46"/> nm)				
Npoly = <input type="text" value="3e+020"/> Gate Doping (at/cm3)				
Phi_m = <input type="text" value="4.05"/> V				
IG Improve X/SiO2 = <input type="text" value="10"/>				
<input type="checkbox"/> Hi-K <input type="checkbox"/> ped. SiO2 = <input type="text" value="0"/> nm <input type="checkbox"/> Diel. Const. = <input type="text" value="25"/>				
<input checked="" type="checkbox"/> Rg = <input type="text" value="30"/> Ohm				
Total Fringing Capa. = <input type="text" value="2.5e-016"/> F/μm				
Overlap(per side) = <input type="text" value="20"/> %*Cg-ideal = <input type="text" value="1.9e-016"/> F/μm				

Dynamic	
CgVdd/Ion =	<input type="text" value="2.18"/> ps
t_invert =	<input type="text" value="4.37"/> ps
RgCg =	<input type="text" value="3.55e-002"/> ps
Cg =	<input type="text" value="1.18e-015"/> F/μm
Cload_inv =	<input type="text" value="4.71e-015"/> F/μm
Cjunc =	<input type="text" value="2.00e-016"/> F/μm
Pstat =	<input type="text" value="3.44e-003"/> μW
Pdyn =	<input type="text" value="2.16e+003"/> μW

In the case of PMOS calculation, the inverter delay t_{invert} is calculated taking $I_{on} = 2,2 \cdot I_{onPMOS}$. Due to different access resistances, we recommend to use the NMOS calculation for the inverter delay evaluation.

Static and Dynamic Power equations :

For the static power calculation, we uses the following formulae [1] :

$$P_{stat} = W_{nmos} (I_{GN} + I_{offN}) + W_{pmos} (I_{GP} + I_{offP}) = 3.2WV_{dd} (I_G + I_{off})$$

$$W_{pmos} = 2.2W_{nmos}$$

For the dynamic power calculation, we use the following formulae [1]:

$$P_{dyn} = \frac{2}{t_{invert}} C_{load_inv} V_{dd}^2 \text{ with the previous calculated } t_{invert} \text{ and } C_{load_inv}.$$

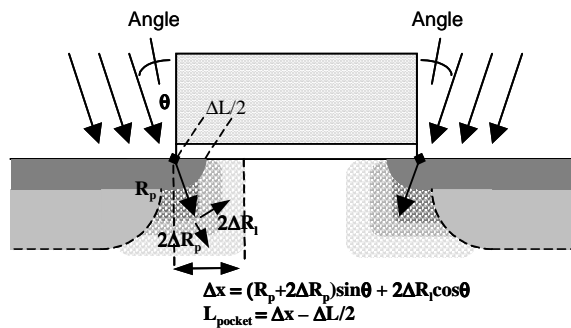
Dynamic	Dynamic
CgVdd/lon= 2.18 ps	CgVdd/lon= 2.18 ps
t_invert = 4.37 ps	t_invert = 4.37 ps
RgCg = 3.55e-002 ps	RgCg = 3.55e-002 ps
Cg = 1.18e-015 F/μm	Cg = 1.18e-015 F/μm
Cload_inv = 4.71e-015 F/μm	Cload_inv = 4.71e-015 F/μm
Cjunc = 2.00e-016 F/μm	Cjunc = 2.00e-016 F/μm
Pstat = 3.44e-003 μW	Pstat = 3.44e-003 μW
Pdyn = 2.16e+003 μW	Pdyn = 2.16e+003 μW

The equations that are used for the delay calculation, static power and dynamic power are described in the annex A (Mastar equations), and can be found in ref [1].

[1] T. Skotnicki, Encyclopédie Technique de l'Ingénieur, « Circuits integres CMOS sur silicium » Cahier E 2 432, février 2000

ANNEX C: Pocket Module

Illustration of the Pocket Module Parameters



Projected range R_p , longitudinal dispersion ΔR_p and lateral dispersion ΔR_l are calculated with SRIM-2003.

ANNEX D: Symmetrical Double Gate with common gate bias

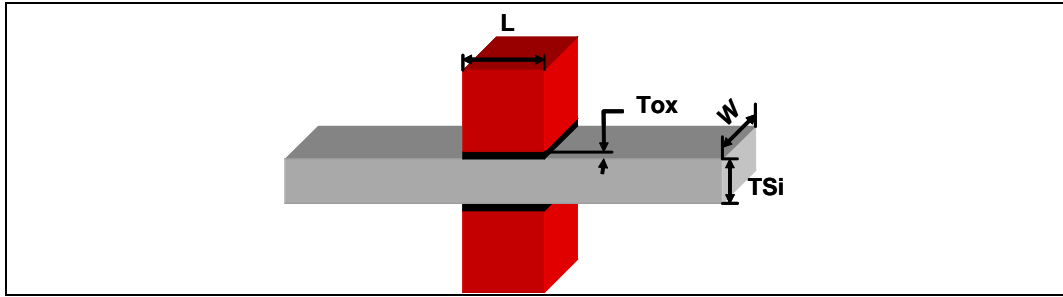


Figure 33: Schematic view of the planar DG device and explanation of the principle geometry parameters.

The specific MASTAR DG equations in detail:

$T_{dep} = \min\left(\sqrt{\frac{2\epsilon_s}{qN_{ch}}(2\phi_F - V_b)}, \frac{TSi}{2}\right)$ $T_{dep0} = \min\left(\sqrt{\frac{2\epsilon_s}{qN_B}(2\phi_F - V_b)}, \frac{TSi}{2}\right)$	$X_j = \alpha \cdot T_{Si} \text{ where } \alpha = 1/2$
$\Delta L = 2 * 0.8 X_j, \quad L = L_g - \Delta L$	$DIBL = \zeta 1 \left(1 + \frac{X_j^2}{L^2}\right) \frac{T_{ox_el}}{L} \frac{T_{dep}}{L} V_{DS}$ $SCE = \zeta 2 \left(1 + \frac{X_j^2}{L^2}\right) \frac{T_{ox_el}}{L} \frac{T_{dep}}{L} \phi_d$
<p style="text-align: center;">NMOS :</p> $E_{eff} = \frac{V_G + V_{th,on}}{6T_{ox_el}} - 2 \frac{V_{FB} + 2\phi_d - \psi_{SUP}}{6T_{ox_el}}$ <p style="text-align: center;">PMOS :</p> $E_{eff} = \frac{V_G + 2 \cdot V_{th,on}}{9T_{ox_el}} - 2 \frac{V_{FB} + 2\phi_d - \psi_{SUP}}{9T_{ox_el}}$	$V_{th} = V_{FB} + \phi_d - \psi_{sup} + \frac{qN T_{dep0}}{C_{ox_eot}}$ $\psi_{sup} = \phi_d - 2\phi_F - \frac{KT}{q} \left[\ln \left(\frac{KT}{q^2} \cdot \frac{1}{N_A} C_{ox} e^{\frac{(q-1)}{2}} \right) \right]$

Comments:

- (1) The depletion depth is $T_{Si}/2$ if this value is below the theoretical bulk depletion depth value.
- (2) X_j – entering in the DIBL and SCE equations - is set equal to half the channel thickness T_{Si} .
- (3) For the electrical channel length correction the lateral diffusion factor is by default twice the bulk default value to take into account the full depth T_{Si} (cf. (2)).
- (4) The effective transverse field has an additional term due to coupling between both gates.
- (5) The threshold voltage is decreased by Ψ_{sup} which describes the coupling between both gates [1,2].

[1] D.Munteanu et al, Solid-State Electron. 47, 1219 (2003)

[2] D.Munteanu et al., Proceedings of the 4th European workshop ULIS'2003, p. 35 (2003).

ANNEX E: FDSOI

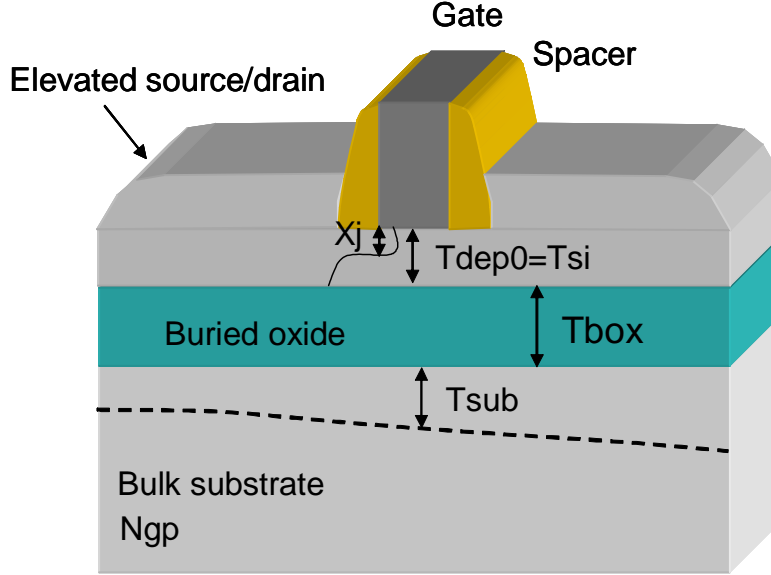


Figure 34: Schematic of the FDSOI device showing the principle geometry parameters.

The specific MASTAR SOI equations in detail:

$X_j = T_{si}$	$V_{th} = V_{FB} + \phi_d + \Psi_{BOX} + \frac{qN_A T_{si}}{C_{ox_eot}}$
<p>If Kappa=0, then</p> $S = \frac{kT}{q} \ln 10 \left(1 + \frac{3T_{ox_el}}{T_{si} + 3.T_{box} + T_s} \right)$ <p>else S=Slope</p>	<p>where $\Psi_{BOX} = \frac{qN_{GP}T_{sub}}{C_{ox_eot}}$</p> <p>with</p> $T_{sub} = -(T_{si} + 3T_{box}) + \sqrt{(T_{si} + 3T_{box})^2 + \frac{2\varepsilon_{si}\phi_d}{qN_{GP}} - \frac{N_A}{N_{GP}} T_{si}^2}$
<p>NMOS :</p> $E_{eff} = \frac{V_G + V_{th,on} - 2 \frac{V_{FB} + \phi_d + \Psi_{BOX}}{6T_{ox_el}}}{6T_{ox_el}}$ <p>PMOS :</p> $E_{eff} = \frac{V_G + 2V_{th,on} - 3 \frac{V_{FB} + \phi_d + \Psi_{BOX}}{9T_{ox_el}}}{9T_{ox_el}} \text{ with } V_g = V_{dd}$	$SCE = 1. \frac{\varepsilon_{Si}}{\varepsilon_{ox}} \left(1 + \frac{(\alpha * X_j)^2}{L^2} \right) \frac{T_{ox_el}}{L} \frac{T_{si}}{L} \phi_d$
$DIBL = 0.77 \frac{\varepsilon_{Si}}{\varepsilon_{ox}} \left(1 + \frac{(\alpha * X_j)^2}{L^2} \right) \frac{T_{ox_el}}{L} \frac{T_{si} + \rho \frac{(L - T_{si})3.T_{box}}{L - T_{si} + 3.T_{box}}}{L} V_{dd} + \beta \Delta_{box}^{DIBL}$ <p>with $\rho=1$ for SOI and 0 for bulk and DG and</p>	

$$\Delta_{box}^{DIBL} = \frac{T_{ox_el} \cdot T_{si}}{L^2} \frac{\sqrt{(T_{si} + 3T_{box})^2 - L^2}}{L} \cdot V_{dd}$$

if $T_{si} + 3T_{box} < L$ then $\Delta_{box}^{DIBL} = 0$

Comments:

- (1) X_j is set by default equal to T_{si} .
- (2) In case of fully-depleted SOI an additional term ψ_{SOI} appears in the threshold voltage to take into account the possible depletion under the buried oxide in the case of thin BOX. N_{GP} is the doping level under the BOX.
- (3) In the case of elevated LDD regions, the X_j might be smaller than T_{si} . In this case the parameter α can be set < 1 with a describing the ratio between X_j and T_{si} .
- (4) In the equation of the subthreshold slope, an additional term accounts for the capacitance of the BOX.
- (5) The parameter ρ is efficient only in SOI model and the $\Delta_{DIBL,BOX}$ term has been added to take into account the observed DIBL increase with increasing BOX thickness due to drain – channel coupling through the BOX. (cf. 31 - 33).
- (6) A comparison between DIBL values obtained by TCAD and by MASTAR is presented Figure 33 confirming the validity of the MASTAR modeling.

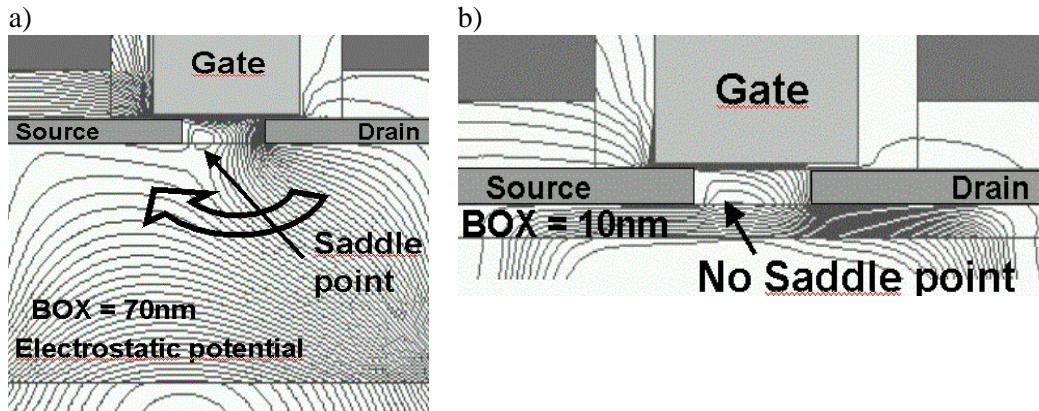


Figure 35: Illustration of the DIBL increase with BOX thickness to drain – channel coupling through the BOX which is taken into account by the factor ρ and the $\Delta_{DIBL,BOX}$ term: (a)-70nm BOX; (b)-10nm BOX.

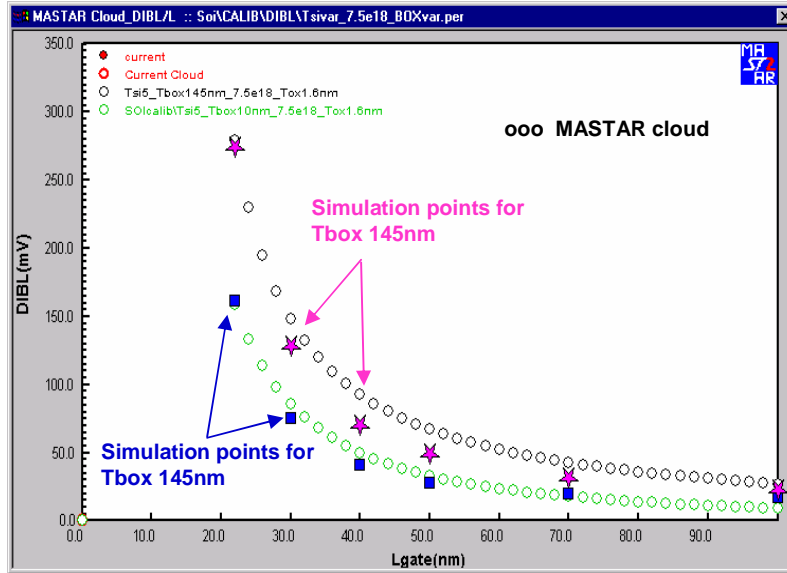


Figure 36: Comparison of TCAD simulation and DIBL calculations by MASTAR for FDSOI devices with $T_{BOX} = 10\text{nm}$ and $T_{BOX} = 145\text{nm}$, ($N_{ch} = 7.5e18\text{cm}^{-3}$ and $T_{ox} = 1.6\text{nm}$ and $V_{dd}=0.8\text{V}$).

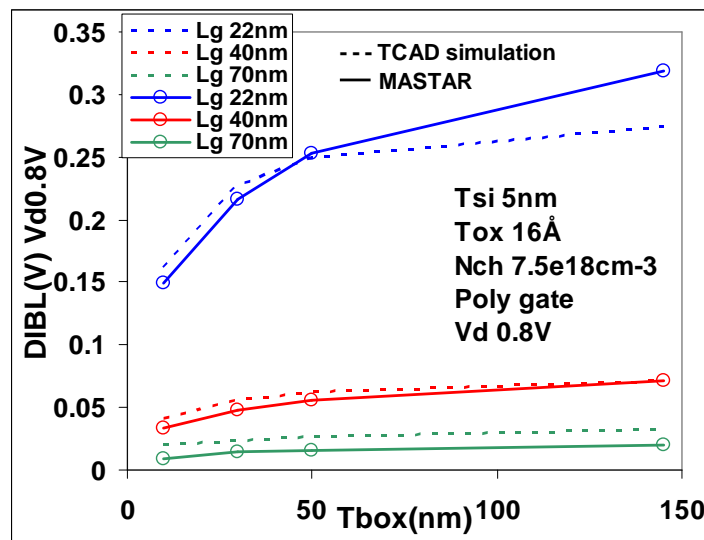


Figure 37: Illustration of the good matching between TCAD simulation and DIBL calculations by MASTAR for FDSOI devices with variable T_{BOX} between 10nm and 145nm, ($N_{ch} = 7.5e18\text{cm}^{-3}$ and $T_{ox} = 1.6\text{nm}$ and $V_{dd}=0.8\text{V}$).

ANNEX F: High-K oxides impact on SCE, DIBL, Gate Leakage Improvement and mobility

SCE and DIBL

In the case of High-K oxides, the fitting parameters ζ_1 and ζ_2 , which are used for the calculation of DIBL and SCE are slightly increased. Indeed, based on TCAD

simulations, we use the following substitutions for both parameters when the High-K module is activated:

$$\zeta_1 \rightarrow \zeta_1 * (1 + k_{DIBL} * \alpha_1 * ((T_{ox} + Ped.SiO_2) - 20\text{\AA})) \text{ avec } \alpha_1 = 0.015$$

$$\zeta_2 \rightarrow \zeta_2 * (1 + k_{SCE} * \alpha_2 * (\epsilon_{mean} - 15)) \text{ avec } \alpha_2 = 0.0078$$

This substitution is valid in the range of $15 < \epsilon_{mean} < 30$ and $20\text{\AA} < T_{ox} + ped.SiO_2 < 50\text{\AA}$ which is the usual range for High-K oxides. By default, the k_{SCE} and k_{DIBL} take the value of 1, but can be adjusted or even set to 0 in the booster characteristics window (cf. Figure 10).

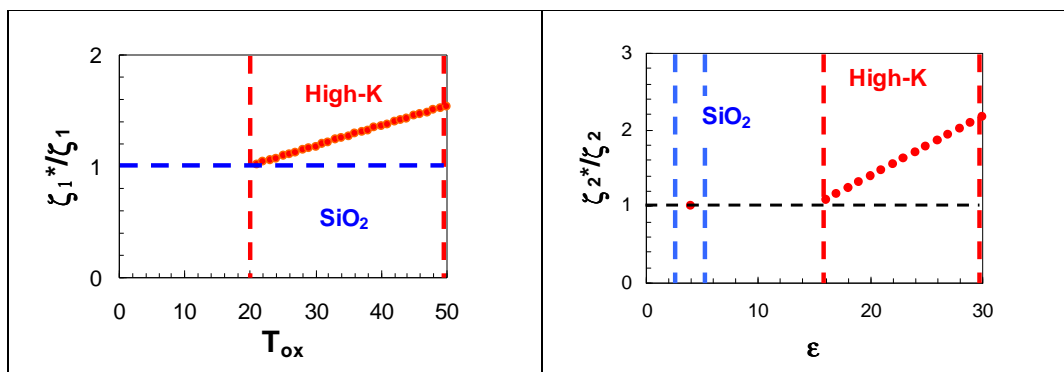


Figure 38: Evolution of the DIBL and SCE fitting factors z_1 and z_2 as a function of the total physical gate oxide thickness and dielectric constant according to TCAD simulations.

Gate Leakage Improvement

The objective of the use of High-K oxides is the reduction of the gate leakage current. The oxide leakage of High-K oxides is very difficult to asset as it depends on a number of parameters such as pedestal oxide thickness, high-K oxide thickness, barrier heights, process conditions etc. For MASTAR, we follow an empirical approach which is justified by the literature data: the best gate leakage data follows an exponential curve when plotted as a function of the EOT value just like the SiO₂ data (cf. Figure 39). Thus, we can introduce a technology improvement factor for the gate leakage TIF_{High-K} with respect to SiO₂ as a function of the EOT value (which is the physical equivalent thickness without poly-depletion and dark space).

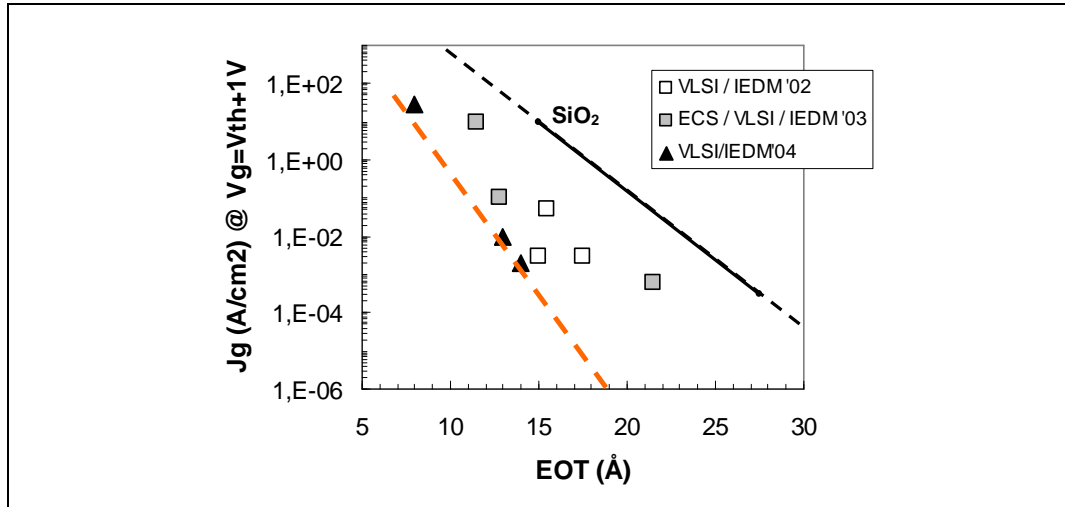


Figure 39: Literature trend for the gate oxide leakage in High-K oxides with respect to SiO₂.

This factor $TIF_{High-K}(EOT)$ also follows an exponential curve and can be calculated – knowing or estimating the gate leakage improvement for two distinct EOT-values – in the following way:

$$TIF_{High-K}(EOT) = 10^{(m \cdot EOT + C)}$$

with

$$m = \frac{\log(TIF_{High-K}(EOT_2)) - \log(TIF_{High-K}(EOT_1))}{EOT_2 - EOT_1}$$

and

$$C = \log(TIF_{High-K}(EOT_1)) - m \cdot EOT_1$$

Default values are $TIF_{High-K} = 50000$ for 20Å EOT and 500 for 10Å EOT which corresponds to the best literature values. These values can be changed inside the booster window (cf. Figure 10). Note that this function is only activated if the functionality inside the gate stack window is marked with a cross. As the reduction depends on the ratio between the thickness of the pedestal oxide and the high-K layer, the effective Technology Improvement Factor as appearing in the gate stack module is pondered by the following factor:

$$TIF_{High-K_eff} = \frac{ped.SiO_2}{ped.SiO_2 + T_{ox_High-K}} * TIF_{ped.SiO_2} + \frac{T_{ox_High-K}}{ped.SiO_2 + T_{ox_High-K}} * TIF_{High-K}$$

where $TIF_{ped.SiO_2}$ is the Technology Improvement factor of the pedestal oxide with respect to pure SiO₂.

High-K Mobility Degradation

In a similar way, the use of High-K oxides has an impact on the effective carrier mobility. Literature data suggests that the thickness of the pedestal oxide plays

the major role indicating mobility degradation for thin pedestal oxides. Therefore, MASTAR is equipped with a mobility reduction coefficient for High-K values $0 < K_{High-K} < 1$ which follows a linear trend below a critical oxide thickness. For its calculation we use the following equations:

$$K_{High-K}(ped.SiO_2) = m * ped.SiO_2 + C$$

with

$$m = \frac{K_{High-K}(ped.SiO_{22}) - K_{High-K}(ped.SiO_{21})}{ped.SiO_{22} - ped.SiO_{21}}$$

and

$$C = K_{High-K}(ped.SiO_{21}) - m * ped.SiO_{21}$$

where K_{High-K} can only adopt values between 0 and 1. Default values are $K_{High-K} = 0.6$ for $ped.SiO_2 = 5\text{\AA}$ and $K_{High-K} = 1$ for $ped.SiO_2 = 15\text{\AA}$. These values can be modified inside the booster window (cf. Figure 10). In the calculations, this factor is used as a multiplicative factor for the effective mobility calculation if the corresponding case inside the gate stack window is marked with a cross.

ANNEX G: New Slope - description of the model

Normally, the sub-threshold slope is defined by the following equation:

$$S = \left(\frac{\partial I_d}{\partial V_g} \right)^{-1} = \frac{kT}{q} \cdot \ln(10) \cdot \left(1 - \frac{1}{C_{ox}} \frac{\partial Q_d}{\partial \phi_s} \right)$$

For long channel devices:

$$S = \frac{kT}{q} \cdot \ln(10) \cdot \left(1 + \frac{\epsilon_s}{\epsilon_{ox}} \frac{T_{ox}}{T_{dep}} \right) = Cte$$

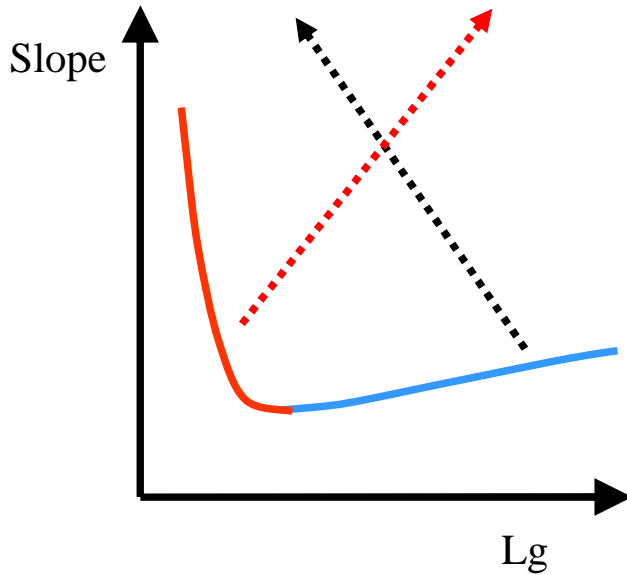
However, this model does not explain the Sub-threshold slope degradation which is observed for short channel devices. The use of the Voltage-Doping transformation (VDT) enables to take into account the variation of the equivalent depletion charge with ϕ_s which is responsible for the degradation of the sub-threshold slope [1].

According to [1], the new equations used are:

$$S = \frac{kT}{q} \cdot \ln(10) \cdot \left(1 - \frac{1}{C_{ox}} \frac{(Q_2 - Q_1)}{\phi_F} \right)$$

The depletion charges Q_1 and Q_2 are calculated for $\phi_{s1} = \phi_F$ and for $\phi_{s2} = 2\phi_F$ using the VDT:

$$Q_2 - Q_1 = \partial Q = \underbrace{-qN_{ch}(T_{dep2} - T_{dep1})}_{\text{Classical term}} - \underbrace{qX_j(N_{ch1}^* - N_{ch2}^*)}_{\text{New term}}$$



with T_{dep} and N_{ch}^* calculated from the VDT [1, 2]

$$T_{dep} = \left(\frac{q(N_{ch} - N_{ch}^*) \cdot X_j^2 + 2\phi_s \epsilon_s}{qN_{ch}} \right)^{1/2}$$

$$N_{ch}^* = N_{ch} - \frac{2\epsilon_s V_{ds}^*}{qL_{eff}^2}$$

$$V_{ds}^* = V_{ds} + 2(\phi_d - \alpha\phi_s) + 2\sqrt{(\phi_d - \alpha\phi_s)(V_{ds} + \phi_d - \alpha\phi_s)}$$

Empirically, α is found to lead to the best agreement with numerical simulations and experimental data by being put equal to:

$$\alpha = \frac{1}{2} \left(1 + \frac{T_{dep0}}{2L_{eff}} \right), \text{ with } T_{dep0} = \sqrt{\frac{2\epsilon_s \phi_d}{qN_{ch}}}$$

As illustrated in the above figure, this new term is responsible for the increase of the sub-threshold slope in small devices.

[1] R Gwoziecki and T. Skotnicki, "Physics of the subthreshold slope - initial improvement and final degradation in short CMOS devices", proc. ESSDERC, pp 639-642, 2002.

[2] T. Skotnicki, G. Merckel et T. Pedron, « The Voltage-Doping Transformation : A New Approach to the Modeling of MOSFET Short-Channel Effects », Electron Device Letters, Vol 9, N° 3, 1998

ANNEX H: Access resistance

Description of the model

The access resistance model included in MASTAR is based on the series of paper published by S.-D. Kim, C.-H.M. Park and J.C.S. Woo [1-4], which describe one of the most complete models for the access resistance.

The total parasitic resistance is divided into four major components:

- R_{ov} (overlap resistance), which corresponds to the resistance of the source drain extension region situated under the gate and that is not part of the channel
- R_{ext} (extension resistance), which corresponds to the resistance of the extension region situated under the sidewall spacer.
- R_{dp} (source/drain resistance), which corresponds to the resistance of the diffused source/drain region.
- R_{cont} (contact resistance), which corresponds to the resistance of the silicon-silicide interface.

Figure 40 represents a schematic view of the different components.

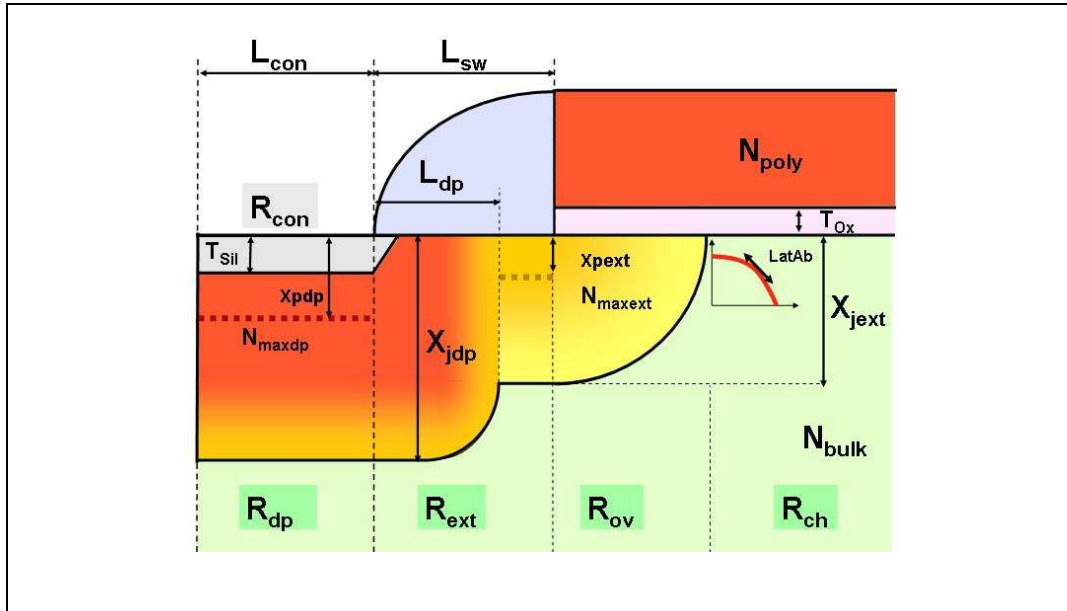


Figure 40: Schematic representation of the different resistance components and the associated characteristic lengths.

Calculation details

- R_{ov} :

Kim's model was implemented for the calculation of the overlap resistance that is extensively discussed in [1-5].

The equations used are the following where the factor 2 in R_{ov} takes into account the source and drain resistances that are supposed to be identical:

$$R_{ov} = 2 \times \left(Rac1 + \frac{1}{1/Rac2 + 1/Rsp_{ov}} \right) \quad (1)$$

$$Rac1 = \int_{L_{ov}-W_{ov}}^{L_{ov}} \frac{dy}{\mu_{ac}(y)N_{ac}(y)q} \quad (2)$$

$$Rac2 = \int_0^{L_{ov}-W_{ov}} \frac{dy}{\mu_{ac}(y)N_{ac}(y)q} \quad (3)$$

$$Rsp_{ov} = \int_0^{L_{ov}-W_{ov}} \frac{\rho_{ov}(y)}{(L_{ov}-W_{ov}-y) \tan \alpha + Tc} dy \quad (4)$$

resistance of the extension-overlap region. For a non-abrupt profile, the current lines will spread from the accumulation channel into the extension with a spreading angle α , see figure 2.

The mobility in the accumulation layer is calculated from the model described in [6]. The accumulation concentration is obtained from the calculation of the charge in the overlap Q_s , itself obtained from the surface potential, see [2]. A simple analytical model was used for the surface potential calculation, which is described in [5]. Knowing $\mu_{ac}(y)$ and $N_{ac}(y)$, R_{ac1} and R_{ac2} were obtained using numerical calculation. The spreading resistance was also obtained using numerical integration. The accumulation layer thickness was calculated from [6]. The resistivity ρ_{ov} was calculated from the extension doping (known from the maximum doping in the extension the abruptness and the y-position assuming a gaussian profile) and the mobility that was deduced from [7].

- R_{ext}:

R_{ext} was calculated in the following way

$$R_{ext} = 2 \times \frac{1}{1/R_{sur_ext} + 1/R_{sp_ext}} \quad (6)$$

The surface resistance of the extension R_{sur_ext} corresponds to the resistance of the extension region where the doping is maximal (x_{pext} depth, see fig. 1). The length of the extension region is assumed to be L_{sw}-L_{dp} where L_{sw} is the sidewall spacer's length and L_{dp} is the deep source/drain diffused region length. This gives:

$$R_{sur_ext} = \rho_{ext} \times \frac{(L_{sw} - L_{dp})}{X_{pext}} \quad (7)$$

X_{pext} is the depth in the junction where the doping is maximal. The spreading resistance of the extension in the x-direction by a numerical integration of the following equation:

$$R_{sp_ext} = \int_{X_{pext}}^{X_j - X_{pext} - W_{ext}} \sigma_{ext}(x) \times (L_{sw} - L_{dp}) dx \quad (8)$$

σ_{ext} is obtained from the extension concentration in the x-direction and the related mobility calculated from [7]. A vertical Gaussian profile was also assumed for the doping.

- R_{dp}:

R_{dp} was calculated using exactly the same equations than for R_{ext}, but on a length equal to L_{dp}, and with the appropriate doping, junction depth, and depletion width.

- R_{cont}:

The contact resistance was calculated from the model described in [8]. Figure 43 shows a schematic representation of the different components of the silicon/silicide contact resistance.

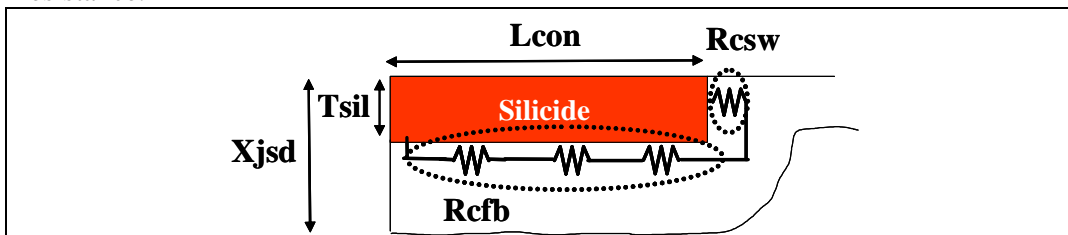


Figure 43: Schematic representation of the different components of the silicon/silicide contact resistance

The contact resistance can be divided into two components associated in parallel: a "flat-bed" component R_{cfb} calculated using a transmission line method, and a "side-wall" component, R_{csw} :

$$R_{cont} = 2 \times \frac{1}{1/R_{cfb} + 1/R_{csw}} \quad (9)$$

$$R_{cfb} = \frac{\rho_c}{L_T} \times \frac{1}{\tanh(L_{con}/L_T)} \quad (10)$$

$$R_{csw} = \frac{\rho_c}{T_{sil}} \quad (12)$$

ρ_c is the contact resistivity, L_{con} is the contact length, L_T is the contact transfer length and T_{sil} is the silicide thickness. ρ_c was obtained from [9] assuming a pure field emission conduction mechanism which is appropriate for very high doping ($>10^{20} \text{ cm}^{-3}$).

$$\rho_c = C_1 \exp\left(C_2 \frac{\phi_b}{\sqrt{N_{if}}}\right) \quad (13)$$

with $C_1=2.44 \times 10^{-9} \Omega \cdot \text{cm}^2$ (NMOS), $5.31 \times 10^{-9} \Omega \cdot \text{cm}^2$ (PMOS) and $C_2=1.29 \times 10^{-5} \text{ m}^{-3/2} \cdot \text{V}^{-1}$ (NMOS), $1.18 \times 10^{-5} \text{ m}^{-3/2} \cdot \text{V}^{-1}$ (PMOS).

N_{if} is the doping value at the interface silicon/silicide and ϕ_b is the Shottky barrier height.

L_T is given by:

$$L_T = \left(\frac{\rho_c}{R_{sq}}\right) \quad (14)$$

where R_{sq} is the sheet resistance of the silicon under the contact:

$$R_{sq} = \frac{\rho_{if}}{(X_{jdp} - W_{dp} - T_{sil})} \quad (15)$$

where ρ_{if} is the resistivity at the interface, X_{jdp} is the deep junction depth and W_{dp} is the depletion width at the bottom of the deep junction.

Finally, the total access resistance can be written as:

$$R_{acc} = R_{ov} + R_{ext} + R_{sd} + R_{cont} \quad (16)$$

Finally, the results given by the model were confronted to the results published in [4], using the same input parameters in order to validate it (figure 5). An excellent agreement is obtained for both NMOS and PMOS, demonstrating its compatibility with Kim's model

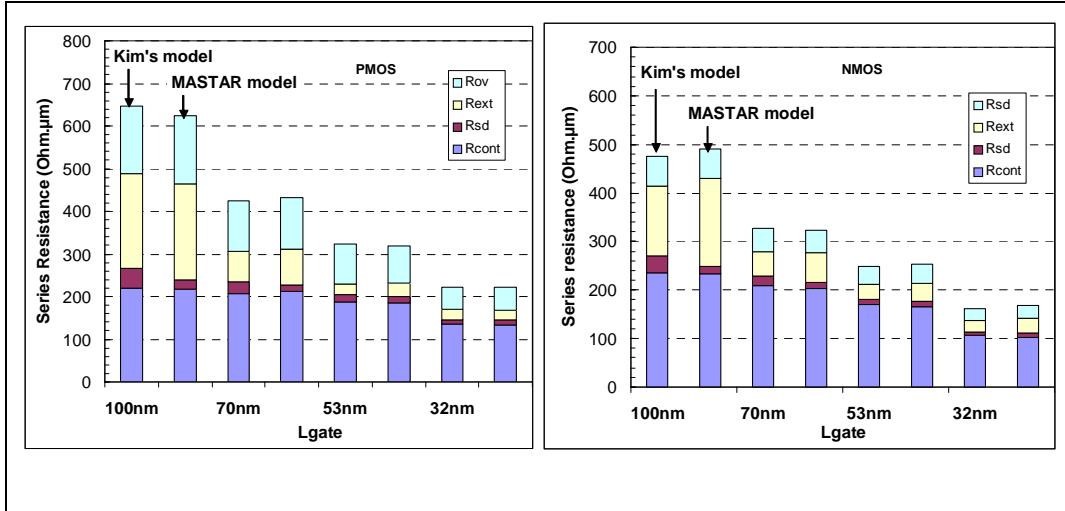


Figure 44: Comparison of the resistance calculated in [4] to the results given by the present model.

References:

[1] S.-D. Kim, C.-H.M. Park and J.C.S. Woo, IEDM Tech. Dig., 2000, pp.723-726.
 [2] S.-D. Kim, C.-H.M. Park and J.C.S. Woo, IEEE Trans. Electron Devices, vol. 49, pp. 457-466, March 2002.
 [3] S.-D. Kim, C.-H.M. Park and J.C.S. Woo, IEEE Trans. Electron Devices, vol. 49, pp. 467-472, March 2002.
 [4] S.-D. Kim and J.C.S. Woo, IWJT 2004 proceedings, pp.1-4, 2004
 [5] S.-D. Kim *et al.*, SISPAD 2004.
 [6] S. Mundanai *et al.*, IEEE Trans. Electron Devices, vol. 46, pp. 1749-1759, August 1999.
 [7] S. Reggiani *et al.*, IEEE Trans. Electron Devices, vol. 49, pp. 490-499, March 2002.
 [8] E. Dubois and G. Larrieu, Solid-State Electron., vol. 46, pp. 997-1004, 2002.
 [9] K. Varahramyan and E.J. Verret, Solid-State Electron., vol. 39, pp. 1601-1607, 1996.

Annex I: Darkspace and E₀ Calculation

In order to take into account the increase of the equivalent oxide thickness in the inversion regime as a consequence of the quantization of the carrier levels in the channel giving rise to a deserted region at the oxide interface, the so-called dark-space, the Schrödinger equation is solved in the triangular quantum well in the inversion layer using the standard Airy Model. The quantum well is defined by the effective field E_{eff} and the surface potential Ψ_s . The quantization of the energy levels $E_{i,n}$ and the corresponding wave functions $\Psi_{i,n}(x)$ are determined solving the Schrödinger equation for all valleys i .

$$\left(-\frac{\hbar^2}{2m_i} \Delta + V(x) \right) \Psi_{i,n}(x) = E_{i,n} \Psi_{i,n}(x)$$

where m_i^* is the effective mass of the valley i along the quantization direction.

Using these data, the total charge distribution in the inversion layer is evaluated using a 2D description, taking into account the 6 first energy levels:

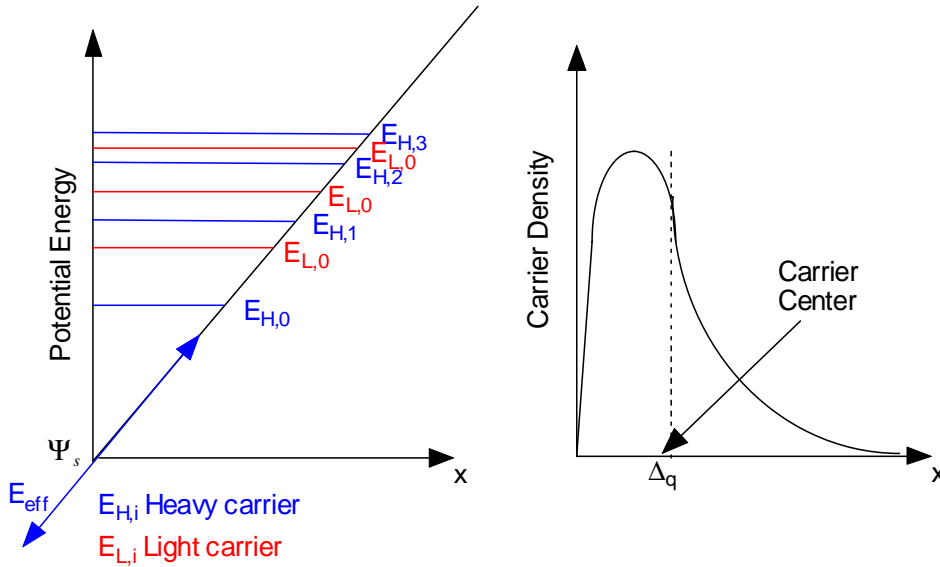
$$n_{tot}(x) = \sum_{\text{valley } i} \sum_{\text{energy } n} \left(\int_{E_{i,n}}^{\infty} D2G_i(E) \cdot f_{FD}(E) \cdot |\Psi_{i,n}(x)|^2 dE \right)$$

where $D2G_i(E)$ is the 2D density of state of the valley i , and $f_{FD}(E)$ the Fermi-Dirac distribution function. The carrier distribution maximum is shifted from the oxide interface, which induces an increase of the equivalent oxide thickness EOT. The EOT is corrected using the following approximation:

$$eot_q = eot_c + \Delta_q$$

where eot_q is the quantum EOT, eot_c is the classic EOT, and Δ_q the correction. Δ_q is the shift of the center of the carrier distribution due to the quantum effects.

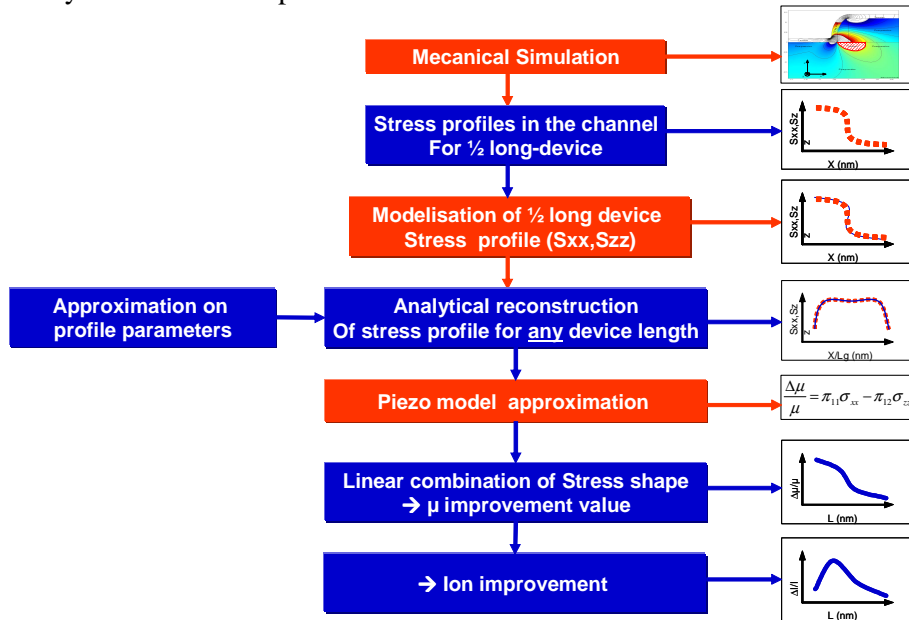
$$\Delta_q = \frac{\int_0^{\infty} n_{tot}(x) \cdot x dx}{\int_0^{\infty} n_{tot}(x) dx}$$



Annex J: Strained Liner Modelisation

In version 4 of MASTAR, the modelisation of strained-liner, such as CESL, has been re-written.

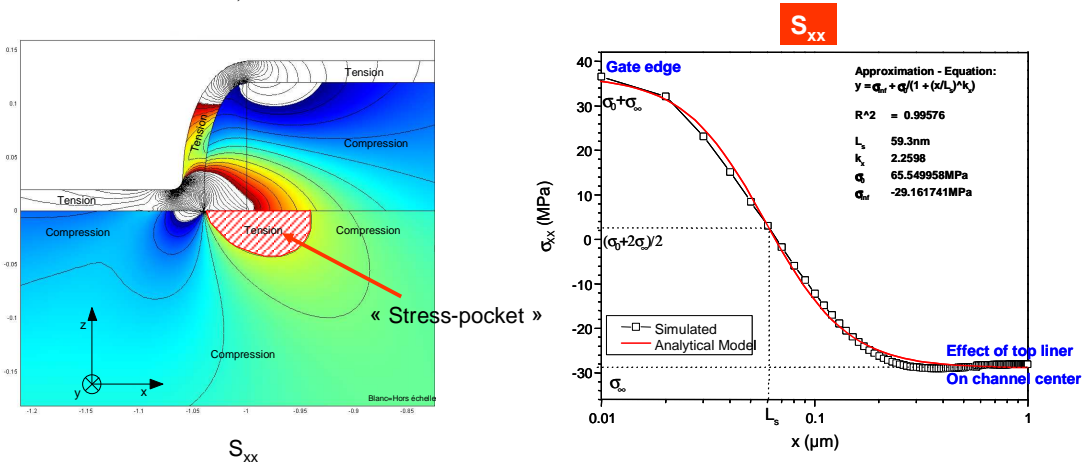
The new model is based on the analytical modeling of stress component S_{xx} and S_{zz} induced by a tensile or compressive liner.



A mathematical expression is used to fit stress component simulation data obtained for long devices. :

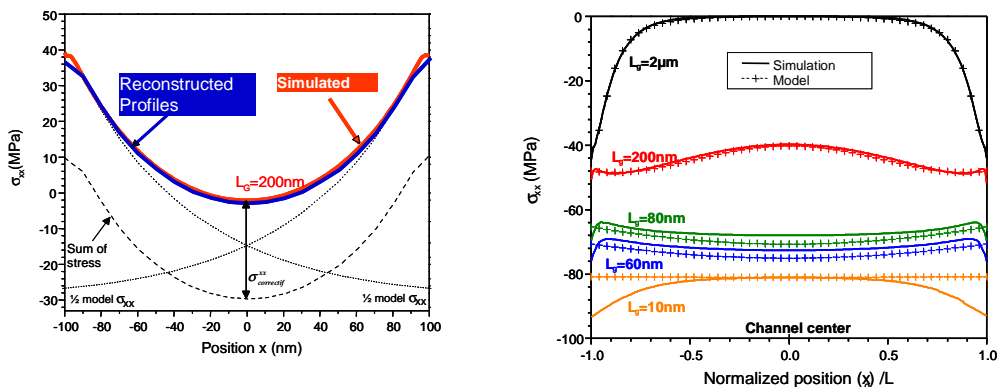
$$\sigma = \frac{\sigma_{tensile}}{\left(1 + \left(\frac{x}{L_s}\right)^k\right)} + \sigma_{\infty}$$

Where $\sigma_{tensile}$ is the stress component in the tensile zone at the gate edge, σ_{∞} is the stress component at the center of the channel, L_s the typical tensile zone length, and k represents the stress gradient between the edge and the center (mainly depends on device architecture)



We made the approximation that modules of S_{xx} and S_{zz} had the same shape, and that the same fitting coefficient could be used.

Then, stress profile is reconstructed for any device length. In order to avoid over-estimation of stress component from the top of the gate, we add a correction term. We assume once again the same function for this term. Resulting stress profile in the channel of various transistors fits with simulated profiles.

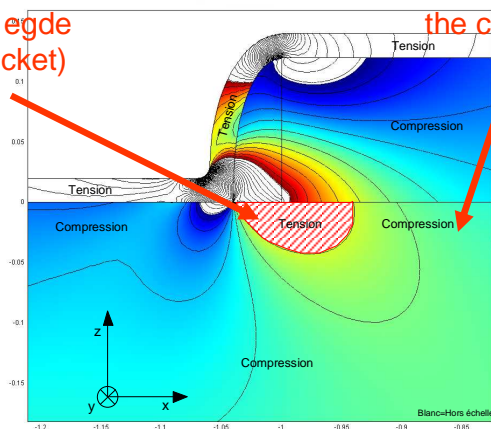


Therefore, the piezo resistivity model allows extracting an analytic model for the mobility improvement factor.

$$\frac{\mu(x, L)}{\mu_r} = \left(K_{\mu}^{poche} - 1 \right) \left[\frac{1}{1 + \left(\frac{x + \frac{L}{2}}{L_s} \right)^k} + \frac{1}{1 + \left(\frac{-x + \frac{L}{2}}{L_s} \right)^k} \right] + \left(K_{\mu}^{canal} - 1 \right) \left[1 + \frac{1}{1 + \left(\frac{L}{2L_s} \right)^k} \right] + 1$$

μ variation in the tensile zone near gate edge (stress pocket)

μ variation in the center of the channel

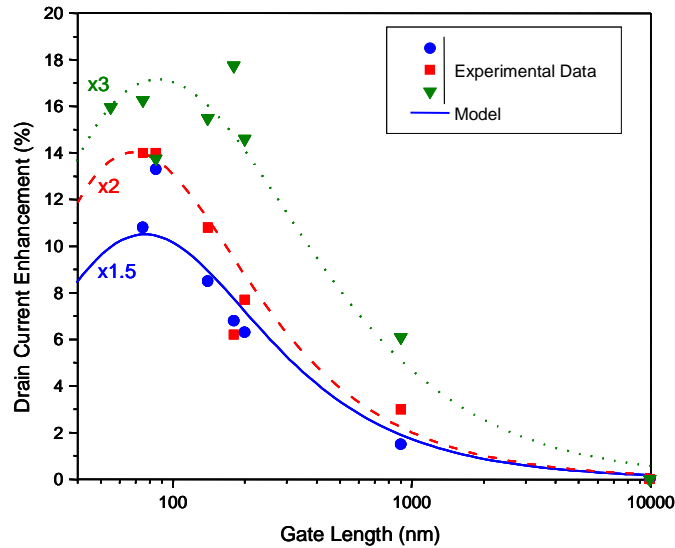


Fitting coefficient are :

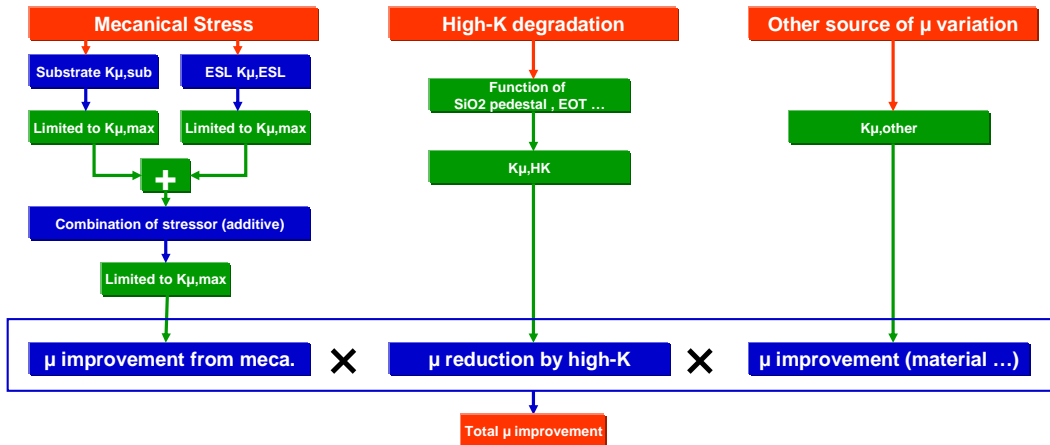
- $K_{\mu poche}$: mobility improvement in the tensile zone

- L_s : typical length of the tensile zone
- K : gradient of the tensile and compressive zones
- $K_{\mu canal}$: mobility degradation in the compressive zone

Agreement with experimental data is good.



Annex K : mobility limitation in MASTAR



Default parameter for mobility limitation are :
 1.8 for electron
 2.6 for holes

This can be modified by user in the booster tab

Acknowledgements:

The following researches have contributed to the development of the MASTAR program (initiated by Thomas Skotnicki, STMicroelectronics)

Thomas Skotnicki	STMicroelectronics Crolles
Frédéric Boeuf	STMicroelectronics Crolles
Markus Müller	Philips Semiconductors Crolles
Arnaud Pouydebasque	Philips Semiconductors Crolles
Claire Fenouillet-Béranger	CEA-LETI
Robin Cerutti	STMicroelectronics Crolles
Samuel Harrison	L2MP, Université de Provence, Marseille
Stéphane Monfray	STMicroelectronics Crolles
Benjamin Dumont	STMicroelectronics Crolles
Fabrice Payet	STMicroelectronics Crolles
Programming : Laurent Gayet	Dolphin