

Modeling and Simulation ITWG

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ITWG/TWG Members

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*: supported by EC User Group SUGERT

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Japanese TWG 11 industrial members

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+ 4 further TWG members

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K. Lee, Samsung

Y.T. Chia, TSMC

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2005/ 2006 Modeling & Simulation SCOPE & SCALES

Equipment related

- Equipment/Feature scale Modeling
- Lithography Modeling

IC-scale

- Circuit Elements Modeling
- Package Simulation

Feature scale

- Front End Process Modeling
- Device Modeling
- Interconnects and Integrated Passives Modeling

- Materials Modeling
- Numerical Methods
- **DFM / DFY** (new 2005)

Modeling Overall Goal

- Support technology development and optimization
- Reduce development times and costs



Key Messages (I)

- Mission of Modeling and Simulation as cross-cut topic:
Support areas covered by other (especially focus) ITWGs
 - ⇒ In-depth analysis of M&S needs of other ITWGs performed, based on documents + inter-ITWG discussions
 - ⇒ Strong links with ALL ITWGs – see also specific texts in 2005
- Modeling and simulation provides an ‘embodiment of knowledge and understanding’. It is a tool for technology/device development and optimization and also for training/education
- Technology modeling and simulation is one of a few enabling methodologies that can reduce development times and costs: Cost reduction assessed 2005 up to 35% (*when simulation is used efficiently*)
 - ⇒ important not only in years of difficult economic conditions



Key Messages (II)

- Art of modeling:
 - Combine dedicated experiments & theory to extract physical mechanisms & parameters
 - Find appropriate trade-off between detailed physical simulation (CPU and memory costly) and simplified but physically appropriate approaches
- Accurate experimental characterization methods are essential
- Reliable experimental reference data required on all levels – profiles, electrical data, – must partly be provided e.g. by device makers!
- Further growing importance of atomistic/materials/hierarchical/multilevel simulation - appropriate treatment of nanostructures

Invitation for extended participation esp. from Korea, Taiwan and USA
- also include suppliers (equipment and software)



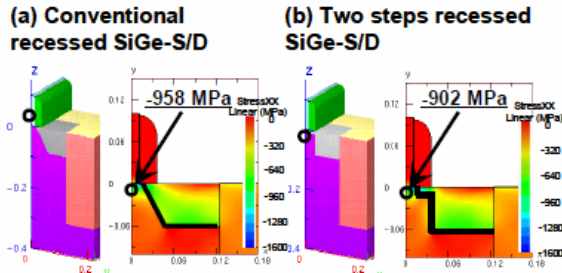
Basic Approach and Focus of 2005/2006 Work

- 1) Detailed cross-cuts worked out in 2003 – regularly updated together with other ITWGs
- 2) 2005 rewrite of text, based on 2004/2005 changes of cross-cuts and tables, and state-of-the-art
 - Involve subchapter editing teams which should consist of representatives from each region (achieved: 3 to 5 regions involved)
- 3) Main 2005 change in chapter structure:
 - Add new subchapter on TCAD for Design, Manufacturing and Yield:
 - Development & use of simulation to assess impact of process variations on device and circuits performance, manufacturing, yield, ...
- 4) 2006 emphasis on
 - revision of M&S tables incl. cost reduction estimate
 - preparation for 2007 w.r.t. Korean, Taiwanese and US TWG
 - preparation of support to other ITWGs by simulation assessment

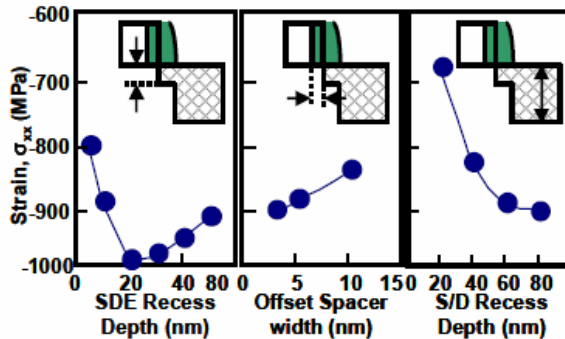


Example for Success Cases

Improvement of PMOS performance with two-step recessed SiGe-S/D (Toshiba – ESSDERC 2006)



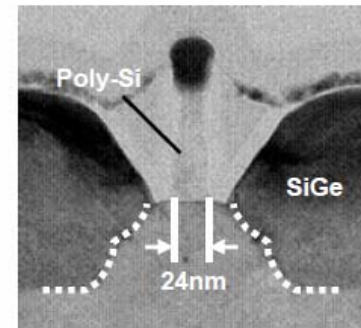
3D stress simulation



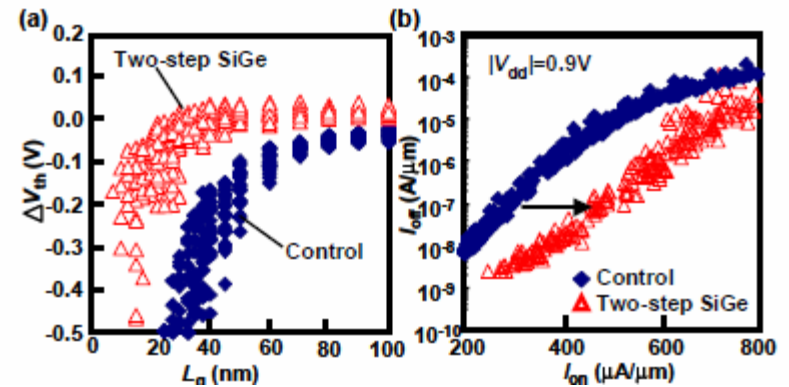
Dependence of channel strain on pMOSFET structure

A High Performance pMOSFET with Two-step Recessed SiGe-S/D Structure for 32nm node and Beyond

N. Yasutake, T. Ishida, K. Ohuchi, N. Aoki, N. Kusunoki, ¹S. Mori, ¹I. Mizushima, T. Morooka, ¹K. Yahashi, S. Kawanaka, K. Ishimaru and H. Ishiuchi



Cross-sectional TEM of optimized two-step recessed SiGe-S/D pMOSFET



Improvement of pMOS performance with two-step recessed SiGe-S/D: V_{th} roll-off ($\Delta V_{th} = V_{th} - V_{th}@L_g = 300 \text{ nm}$); $I_{on} - I_{off}$ characteristics ($|V_{dd}| = 0.9 \text{ V}$)



Example for Success Cases

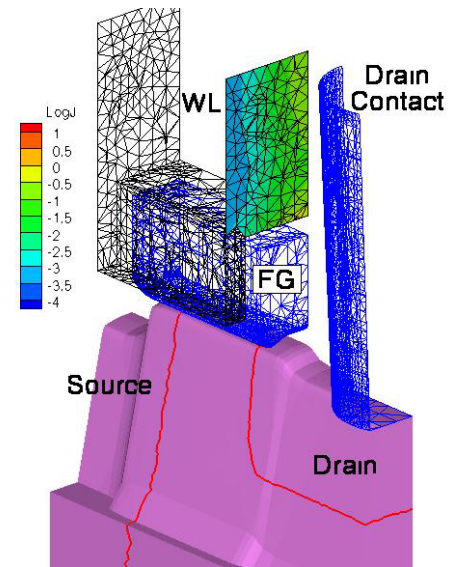
NOR Flash Reliability: Contact-Gate Leakage

Requirements met during simulation:

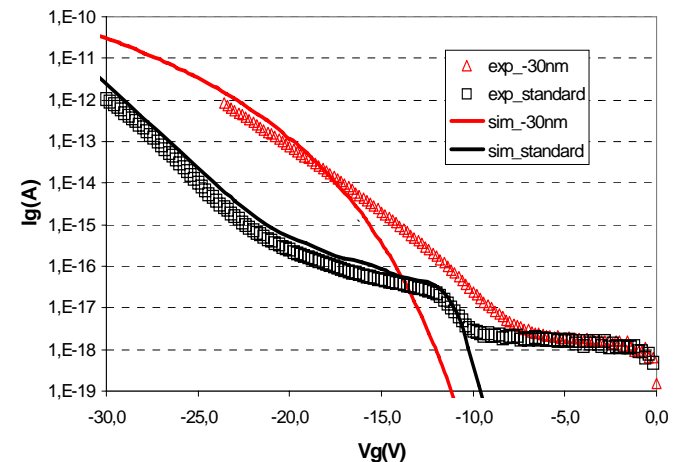
- Accurate 3D description of memory cell morphology
- Leakage through non-planar multi-layer dielectric stack
- 3D non-local tunneling model to account for local curvature radii
- Floating Gate charging during measurement

Main results:

- Sound interpretation of physical mechanisms involved
- Lateral trap-assisted conduction dominates for aggressively scaled contact-gate distance
- Guidelines for reliable scaling of NOR cell



Source: STMicroelectronics Agrate (accepted for IRPS 2007)

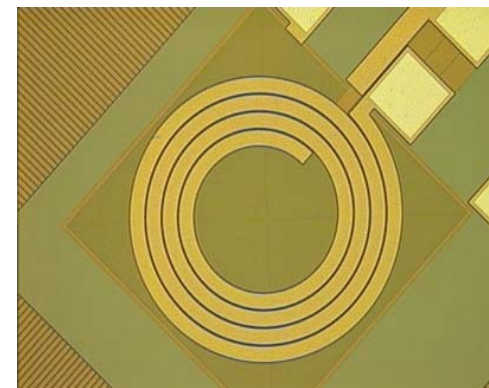
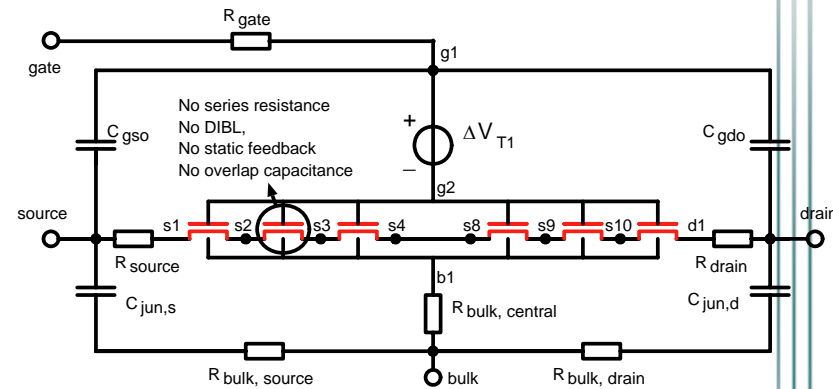


2006 Short-term Difficult Challenges under Review

High-Frequency Device and Circuit Modeling for 5-100 Ghz Applications

Needs

- Efficient extraction and simulation of full-chip interconnect delay and power consumption
- Accurate and yet efficient 3D interconnect models, especially for transmission lines and S-parameters
- Extension of physical device models to III/V materials
- High-frequency circuit models including non-quasi-static effects, substrate noise, 1/f noise and parasitic coupling
- Parameter extraction assisted by numerical electrical simulation instead of RF measurement
- Scalable active and passive component models for compact circuit simulation
- Co-design between interconnects and packaging



(From Philips)

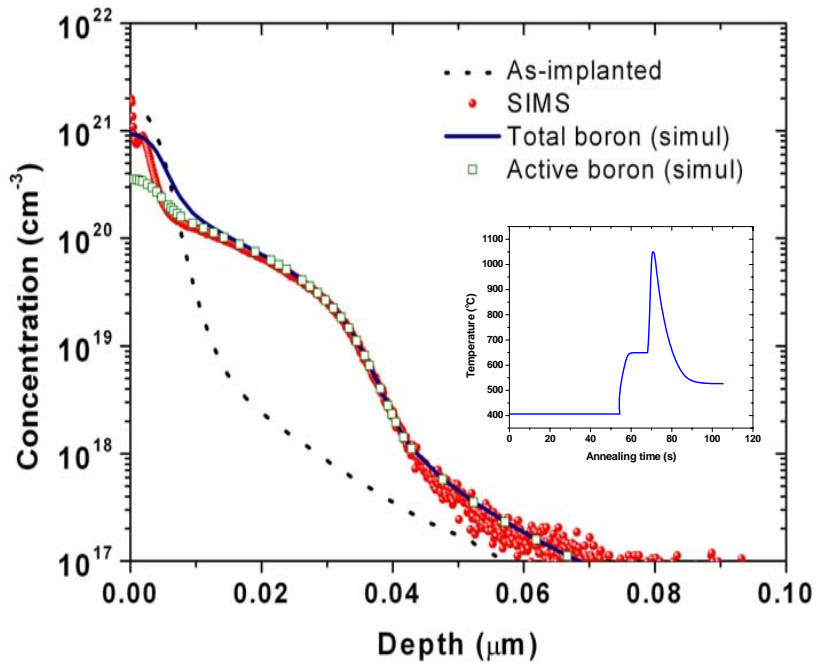


2006 Short-Term Difficult Challenges under Review

Front-End Process Modeling for Nanometer Structures

Needs

- Diffusion/activation/damage/stress models and parameters incl. SPER and low thermal budget processes in Si-based substrate, e.g. Si, SiGe:C, Ge, SOI, epilayers and ultra-thin body devices
- Modeling of epitaxially grown layers: Shape, morphology, stress
- Characterization tools/methodologies for these ultra-shallow geometries/ junctions and low dopant levels
- Modeling hierarchy from atomistic to continuum for dopants and defects in bulk and at interfaces
- Front-end processing impact on reliability



Source: P. Pichler et al., Proc. IEDM 2004

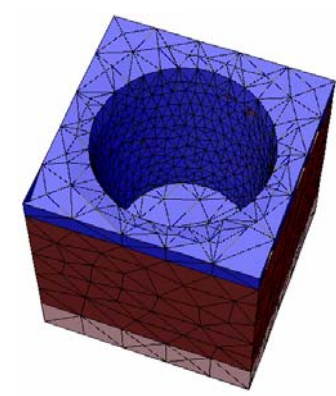


2006 Short-Term Difficult Challenges under Review

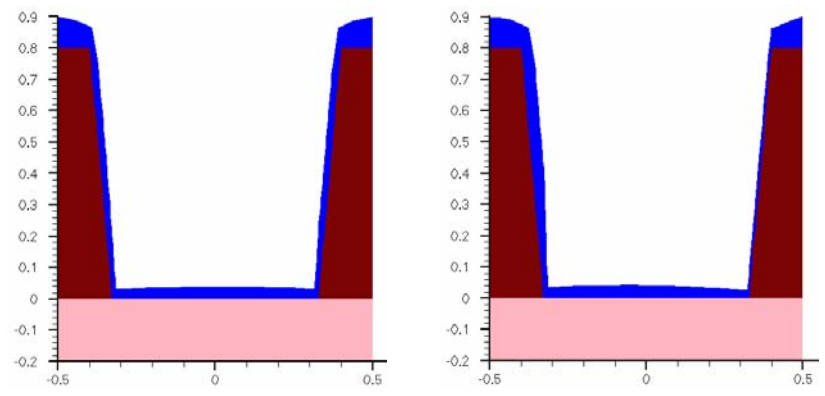
Integrated Modeling of Equipment, Materials,

Needs Feature Scale Processes and Influences on Devices

- Fundamental physical data (e.g. rate constants, cross sections, surface chemistry for ULK, photoresists and high-k metal gate); reaction mechanisms and simplified but physical models for complex chemistry and plasma reaction
- Linked equipment/feature scale models (including high-k metal gate integration, damage prediction)
- CMP, etch, electrochemical polishing (ECP) (full wafer and chip level, pattern dependent effects)
- MOCVD, PECVD and ALD, electroplating and electroless deposition modeling
- Multi-generation equipment/wafer models



Simulated across-wafer variation of feature profile for a sputter-deposited barrier.



(From Fraunhofer IISB)



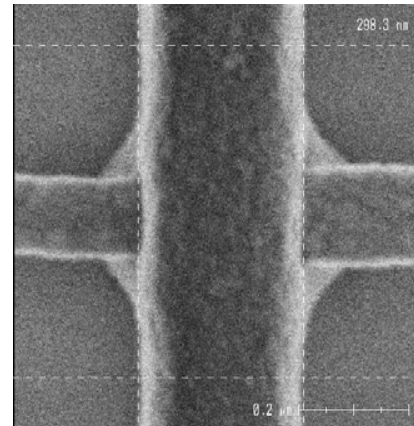
2006 Short-Term Difficult Challenges under Review

Lithography Simulation including NGL

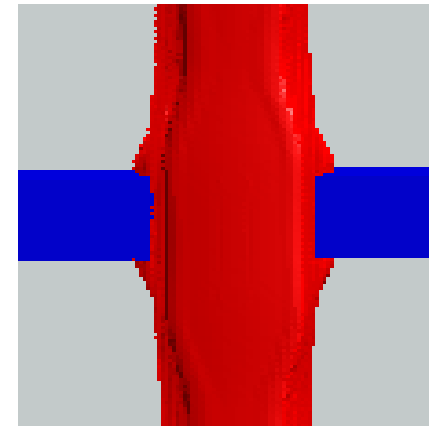
Needs

- Optical simulation of resolution enhancement techniques including mask optimization (OPC, PSM)
- Predictive resist models (e.g. mesoscale models) incl. line-edge roughness, etch resistance, adhesion, and mechanical stability
- Methods to easily calibrate resist model kinetic and transport parameters
- Models that bridge requirements of OPC (speed) and process development (predictive) including EMF effects
- Experimental verification and simulation of ultra-high NA vector models, including polarization effects from the mask and the imaging system
- Models and experimental verification of non-optical immersion lithography effects (e.g. topography and change of refractive index distribution)
- Simulation of multiple exposure/patterning
- Multi-generation lithography system models
- Simulation of defect influences / defect printing
- Modeling lifetime effects of equipment and masks

Example: Footing effect in vicinity of shadowed region at bottom of poly-Si line



Top-down wafer SEM
(from T. Sato, Toshiba)



3D simulation (from A. Erdmann, FhG-IISB)

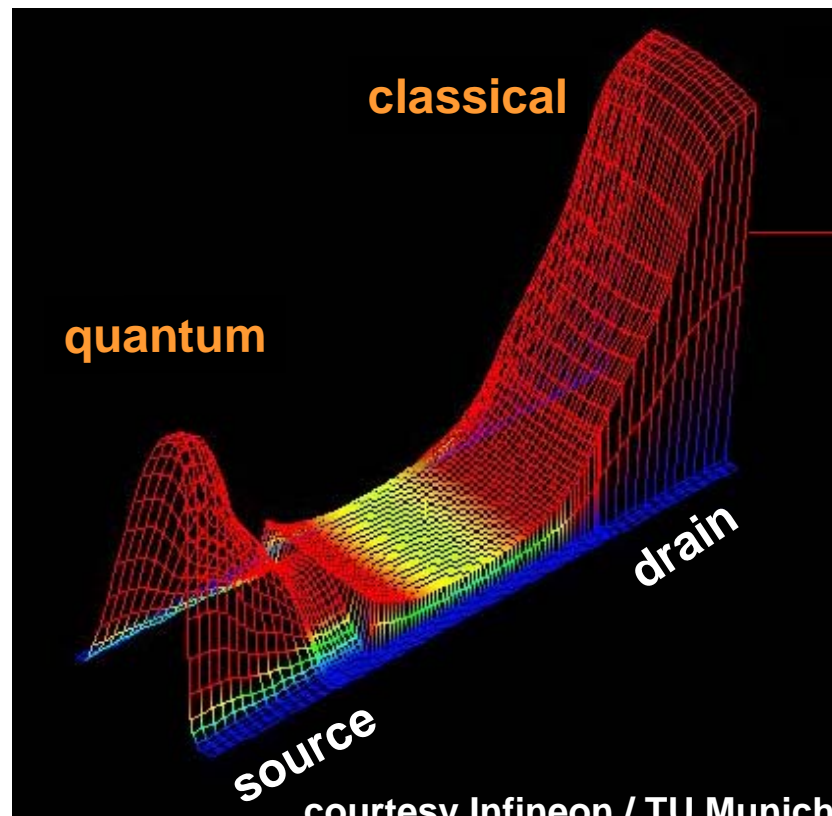


2006 Short-Term Difficult Challenges under Review

Ultimate Nanoscale Device Simulation Capability

Needs

- Methods, models and algorithms that contribute to prediction of CMOS limits
- General, accurate and computationally efficient quantum based simulators
- Models and analysis to enable design and evaluation of devices and architectures beyond traditional planar CMOS
- Models and analysis to investigate new memory devices like MRAM, PRAM, etc
- Gate stack models for ultra-thin dielectrics
- Models for device impact of statistical fluctuations in structures and dopant distributions
- Material models for stress engineering.
- Reliability modeling for ultimate CMOS
- Physical models for stress induced device performance

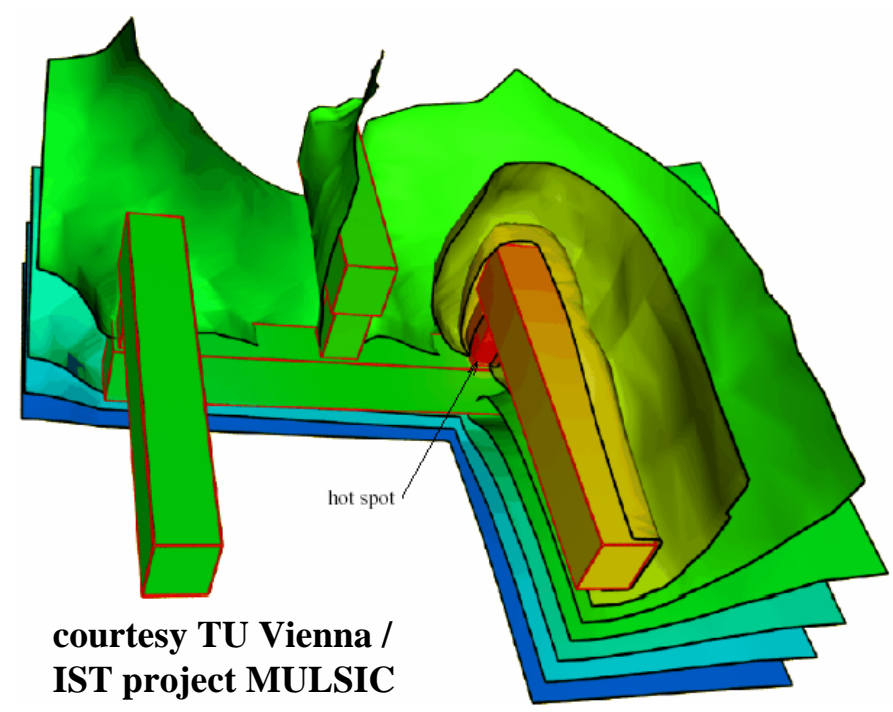


Quantum-mechanical vs. classical carrier density in double-gate transistor

2006 Short-Term Difficult Challenges under Review **Thermal-Mechanical-Electrical Modeling for Interconnects and Packaging**

Needs

- Model thermal-mechanical, thermo-dynamic and electronic properties of low-k, high-k and conductors for efficient in-chip package layout and power management, and the impact of processing on these properties especially for interfaces and films under 1 micron
- Model reliability of packages and interconnects [incl. 3D integration](#) (e.g. stress voiding, electromigration, piezoelectric effects; textures, fracture, adhesion)
- Models for electron transport in ultra fine patterned conductors



Temperature distribution in
an interconnect structure



2006 Difficult Challenges < 32 nm

Table 122 Modeling and Simulation Difficult Challenges *UPDATED (continued)*

<i>Difficult Challenges < 32 nm</i>	<i>Summary of Issues</i>
Modeling of chemical, thermomechanical, and electrical properties of new materials	Computational materials science tools to describe materials properties, process options, and operating behavior for new materials applied in devices and interconnects, including especially for the following: Gate stacks, predictive modeling of dielectric constant, bulk polarization charge, surface states, phase change, thermomechanical (including stress effects on mobility), optical properties, reliability, breakdown, and leakage currents including band structure, tunneling from process/materials and structure conditions. Models for air gap and novel integrations in 3D interconnects including data for ultrathin material properties. Linkage with first principle computation and reduced model (classical MD or thermodynamic computation). Accumulation of databases for semi-empirical computation. Models for new ULK materials that are also able to predict process impact on their inherent properties.
Prediction of dispersion of circuit parameters	Computer-efficient inclusion of influences of statistics (including correlations) before process freeze, quantum/ballistic transport, etc., into compact modeling Efficient extraction of circuit-level variations from process and device simulation
IS	Nano-scale modeling Process modeling tools for the development of novel nanostructure devices (nanowires, carbon nanotubes (including doping), quantum dots, molecular electronics) Device modeling tools for analysis of nanoscale device operation (quantum transport, resonant tunneling, spintronics, contact effects - non charge-state devices)
IS	Optoelectronics modeling Materials and process models for optoelectronic elements (transmitters and receivers, optical couplers). Coupling between electrical and optical systems, optical interconnect models, semiconductor laser modeling. Physical design tools for integrated electrical/optical systems



Requirement Tables: 2005 Status & 2006 Changes

General:

- Considerable revision in 2005
- Several details changed in 2006
- Special attention to accuracy requirements – incl. cost reduction estimate
- Table continues to contain some items in “zebra” colour - according to ITRS guidelines:

“Limitations of available solutions will not delay the start of production. In some cases, work-arounds will be initially employed. Subsequent improvement is expected to close any gaps for production performance in areas such as process control, yield, and productivity.”

⇒ This means for simulation: It can be used, but with more calibration, larger CPU time/memory, less generality than in the end required ...



*For 2005/2006, interim solutions are known but research is still needed towards mature commercial solutions.

Year of Production	2005	2006	2007	2008	2009	2010	2011	2012	2013
DRAM ½ Pitch (nm) (contacted)	80	70	65	57	50	45	40	36	32
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	90	78	68	59	52	45	40	36	32
MPU Physical Gate Length (nm)	32	28	25	22	20	18	16	14	13

Lithography

WAS	Exposure	Simulation of immersion lithography including physical mask parameters, mask birefringence and mask polarization effects	Simulation of EUV, EPL, ML2, imprint lithography options, models bridging OPC and predictive feature scale simulation		NGL models and modeling of materials and components (immersion, EUV, EPL, ML2 lithographic processes, imprint)	
IS	Exposure	Simulation of immersion lithography including physical mask parameters, mask birefringence and mask polarization effects [1]	Simulation of immersion lithography for high NA liquids (NA about 1.5) [2]	Simulation of EUV, EPL, very high NA (about 1.7), ML2, imprint lithography options, models bridging OPC and predictive feature scale simulation [3]	NGL models and modeling of materials and components (immersion, EUV, EPL, ML2 lithographic processes, imprint)	
WAS	Resist models	Detailed chemically amplified resist and EUV resist models including LER and immersion (liquid-solid interface), and methods to easily calibrate parameters; coupling with etch models		Finite polymer-size effects	Meso-scale resist models with finite molecule effects	Non-conventional photoresist models and coupling with etch models
IS	Resist models	Detailed chemically amplified resist and EUV resist models including LER and immersion (liquid-solid interface), and methods to easily calibrate parameters; coupling with etch models		Multiple exposure; finite polymer-size effects; line collapsing; lithography on topography	Meso-scale resist models with finite molecule effects; resist flare	Non-conventional photoresist models and coupling with etch models
	Full-chip lithography simulation	Simulation of lithography across whole chip to detect weak spots	Simulation of lithography and etching across whole exposure field to detect weak spots			

Front End Process Modeling

WAS	Gate stack*	♦ High-k dielectrics and gate materials (interfaces, impurity diffusion, electrical barrier) [4]	Model material properties and electrical behavior of prioritized alternative dielectrics and gates (interfaces, defects, impurities, mobility, leakage) [5]		Modeling of new process steps / processing and properties of alternative materials
IS	Gate stack*	♦ High-k dielectrics and gate materials (interfaces, impurity diffusion, electrical barrier) [4]	Model material properties and electrical behavior of prioritized alternative dielectrics and gates (interfaces, defects, impurities, mobility, leakage - incl. metal gates and FUSI) [5]		Modeling of new process steps / processing and properties of alternative materials

2006 Short-Term Requirements



2006 Short-Term Requirements

*For 2005/2006, interim solutions are known but research is still needed towards mature commercial solutions.

Year of Production	2005	2006	2007	2008	2009	2010	2011	2012	2013
DRAM ½ Pitch (nm) (contacted)	80	70	65	57	50	45	40	36	32
WAS	Diffusion and activation models	Interface influences and activation for ultra-shallow junction formation		Enhancements of models for Si, extension for Si based materials incl. stress/strain and new annealing steps (e.g. flash/laser anneals, SPER). Atomistic modeling to complement experiments and continuum models.					
IS	Diffusion and activation models	Interface influences and activation for ultra-shallow junction formation		Enhancements of models for Si, extension for Si based materials incl. stress/strain and new annealing steps (e.g. flash/laser anneals, SPER)			Atomistic modeling to complement experiments and continuum models.		
<i>Topography and Material Modeling [6]</i>									
WAS	Deposition	Integration between feature scale and equipment simulations		Electrical properties and stress incl. microstructure; layout dependence; prediction of liquid dispense (resist, spin-on ULK) on planarity and gate pattern; coupling with etching, lithography and CMP models		Adhesion and reliability, including microstructure; full molecular dynamics (or atomistic) feature scale models, prediction of surface properties			
IS	Deposition	Integration between feature scale and equipment simulations		Electrical properties and stress incl. microstructure; layout dependence			Prediction of microstructure and surface properties		
WAS	Planarization *	Comprehensive 3D physical CMP models		Chip-level including dummy placement optimization, padwear and conditioning disc modeling, physics based optimization of rates, uniformity, and defect reduction		CMP process for circuit design including process variations			
IS	Planarization *	Comprehensive Physical CMP models incl. dummy placement optimization		Chip-level including dummy placement optimization, padwear and conditioning disc modeling, physics based optimization of rates, uniformity, and defect reduction		Simulation of defect reduction incl. padwear and condition disc modeling			
WAS	Etching	(Surface) physics based feature scale models (incl. redeposition)	Integration of feature-scale simulation with equipment (plasma) models; process integration (coupling of etch-deposition-plating-CMP-lithography- including data beyond topography to also include sub-surface material property prediction), full molecular dynamics (or atomistic) feature scale models						
IS	Etching	(Surface) physics based feature scale models (incl. redeposition)	Integration of feature-scale simulation with equipment (plasma) models; process integration (coupling of etch-deposition-plating-CMP-lithography) including data beyond topography to also include sub-surface material property prediction; full molecular dynamics (or atomistic) feature scale models				Including data beyond topography to also include sub-surface material property prediction), full molecular dynamics (or atomistic) feature scale models		



2006 Short-Term Requirements

Year of Production		2005	2006	2007	2008	2009	2010	2011	2012	2013
DRAM ½ Pitch (nm) (contacted)		80	70	65	57	50	45	40	36	32
WAS	Alternative material modeling				Calculation of thermal (thermodynamic), mechanical and electronic properties; process impact on intrinsic material behavior, integrity and electrical performance under strain					
IS	Alternative material modeling				Calculation of thermodynamic and electronic properties	Calculation of thermal (thermodynamic), mechanical and electronic properties; process impact on intrinsic material behavior, integrity and electrical performance under strain				
	Equipment impact on process results including material properties				-	Computer engineered materials and process recipes; predictive manufacturability and yield; full process integration models. Integrated equipment/feature scale modeling extended to include material information from the atomic scale				
<i>Numerical Device Modeling [7]</i>										
WAS	Transport modeling [8].	Mobility models incl. stress, surface roughness effects of nitrided oxides and orientation of the channel		Mobility models for high-k materials	Efficient inclusion of quasi-ballistic transport					
IS	Transport modeling [8]	Mobility models incl. stress, surface roughness effects of nitrided oxides and orientation of the channel		Mobility models for high-k materials; efficient inclusion of quasi-ballistic transport	QM confinement in thin films (esp. SOI)					
WAS	Additional requirements for non-classical CMOS	Device models to include additional interfaces (esp. with respect to mobility in thin films)		Efficient quantum-mechanical simulation of 3D device structures, including thin films, consistent with mobility models	Nanoscale simulation capability including accurate atomistic and quantum effects					
IS	Additional requirements for non-classical CMOS	Device models to include additional interfaces (esp. with respect to mobility in thin films)		Efficient quantum-mechanical simulation of 3D device structures, including thin films, consistent with mobility models	Nanoscale simulation capability including accurate atomistic and quantum effects; QM confinement in nanowires etc					
WAS	Novel memory devices	Material properties and device modeling of MRAMs, PCMs, FeRAMs and SONOS/NROMs								
IS	Novel memory devices *	♦ Unit-cell performance modeling of MRAMs, PCMs, FeRAMs and SONOS/NROMs			Material properties and reliability modeling of novel memory devices					
WAS	RF modeling *	♦ Physical device models for HF noise and mobility in III/Vs								
IS	RF and noise modeling *	♦ Physical device models for HF noise and mobility in III/Vs								
<i>Circuit Component Modeling [9]</i>										
WAS	Active devices*	♦ Non-classical CMOS compact models / non-quasi-static models and series resistance		Circuit models for non-classical CMOS devices including reliability and influences of statistics	Include ballistic effects			Circuit models for nanoscale devices and interconnects		
IS	Active devices*	♦ Non-classical CMOS compact models / non-quasi-static models and series resistance		Circuit models for non-classical CMOS devices including reliability and influences of statistics	Include quasi-ballistic effects and non-stationary transport			Circuit models for nanoscale devices and interconnects		



2006 Short-Term Requirements

Year of Production		2005	2006	2007	2008	2009	2010	2011	2012	2013
DRAM ½ Pitch (nm) (contacted)		80	70	65	57	50	45	40	36	32
WAS	Interconnects and integrated passives	Hierarchical full chip RLC [10]		Hierarchical process-aware full-chip RLC		Include self-heating and reliability			Mixed electrical/optical simulation	
IS	Interconnects and integrated passives	Hierarchical full chip RLC [10]		Hierarchical process-aware full-chip RLC		Include self-heating and reliability			Mixed electrical/optical simulation	
Process and materials impact on electrical performance of interconnects *		◆ Models that relate material properties (process related or fundamental) to electron transport (e.g. in conducting lines). Includes models for electron scattering. Models that predict paths to material property repair (e.g. low-κ repair, capacitance repair)								
Package Modeling										
WAS	Electrical modeling*	◆ Unified RLC extraction for package/chips	Reduced order models		Full-wave analysis		Mixed electrical/optical analysis			
IS	Electrical modeling*	◆ Unified RLC extraction and multiscale modeling for package / chips		Reduced order models		Full-wave analysis		Mixed electrical/optical analysis		
WAS	Thermal-mechanical modeling *	◆ Thermo-mechanical-integrated models	Include non-bulk and porous materials properties		Include reliability (esp. life prediction)					
IS	Thermal-mechanical modeling *	◆ Thermo-mechanical-integrated models	◆ Include non-bulk and porous/air gap materials properties		Include reliability (esp. life prediction)					
WAS	Material properties *	◆ Improved material models (visco-elasticity, creep, plasticity), interfaces	Full die simulation							
IS	Material properties *	◆ Improved material models (visco-elasticity, creep, plasticity), interfaces	Full die simulation							
Numerical analysis										
WAS	Meshing *	◆ Robust, reliable grid generation including moving boundaries								
IS	Meshing *	◆ Robust, reliable 3D grid generation including moving boundaries								
Algorithms		More robust and more parallelizable algorithms			Discretization schemes alternative e.g. to box methods		Efficient atomistic/quantum methods; ab-initio or molecular dynamics based topography simulations			



More details given in tables & ITRS text

Thank you

