

# 2006 Lithography Update

Michael Lercel

And the rest of the Litho TWG's



# Lithography ITWG key contributors for 2006

- Japan
  - Hanyu, Kameyama, Hayashi, Yamaguchi, Mori, Higashikawa
- Europe
  - M. Vasconi, Y. Rody
- Korea
  - H. Cho
- Taiwan
  - B. Lin, Y.C. Ku
- USA
  - Michael Lercel (chair), Gene Fuller (co-chair)

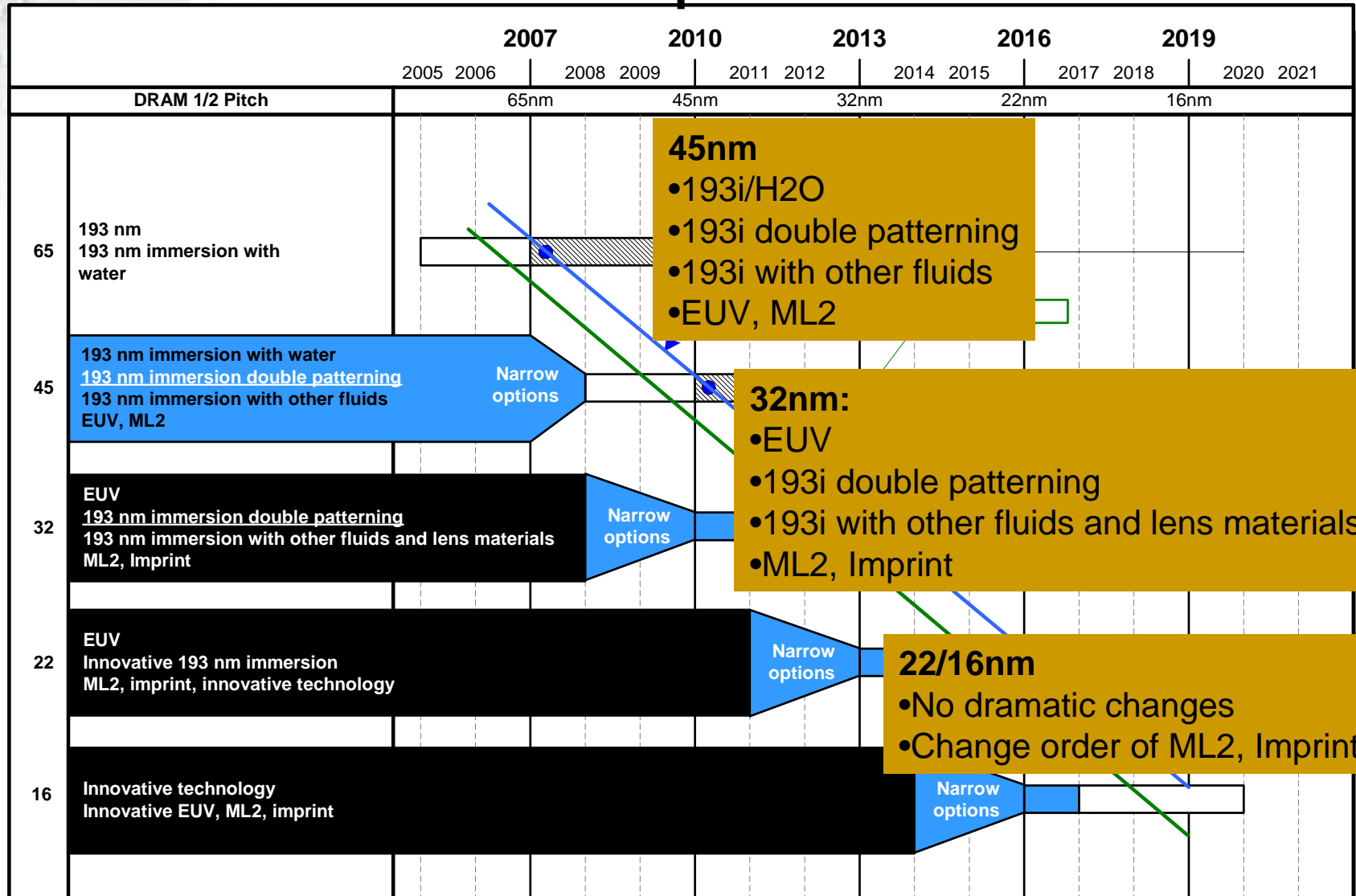


# 2006 Major Updates

- Updates to Potential Solutions Table
  - Clarification on Immersion Lithography Options
  - Double exposure 193nm
- Difficult Challenges
  - Add items for double exposure
- Mask tables updated
  - Added information for double exposure
  - Color changes based on industry improvements
- Maskless litho table added
  - Data volume and grid size requirements



# Potential Solutions 2006 Update



**45nm**

- 193i/H2O
- 193i double patterning
- 193i with other fluids
- EUV, ML2

**32nm:**

- EUV
- 193i double patterning
- 193i with other fluids and lens materials
- ML2, Imprint

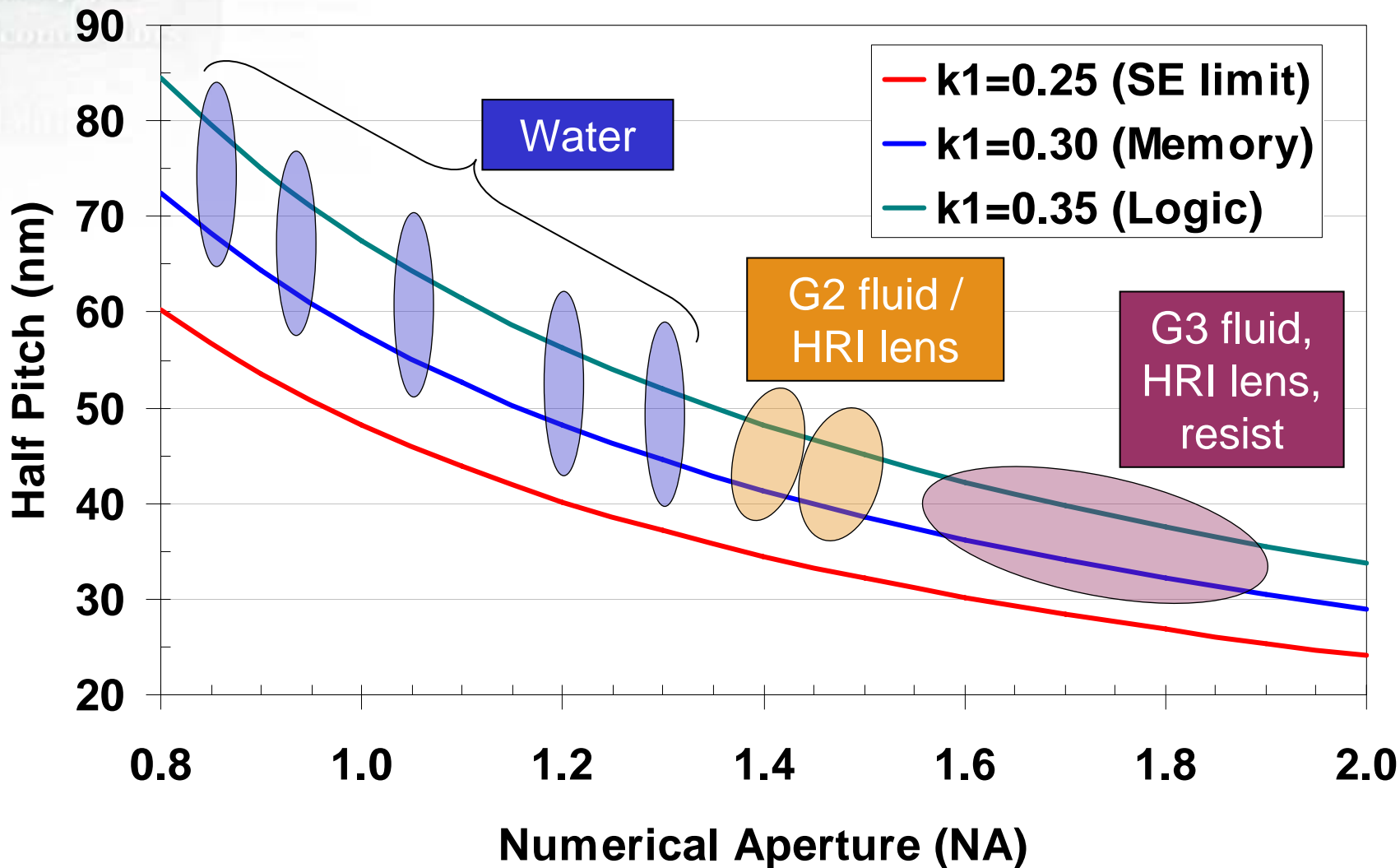
**22/16nm**

- No dramatic changes
- Change order of ML2, Imprint

Research Required
  Development Underway
  Qualification/Pre-Production
  Continuous Improvement

This legend indicates the time during which research, development, and qualification/pre-production should be taking place for the solution.

# 193 nm Immersion Generations



$$HP = k_1 \frac{\lambda}{NA} \quad (\lambda = 193 \text{ nm})$$



# 2006 ITRS Lithography Requirements

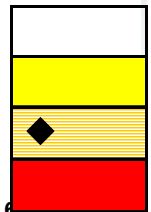
Year of Production	2006	2007	2010	2013	2016	2019
DRAM 1/2 pitch (nm) (contacted)	70	65	45	32	22	16
DRAM 1/2 pitch (nm)	<b>70</b>	<b>65</b>	<b>45</b>	<b>32</b>	<b>22</b>	<b>16</b>
Flash 1/2 pitch (nm) (un-contacted poly)	<b>64</b>	<b>57</b>	<b>40</b>	<b>28</b>	<b>20</b>	<b>14</b>
Contact in resist (nm)	<b>79</b>	<b>70</b>	<b>50</b>	<b>35</b>	<b>25</b>	<b>18</b>
Contact after etch (nm)	<b>72</b>	<b>64</b>	<b>45</b>	<b>32</b>	<b>23</b>	<b>16</b>
Overlay [A] (3 sigma) (nm)	<b>13</b>	<b>11</b>	<b>8</b>	<b>5.7</b>	<b>4</b>	<b>2.8</b>
CD control (3 sigma) (nm) [B]	<b>7.4</b>	<b>6.6</b>	<b>4.7</b>	<b>3.3</b>	<b>2.3</b>	<b>1.7</b>
MPU gate in resist (nm)	<b>48</b>	<b>42</b>	<b>30</b>	<b>21</b>	<b>15</b>	<b>11</b>
Contact in resist (nm)	<b>97</b>	<b>84</b>	<b>56</b>	<b>39</b>	<b>28</b>	<b>20</b>
Contact after etch (nm)	<b>88</b>	<b>77</b>	<b>51</b>	<b>36</b>	<b>25</b>	<b>18</b>
Gate CD control (3 sigma) (nm) [B] **	<b>2.9</b>	<b>2.6</b>	<b>1.9</b>	<b>1.3</b>	<b>0.9</b>	<b>0.7</b>
Mask CD uniformity (nm, 3 sigma) isolated lines (MPU gates), binary or attenuated phase shift mask [H] *	<b>3.4</b>	<b>2.6</b>	<b>1.3</b>	<b>1</b>	<b>0.7</b>	<b>0.5</b>
Mask Image placement (nm, multipoint) [F]	<b>8</b>	<b>7</b>	<b>4.8</b>	<b>3.4</b>	<b>2.2</b>	<b>1.5</b>
Mask Image placement (nm, multipoint) for double patterning	<b>5.7</b>	<b>4.9</b>	<b>3.4</b>	<b>2.4</b>	<b>1.6</b>	<b>1.1</b>
Low frequency line width roughness: (nm, 3 sigma) <8% of CD *****	<b>3.8</b>	<b>3.4</b>	<b>2.4</b>	<b>1.7</b>	<b>1.2</b>	<b>0.8</b>

Manufacturable solutions exist, and are being optimized

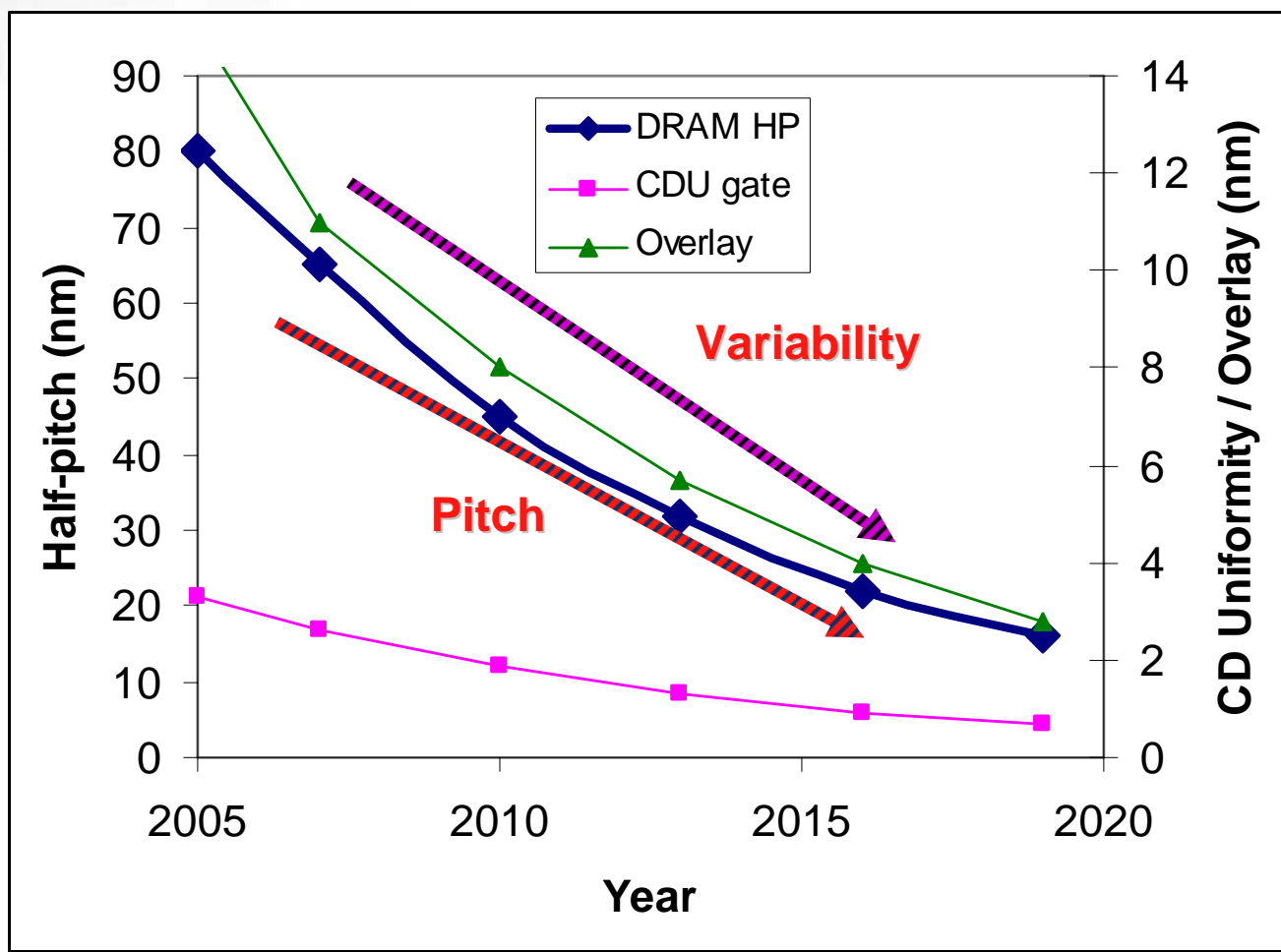
Manufacturable solutions are known

Interim solutions are known

Manufacturable solutions are NOT known



# Lithography Roadmap



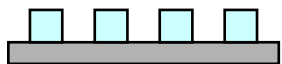
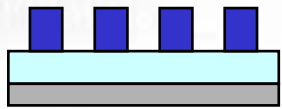
**Roadmap Scaling**

- Pitch
- Variability

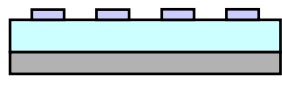
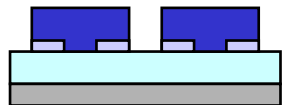
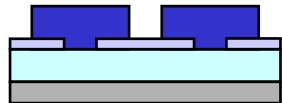
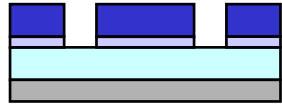
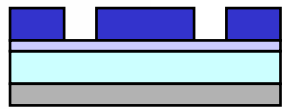


# Double Patterning (DE/DE)

**Conventional  
Single Expose**



**Double Exp/  
Double Etch**



-  Resist
-  Hard Mask
-  Under Layer
-  Substrate

Expose #1

Hard Mask  
Etch

Coat #2

Expose #2

Etch Hard Mask

Etch

## *Double Patterning Challenges*

- Resist / Process
- Overlay
- DFM: DE split CAD
- COO

Variety of application  
dependent processes

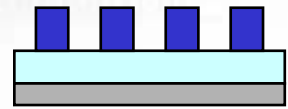
From Andrew Grenville.



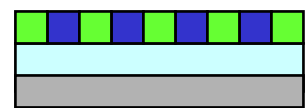
# Double Patterning (DE/SE)

**Conventional  
Single Expose**

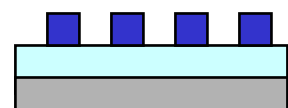
**Double Exp/  
Single Etch**



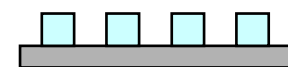
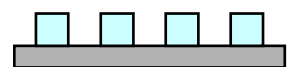
Expose #1



Expose #2



Develop



Etch

*Double Patterning  
SE Challenges*

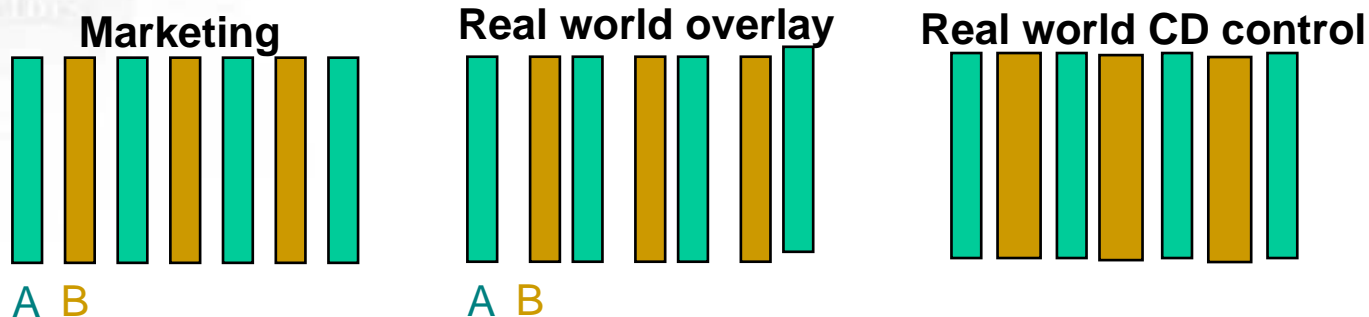
- Resist / Materials
- Overlay
- DFM: DE split CAD
- COO (Litho only)

- Resist
- Latent Image
- Under Layer
- Substrate

Materials not yet available



# Double Patterning Requirements



- **Mask table entries (for performance)**
  - Image placement for double patterning (~70% of single exposure value)
  - Difference in CD mean-to-target for two masks used as a double patterning set
- **Resist table entries (for yield)**
  - Defects in spin-coated resist films for double patterning (50% of single exposure value)
  - Backside particle density for double patterning (50% of single exposure value)

# Double Patterning Table Additions

<b>Optical Mask Requirements</b>	<i>2006</i>	<i>2007</i>	<i>2010</i>	<i>2013</i>
DRAM HP (nm)	70	65	45	32
Image placement for double patterning	<b>5.7</b>	<b>4.9</b>	<b>3.4</b>	<b>2.4</b>
Difference in CD Mean-to-target for two masks as a double patterning set	<b>2.8</b>	<b>2.6</b>	<b>1.8</b>	<b>1.3</b>

**Red for 2006-2007 indicates that general case for double exposure patterning is not possible in this timeframe. Certain double exposure cases require less tight overlay and mask image placement. .Issue will be addressed in 2007 update**

<b>Resist Requirements</b>	<i>2006</i>	<i>2007</i>	<i>2010</i>	<i>2013</i>
DRAM HP (nm)	70	65	45	32
Defects in spin-coated resist films for double patterning (#/cm <sup>2</sup> )	<b>0.005</b>	<b>0.005</b>	<b>0.005</b>	<b>0.005</b>
Backside particle density for double patterning (#/cm <sup>2</sup> )	<b>0.285</b>	<b>0.14</b>	<b>0.14</b>	<b>0.14</b>



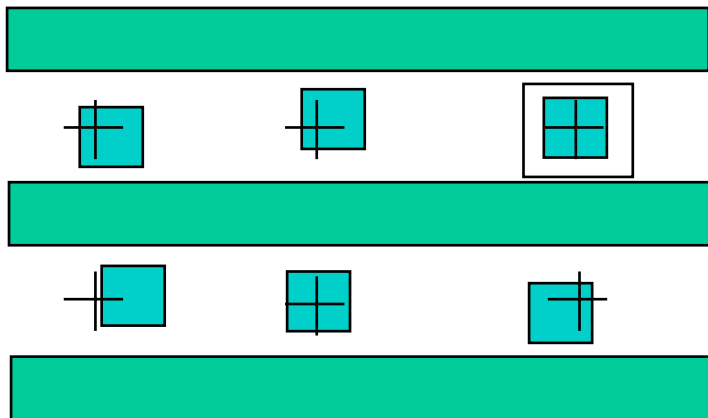
# Difficult Challenges – Double Exposure

- Double exposure / patterning
  - Overlay of multiple exposures including mask image placement
  - Availability of software to split the pattern apply optical proximity correction (OPC), and verify the quality of the split while preserving critical features and maintaining no more than two exposures for arbitrary designs
  - Availability of high productivity scanner, track, and process to maintain low cost-of-ownership
  - Photoresists with independent exposure of multiple passes
  - Fab logistics and process control to enable low cycle time impact that include on-time availability of additional reticles and efficient scheduling of multiple exposure passes



# Overlay

- **Change from 35% to 20% of DRAM half-pitch in 2005**
  - Decision to not make any further changes in 2006
  - Reflects increasing emphasis placed on overlay to achieve device scaling in both Flash/DRAM and logic
- **Overlay red in 2008 (10nm)**
- **Mask tables updated to reflect current industry capability**
  - Now yellow for 10nm and red for 6nm mask image placement
  - Image placement red for 2009 (single exposure)



## Mask Tables Updates

- Color changes only: based on improvements in the industry
  - Achievable resolution, CD uniformity, image placement, flatness, linearity, and defect sizes
  - Color added to MEEF tables
  - Applied to EUVL, optical, and imprint tables
- Added lines for double exposure (mask image placement and mask critical dimension (CD) mean)
- Corrected data volume values for EUVL

## Resist Table Footnote

- Due to shot noise effects, the required sensitivity will increase with decreasing critical feature size. Sensitivity may increase beyond the table values for 22nm half-pitch and smaller dimensions.
- *Issue will be revisited with a white paper study for the 2007 update*



# Summary

- Potential solutions updated to clarify “193nm extensions” to specifically reference non-water based immersion and double patterning
- 2006 Lithography update concentrated on adding requirements for double patterning
  - New table entries added for optical mask requirements and resist requirements
  - Difficult challenges section added
- No change to dramatic overlay tightening made in 2005
- No substantial updates made to EUVL or nanoimprint tables

