

Yield Enhancement - International Technical Working Group

ITRS HsinChu December 5, 2006

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International Technology Roadmap for Semiconductors

HsinChu - December 5, 2006

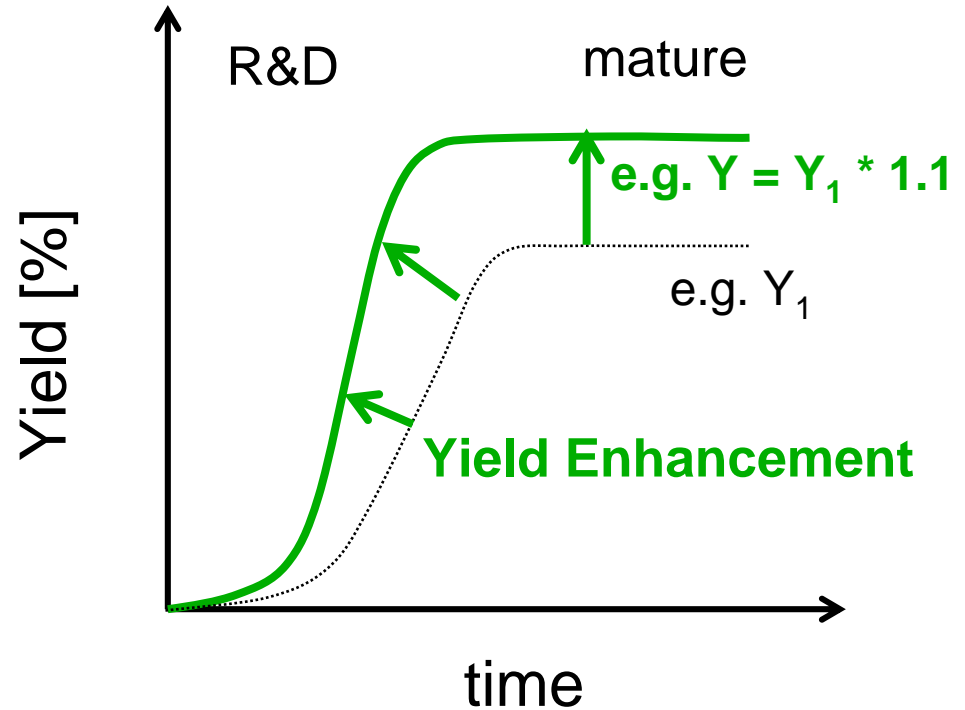
Outline

- Chapter Outline
- Organization of the Chapter
- 2006 Key Challenges
- 2006 Update at a Glance
- Yield Enhancement International Technical Working Group contributors
- Subchapters
 - Defect Detection and Characterization
 - Wafer Environment Contamination Control
 - Yield Model and Defect Budgets
- Defect Budget Survey
- Outlook



Chapter Outline

- Scope and topics
 - improvement from R&D yield level to mature yield
 - limited to front-end processing
 - defect detection
 - yield learning/fast ramp



Phase 1: R&D yield level → YE → **speed up yield detracting identification**

Phase 2: ramp-up yield level → YE → **Faster ramp up**

Phase 3: mature yield level → YE → **Higher yield levels!**



Organization of the Chapter

- **Chair:** Lothar Pfitzner (Fraunhofer IISB) **Co-Chair:** Dilip Patel (Intel assignee to SEMATECH)
- Difficult Challenges
 - Table 109
- Technology Requirements and Potential Solutions
 - Yield Model and Defect Budget (YMDB)
 - Chair: Sumio Kuwabara (NEC) - Japan
 - Table 111
 - Defect Detection and Characterization (DDC)
 - Chair: Ines Thurner (Qimonda) - Europe
 - Table 113
 - Yield Learning (YL)
 - Chair: Tings Wang (Promos) - Taiwan
 - Table 114
 - Wafer Environment Contamination Control (WECC) – USA
 - Chair: Kevin Pate (Intel) - USA
 - Table 115



2006 Key Challenges (No Change!)

- **The Yield Enhancement community is challenged by the following topics:**
 - **Signal to Noise Ratio** – it is a challenge to find small but yield relevant defects under a vast amount of nuisance, false defects.
 - **High Throughput Logic Diagnosis Capability** - identification and tackling of systematic yield loss mechanisms.
 - **Detection of Multiple Killer Defect Types** - and simultaneous differentiation at high capture rates, low cost of ownership and throughput.
 - **High-Aspect-Ratio Inspection** - need for high-speed and cost-effective high aspect ratio inspection tools remains as the work around using e-beam inspection does not at all meet requirement for throughput and low cost.
 - **Process Stability vs. Absolute Contamination Level Including the Correlation to Yield** - data, test structures, and methods are needed for correlating process fluid contamination types and levels to yield and determine required control limits.
 - **In - line Defect Characterization and Analysis** – as an alternative to EDX analysis systems [1]. The focus is on light elements, small amount of samples due to particle size and microanalysis
 - **Wafer Edge and Bevel Control and Inspection** - In order to find the root cause inspection of wafer edge, bevel and apex on front and backside is needed
 - **Data Management and Test Structures for Rapid Yield Learning** - to enable the rapid root-cause analysis of yield-limiting conditions
 - **Development of Parametric Sensitive Yield Models** - including new materials, (OPC) – optical proximity correction - and considering the high complexity of integration.

NEW PROPOSAL:

- **Variation of Critical Dimensions** – how to monitor the variations of Critical Dimensions, how can we minimize the CD variations, how do we specify the tolerances and how can we get immunity/robustness for the variations.



2006 Update at a Glance

- **Defect Budget and Yield Model :**
 - Standardization of chip size for PWP
 - Introduction of Y_{Material} to separate starting material based yield degradation from process based one.
- **Defect Detection and Characterization:**
 - Check and update of tables
 - Estimation of impact of roughness on non patterned inspection and definitions for coordinate precision
- **Wafer Environment and Contamination Control:**
 - Check and update of tables
 - Continuous introduction of new materials drive the lists of ionic and other elemental impurities
 - Focus on organic contamination
 - Understand particle measurements in liquids better



2006 YE ITWG Contributors (updated)

Europe

Ines Thurner (DDC; Qimonda)
Lothar Pfitzner (Chair; Fraunhofer IISB)
Andreas Nutsch (DDC; Fraunhofer IISB)
Andreas Neuber (WECC; MW Zander)
Benoit Hirschberger (DDC; STM)
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Hubert Winzig (WECC; Infineon)
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Japan

Sumio Kuwabara (DB&YM; NEC EL)
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Yoko Miyazaki (DDC; Accretech)
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Yoshimi Shiramizu (WECC; NEC EL)
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Kazuhiro Honda (DDC; JEOL)
Isao Kojima (DDC; AIST)

Taiwan

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Korea

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Joseph O'Sullivan (WECC; Intel)
Keith Kerwin (WECC; TI)
Kristen Cavicchi (WECC; BOCE)
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Mark Camenzind (WECC; Air Liquide)
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Ralph Richardson (WECC; AirProducts)
Rob Henderson (WECC; YieldService)
Robert McDonald (WECC; Metara)
Sarah Schoen (WECC; Air Liquide)
Slava Libman (WECC; Intel)
Scott Anderson (WECC; Air Liquide)
Stephen Toebe (WECC; Brooks)
Steve Hues (WECC; Micron Technology)
Terry Stange (WECC; Hach Ultra)
Tom Gutowski (WECC; Pall (Tom
passed away this year))
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Victor Chia (WECC; Cascade Labs)
William Moore (WECC; IBM)
James S. Clarke (DDC; Intel)
Ken Tobin (DDC; ORNL)

**Thank you
very much!**

United States

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Bart Tillotson (WECC; Fujifilm Electronic
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Chris Long (WECC; IBM)
Chris Muller (WECC; Purafil)
Dan Rodier (WECC; IBM)
Dan Wilcox (WECC; AMD)
Dave Roberts (WECC; Air Products)



Defect Detection and Characterization

- 2006 update
 - patterned wafer inspection:
 - specifications for 90 % and 50 % capture rate
 - non patterned wafer inspection
 - consider roughness of layers
- future objectives
 - macro inspection table
 - divide table 113 into three tables to the topics patterned, non-patterned inspection, and characterization
 - discuss coordinate accuracy and requirements
 - discuss non-patterend inspection table
 - HARI specification: verify for application of DUV solutions



Wafer Environment Contamination Control

- 2006 update
 - Check and update of tables:
 - Review and alignment of particle specification with front end processing group
 - Alignment of specs for gases and cleanroom environment with litho group
 - Improvement of footnote structure shall allow for easier reading
 - Continuous introduction of new materials drive the lists of ionic and other elemental impurities
 - Focus on organic contamination
 - Better understanding of particle measurements in liquids:
 - Results and impact depend from material and used instrument
- Future objectives – New proposals and revisions
 - Show clearly impact of process integration on specifications, e.g. contamination removal by subsequent cleaning steps, thereby align WECC requirements with FEP, and in the future also Interconnect, Litho and others
 - Revise specifications, which can be relaxed, if there is not enough process related evidence, why they are needed or why they are at a certain level.



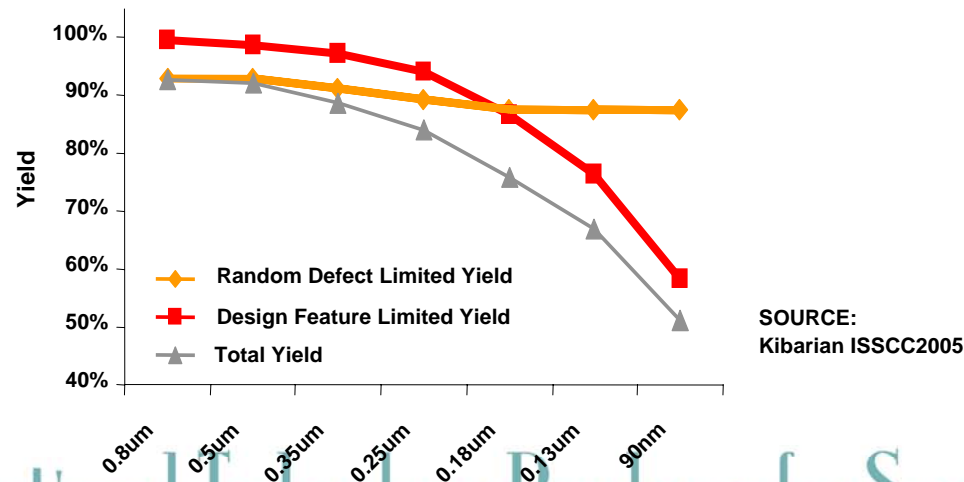
Wafer Environment Contamination Control

- Future objectives – New proposals and revisions
 - Update list of critical ions - New ions to be considered in process monitoring: Pt, Co, Ru, Pd due to potential cross-contamination issues
 - Update gas contaminant lists based on the bulk gas list similar to ion list
 - Complement materials about measurement and monitoring methods
 - Continue work on particle specifications and measurement methods and their limitations.
 - Continue work to establish process specific requirements.
- Future objectives – New topics and issues
 - Complementation of Wafer Environmental Contamination Control (WECC) requirements with Wafer Environmental Process Control (WEPC) requirements incl. definition of relevant SPC specifications and limits
 - Organics and their speciation
 - Which organics are detrimental? Which processes are impacted (e.g. lense hazing)?
 - Is TOC a valid parameter vs. individual species?



Yield Model and Defect Budget

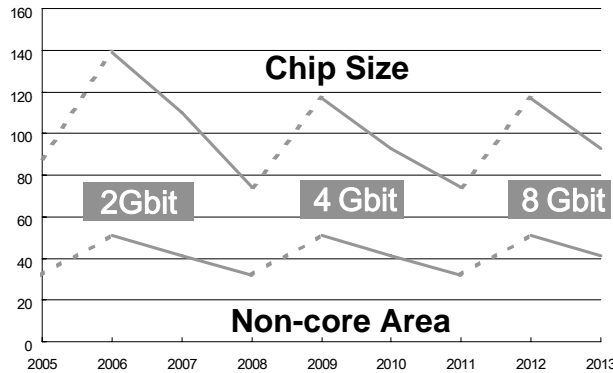
- 2006 update
 - Standardization of chip size for PWP
 - Introduction of Y_{Material} to separate starting material based yield degradation from process based one according to a request from FEP.
- future objectives
 - Unified yield model including both **systematic** and **random** defect variables for holistic YE approach, and its budgets



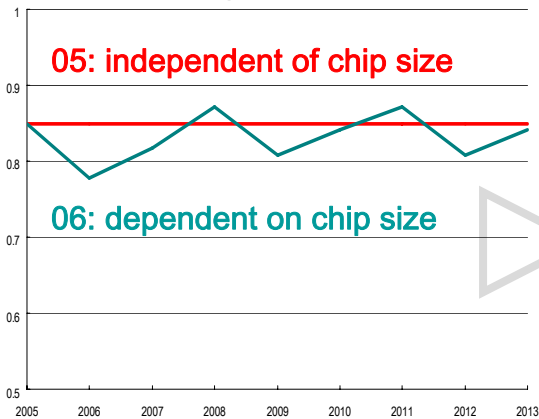
Yield Model and Defect Budget

- Standardization of chip size for PWP

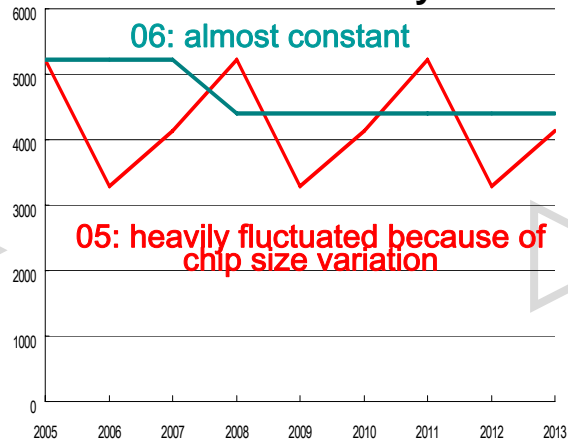
Imported Chip Size from ORTC (DRAM)



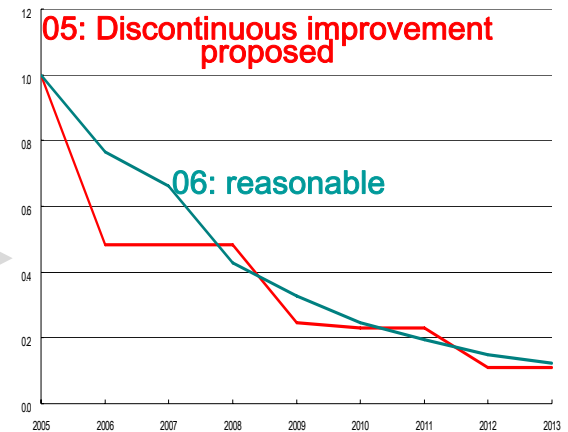
Target Yield



Defect Density



PWP(normalized)



- **Improvement of the Yield Enhancement chapter**
 - Highly active subchapters DDC, WECC, DB&YM → improve activity of YL (acquisition of members in Asia and other regions) and discuss enhancement of scope and improvements of the YL subchapter
 - Adjust outline and content of the chapter and make necessary changes to reflect current/future needs
 - revision of the tables → have a close look on the size and content of the tables - divide tables and change outline of the chapter