International Technology Roadmap for Semiconductors

Assembly and Packaging
2006

Assembly and Packaging Roadmap 2006 Participants

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ITRS A&P Chapter Organization

- Scope
- Difficult Challenges
- Technical Requirements
- Infrastructure Challenges
- Potential Solutions
- Tables

Assembly and Packaging Roadmap 2006

- Packaging has become the limiting element in system cost and performance
- The Assembly and packaging role is expanding to include system level integration functions.
- As traditional Moore's law scaling become more difficult innovation in assembly and packaging can take up the slack.

Assembly and Packaging Emerging as Limiting Factor for Cost and Performance

- Consumers now drive more than half of integrated circuit revenue
- Assembly and Packaging technology is a primary differentiator for consumer electronics
- These factors are driving an unprecedented pace of innovation in:
  - New Materials
  - New Technologies
  - New Systems Integration

Assembly and Packaging

The pace of change in several areas is faster than anticipated

- System in a package (SiP) has become the structure of choice for many consumer products with new requirements for package design, materials, processing and test access
- Wafer thinning has progressed to a level requiring special handling and assembly processes
- Stacked die package layer count is increasing rapidly requiring new methods for bonding, testing, etc.

Packaging Technology Challenges

Interconnect Scaling
Connect Si features (nm) to circuit board features (cm)

High Speed Signaling
Facilitate distortion – free signaling

Power Delivery
Efficiently deliver Power to enable high speed Si performance

Power Removal
Efficiently duct away dissipated power

New Packaging Technologies

- Thinned wafers
- 3D systems integration
- Wafer level packaging
- Bio-chips
- Integrated optics
- Embedded/integrated active and passive devices
- MEMS
- Printable circuits
  - Semiconductors
  - Light emitters
  - RF
  - Interconnect
- Flexible (wearable) electronics

Systems Integration in the Cellular Phone

It is not only integrated circuits

Embedded Antenna

- Smaller・ Stability of signal
- Influence on the human body

Camera Circuit

- Smaller
- Lower power consumption
- One unit of lens and control circuit

LCD Circuit

- Larger display, Color display
- Lower power consumption
- Higher resolution

Memory Circuit

- Memory area for downloaded software
- Higher memory capacity

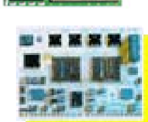
DSP・ CPU・ BB

- Dual CPU: Transmission /Application

Plug In Memory Card

- Smaller, thinner
- Higher memory capacity

Tx、Rx Circuit



- Smaller & lower power consumption of analog circuit
- Decrease of # of mounted components

Power Supply Circuit

- Smaller Size

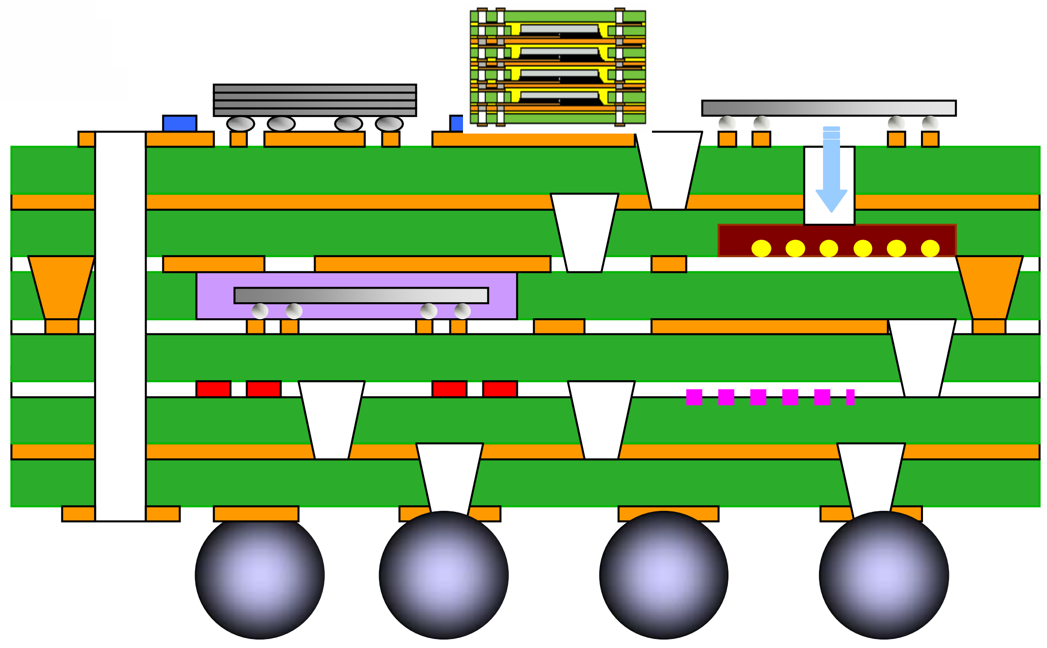
Outer Interface Circuit

- Bluetooth, USB interface
- MP3, GPS interface
- Memory Card interface

Source: H.Ueda JEITA

SiP: Multi-level System Integration

SiP may include SoC and other traditional packages



Packages may include:

- ➔Sub-system packages
- ➔Stacked thin packages containing passives and active chips
- ➔Mechanical, optical and other non electrical functions
- ➔Complete systems or sub-systems with embedded components
- ➔Bare die

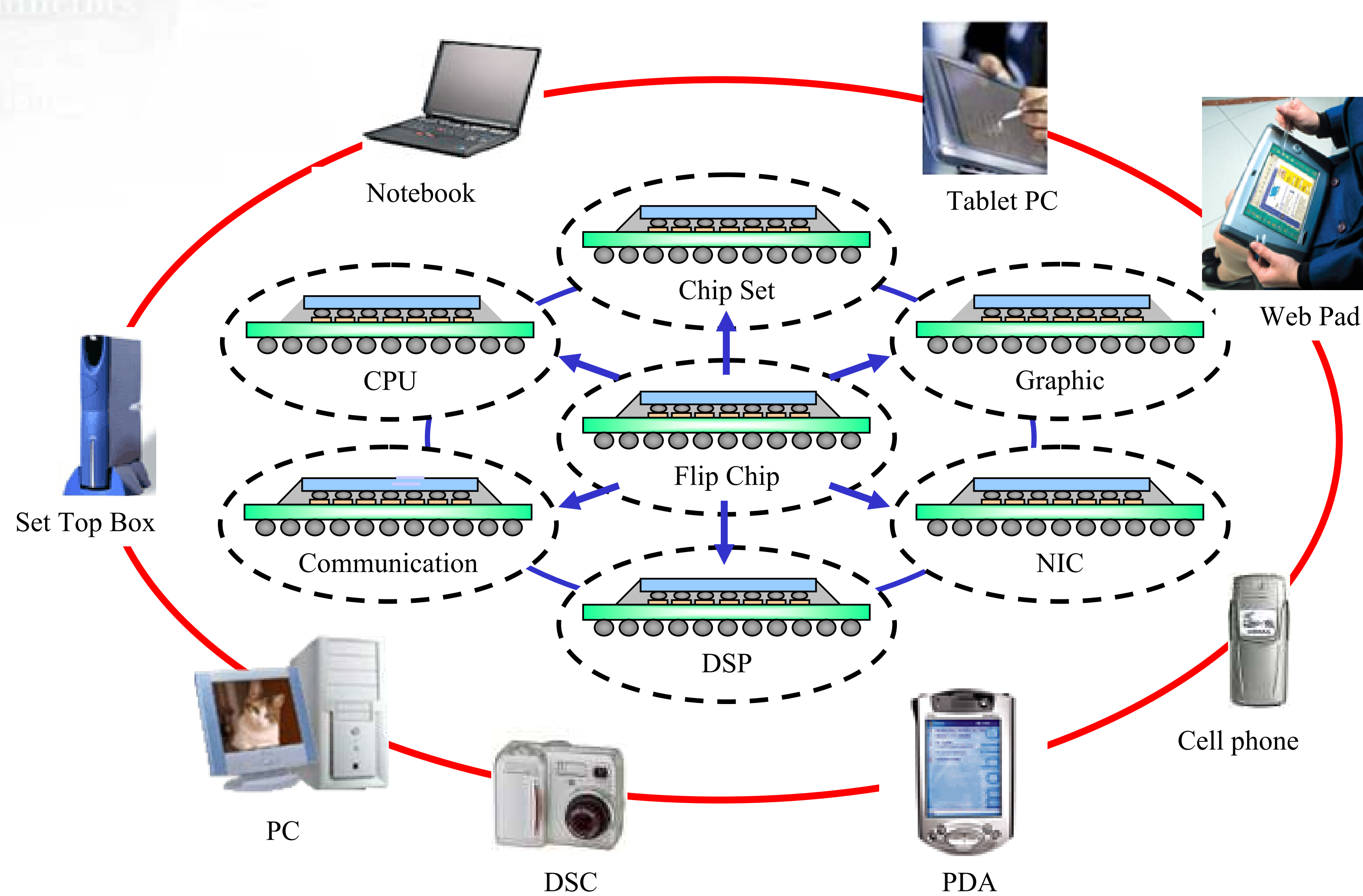
Source: Fraunhofer IZM

Categories of SiP

Category	Sub-category	Types
Horizontal Placement		Wire Bonding Type; Flip Chip Type
Stacked Structure	Interposer Type	Wire Bonding Type; Wire Bonding + Flip Chip Type; Flip Chip Type
	Interposer-less Type	Terminal Through Via Type
Embedded Structure		Chip (WLP) Embedded + Chip on Surface Type; 3D Chip Embedded Type; WLP Embedded + Chip on Surface Type

Source: 20030710 K. Nishi, Hitachi, JEITA; Revised by H. Utsunomiya

Applications for Flip Chip based SiP



Package substrate is the key issue for Flip Chip

Source： IEK/ITRI)

Assembly and Packaging

There are significant revisions to tables

- Difficult Challenges
  - Pb free transition presents cost, reliability and process compatibility problems that are not resolved
  - A new generation of DFM and DFT will be required for complex SiP and SoC packaging
  - Stress induced changes in electrical properties for very thin die
  - Reliability for through wafer vias and die layer bonding
  - Warpage control for stacked die
  - Interconnect for nano-scale structures
  - Self assembly for very small die

Significant Table Revisions

Continued

- Many new Materials are required for the emerging package requirements:
  - Improved thermal conductivity for dielectrics and materials interfaces
  - Molding compounds compatible with copper and other new materials
  - Improved resistance to electromigration as temperature and current density continue to rise
  - Dielectrics with improved fracture toughness and interfacial adhesion
  - Green materials that meet regulatory, cost and reliability requirements

New Materials

Most, if not all, packaging materials will change within this decade

- Cu interconnect
- Ultra Low k dielectrics
- High k dielectrics
- Organic semiconductors
- Green Materials
  - Pb free
  - Halogen free
  - other

Assembly and Packaging
Technical working Group 2006 Focus

We are giving special focus in 2006 to preparation of a white paper titled:

"The next step in Assembly and Packaging: Systems Level Integration"

Objectives of this white paper

- Catalyze additional SiP chapter for 2007 ITRS issue
- Identify needs and gaps
- Identify new technology trends for future SiP

"The next step in Assembly and Packaging: Systems Level Integration"

Introduction & Motivation

- The basic elements generic to all SiP System level integration applications will be defined.
- Examples will be used from various application areas to show how the basic elements are incorporated into these applications.

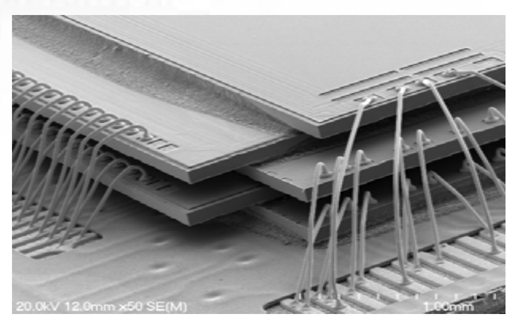
Critical updates to selected sections in preparation for 2007

- Expansion of the section on handling and packaging of extremely thin die
- Expanded treatment of sensors in cooperation with iNEMI

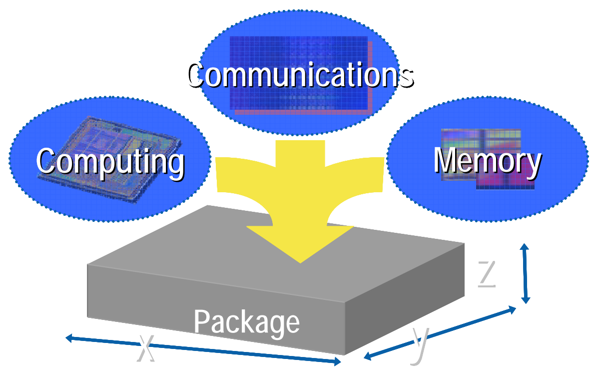
In Preparation for 2007

- “More than Moore”
  - SiP
    - At the limit Camera, wireless, logic, memory, display, data entry (human interface), location (GPS), sensors (accelerometers), security, MEMS
    - Lower cost, smaller size, lower power, higher performance
  - 3D packaging
    - TSV and laminated layers
  - System integration (including thermal management)
  - Embedded passive and active devices
  - Power subsystems
  - Wafer level packaging

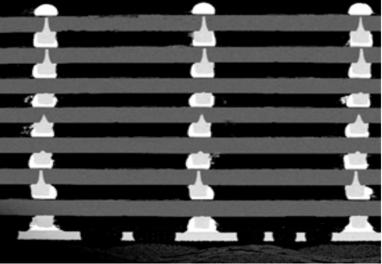
3D Packaging increases Performance Density and enables system level integration


Wire bonded stacked die

New System in Package (SIP) solutions enables rapid integration of different functions



Small form factor for ultramobile PCs, hand-helds, phones & other consumer electronics


Thru-Si via Stacking