

Interconnect Working Group



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Hsinchu, Taiwan

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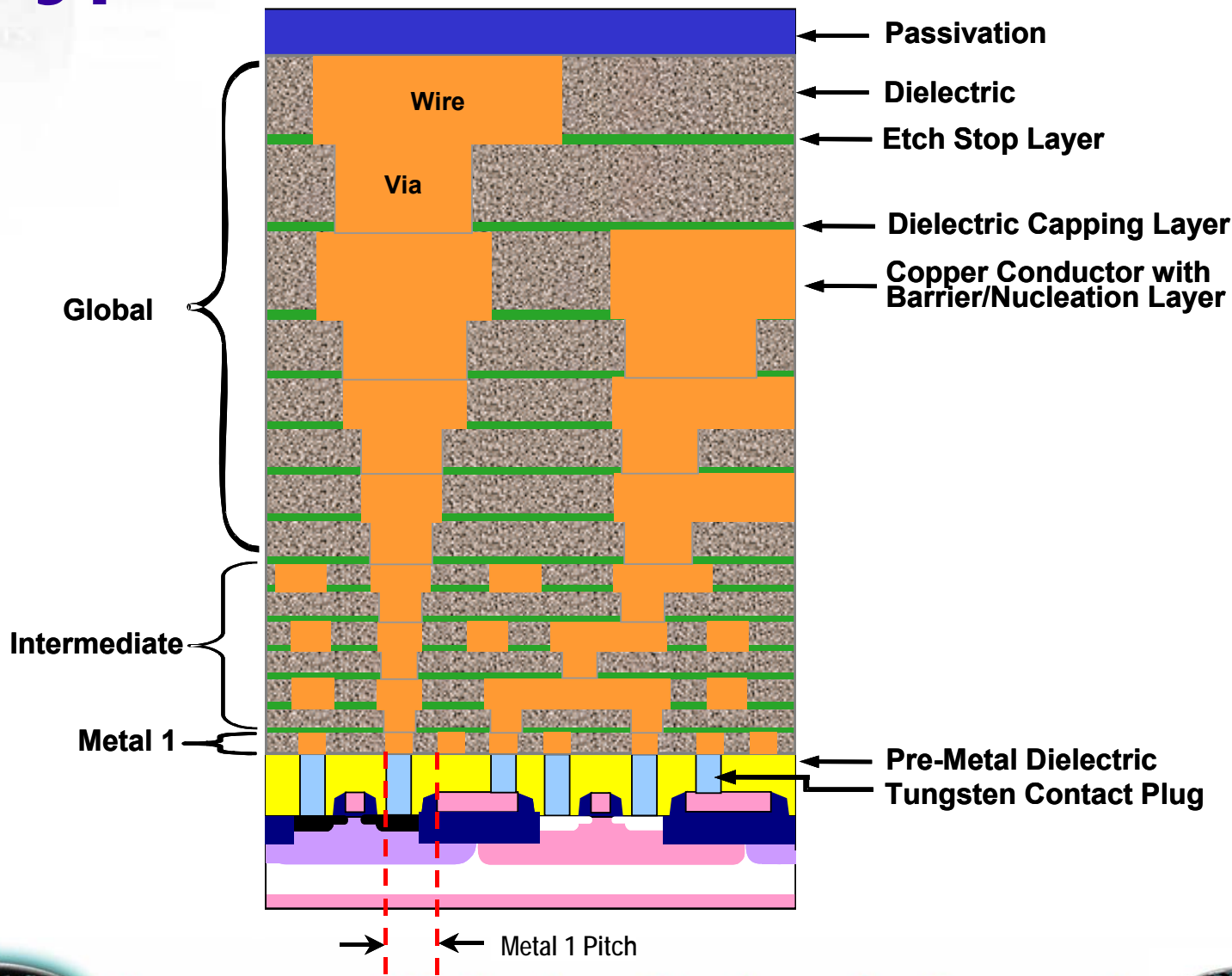
Agenda

- **Scope and structure**
- **Technology requirements**
- **Difficult challenges**
- **Cu resistivity effects**
- **Energy and performance**
- **Low k roadmap**
- **Emerging interconnect**
- **Last words**

Interconnect scope

- Conductors and dielectrics
 - Starts at conductor etch
 - Metal 1 through global levels
 - Includes the pre-metal dielectric (PMD)
- Associated planarization
- Necessary etch, strip and cleans
- Embedded passives
- Reliability and system and performance issues
- Ends at the top wiring bond pads
- Predominantly “needs” based, with some important exceptions (κ and resistivity)

Typical MPU cross section



Technology Requirements

- Tables for HP MPU and ASIC plus DRAM
- Wiring levels including “optional levels”
- Reliability metrics
- Minimum wiring/via pitches by level
- **Performance figure of merit (Power Index) and capacitance (NEW)**
- Planarization requirements
- Conductor resistivity with and without scattering
- Barrier thickness
- **Dielectric metrics including effective κ (UPDATED)**
- Crosstalk metric
- **Metal 1 variability due to CD and scattering**

Difficult challenges

- *Identify solutions which address wiring scaling issues*
- Introduction of new materials to meet conductivity requirements and reduce the dielectric permittivity
- Engineering manufacturable interconnect structures compatible with new materials and processes

Size matters

- 2003 – the impending impact of Cu resistivity increases at reduced feature sizes (due to scattering) - first noted
- 2004 – metrics introduced to highlight the impact of width dependent scattering on the effective resistivity and impact on RC delay
 - Models have been refined to more accurately predict the resistivity due to changes in aspect ratio, shape and metal thickness
- 2006 - Metrics have been updated
- Adapt the same methodology

Size matters

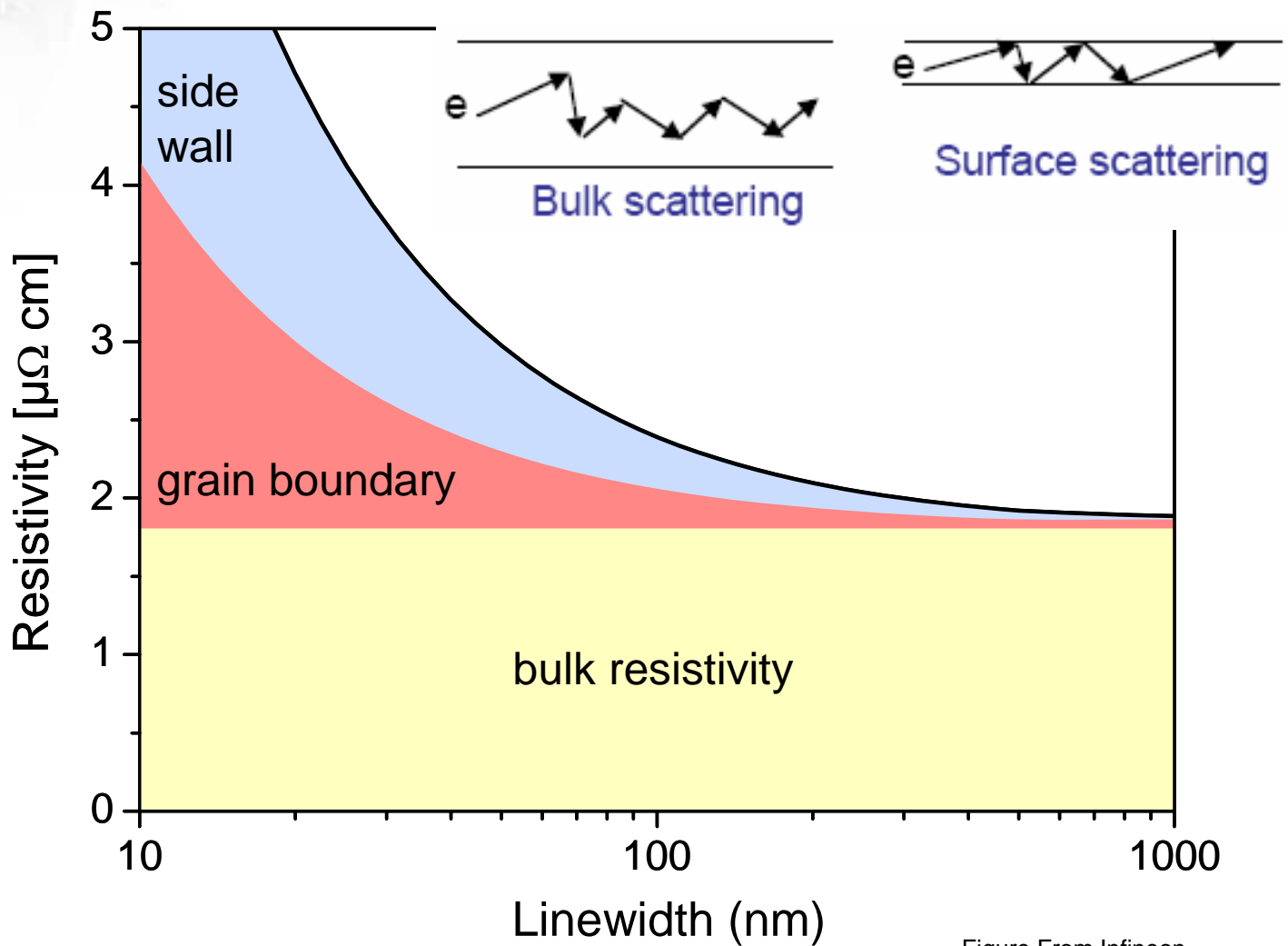


Figure From Infineon

For DRAM, Cu is introduced in 2007

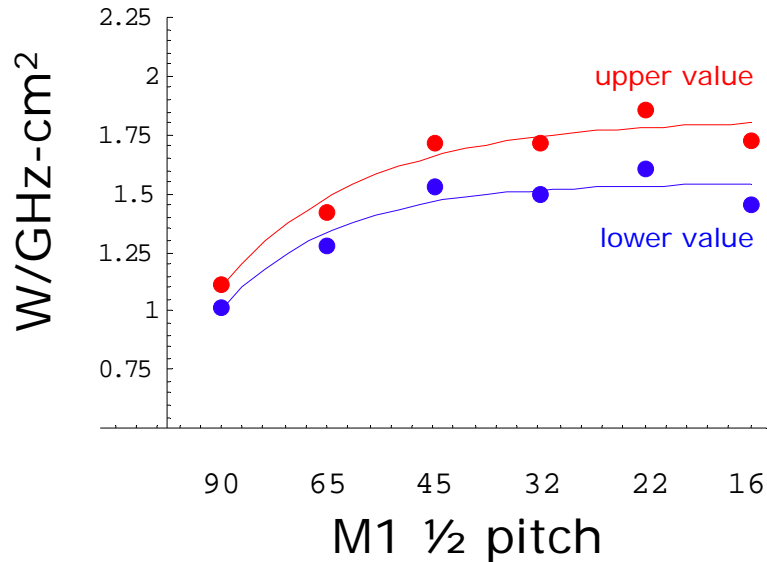
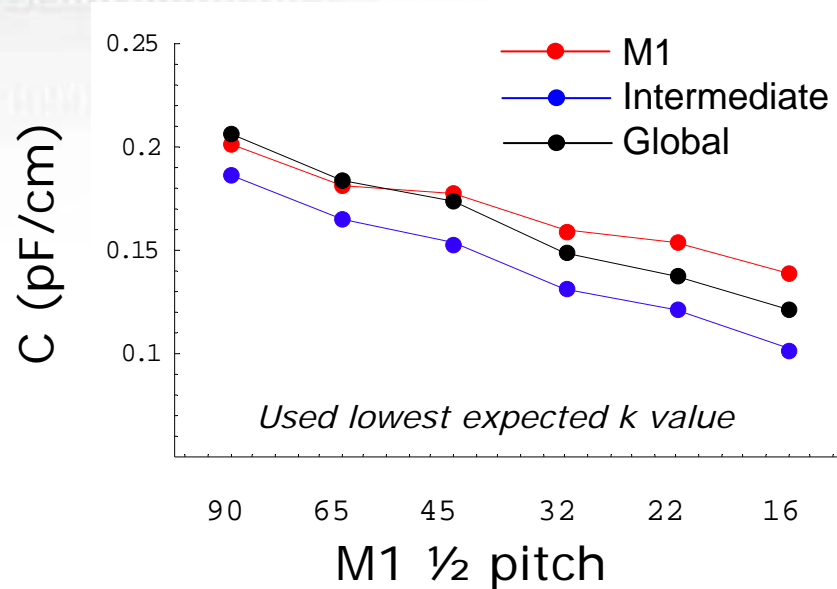
International Technology Roadmap for Semiconductors



Dynamic Power

- Increasing concern about rising dynamic power in the interconnect stack
 - Interconnects make a significant contribution to total dynamic power
- Impacts effective k roadmap
 - Drives reduction in parasitic capacitance
- Dynamic power is a key constraint for high performance MPUs

Capacitance and Power Index



Capacitance decreases

Dynamic power increases

$$P_{layer} \left[\frac{W}{GHz-cm^2} \right] = C \cdot V^2 \cdot a \cdot (1 GHz) \cdot \left(e_w \cdot \frac{1 cm^2}{p} \right) = \text{Power per GHz per } cm^2 \text{ of metal layer.}$$

C = capacitance per unit length.

$V = V_{dd}$, p = pitch, e_w = wiring efficiency, a = average activity factor of interconnects.

Row to be added to table 80a (“**MPU and ASIC Interconnect Technology Requirements—Near-term Years**”) shown in red

M1_half_pitch	90	78	68	59	52	45	40	35	32
Power index (W/GHz-cm²) [x]	1- 1.1	1.2- 1.3	1.3- 1.4	1.3- 1.4	1.4- 1.5	1.5- 1.7	1.7- 1.9	1.4- 1.6	1.5- 1.7

Row to be added to table 80b (“**MPU and ASIC Interconnect Technology Requirements—Long-term Years**”) shown in red

M1_half_pitch	28	25	22	20	18	16	14
Power index (W/GHz-cm²) [x]	1.7- 2.0	1.4- 1.6	1.6- 1.9	1.3- 1.6	1.3- 1.5	1.5- 1.7	1.7- 2.0

FOOTNOTE TO BE ADDED AT THE BOTTOM OF TABLES 80 (a and b)

[x] Power index = $C V_{dd}^2 a (1 \text{ GHz}) e_w (1 \text{ cm}^2)/p$; p = pitch; V_{dd} = supply voltage; e_w = wiring efficiency = 1/3; a = activity factor = 0.03. The calculated values are an approximation for the “power per GHz per cm² of metallization layer”. This index scales with the critical parameters that determine the interconnect dynamic power. NOTES: the values provided are an average for M1, Intermediate and Global interconnects. The range of values results from the maximum and minimum effective dielectric constants.

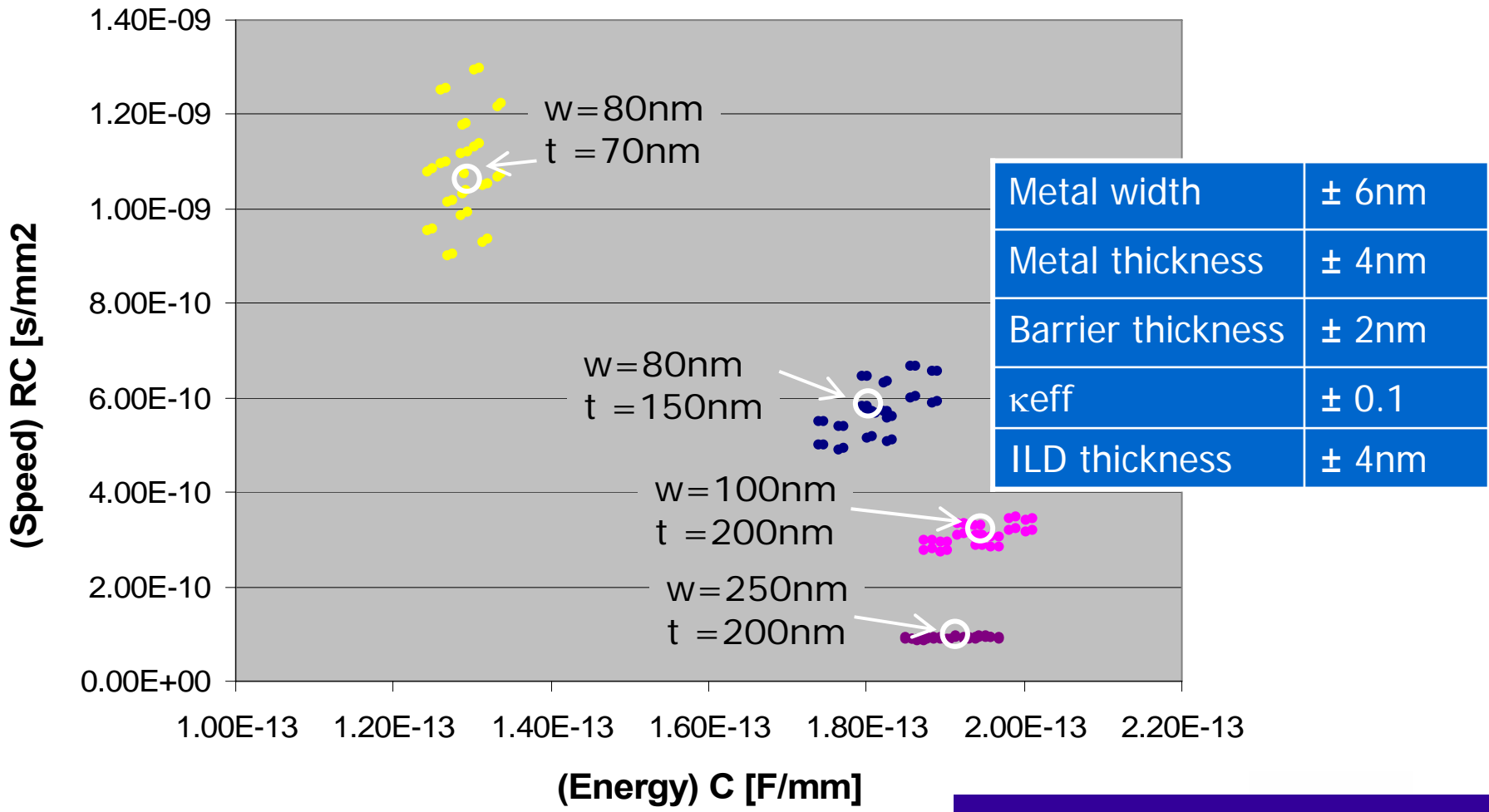
Row to be added to table 80a (“*MPU and ASIC Interconnect Technology Requirements—Near-term Years*”) shown in red

M1_half_pitch	90	78	68	59	52	45	40	35	32
Capacitance per unit length for M1 wires (pF/cm) [y]	2.0-2.2	2.0-2.2	1.8-2.0	1.9-2.1	1.8-2.0	1.8-2.0	1.8-2.0	1.6-1.8	1.6-1.8
Capacitance per unit length for intermediate wires (pF/cm) [y]	1.9-2.0	1.9-2.0	1.7-1.8	1.7-1.8	1.5-1.7	1.5-1.7	1.5-1.7	1.3-1.5	1.3-1.5
Capacitance per unit length for global wires (pF/cm) [y]	2.1-2.3	2.1-2.3	1.8-2.0	1.8-2.0	1.7-1.9	1.7-1.9	1.7-1.9	1.5-1.7	1.5-1.7

Row to be added to table 80b (“*MPU and ASIC Interconnect Technology Requirements—Long-term Years*”) shown in red

M1_half_pitch	28	25	22	20	18	16	14
Capacitance per unit length for M1 wires (pF/cm) [y]	1.6-1.8	1.5-1.7	1.5-1.8	1.5-1.8	1.4-1.6	1.4-1.6	1.4-1.7
Capacitance per unit length for intermediate wires (pF/cm) [y]	1.3-1.5	1.2-1.4	1.2-1.4	1.2-1.4	1.0-1.2	1.0-1.2	1.0-1.2
Capacitance per unit length for global wires (pF/cm) [y]	1.5-1.7	1.4-1.6	1.4-1.6	1.4-1.6	1.2-1.4	1.2-1.4	1.2-1.4

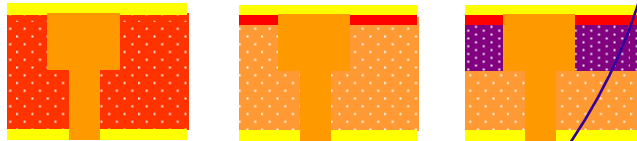
R and C Variability



Low κ again! HP MPU and ASIC

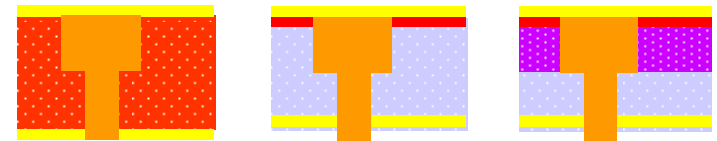
Year of Production	2005	2006	2007	2008	2009	2010	2011	2012	2013
Interlevel metal insulator (minimum expected) – bulk dielectric constant (κ)	≤ 2.7	≤ 2.7	≤ 2.4	≤ 2.4	≤ 2.2	≤ 2.2	≤ 2.2	≤ 2.0	≤ 2.0
Interlevel metal insulator – bulk dielectric constant (κ)	2.6- 3.0	2.6- 3.0	2.3- 2.7	2.3- 2.7	2.1- 2.4	2.1- 2.4	2.1- 2.4	1.8- 2.1	1.8- 2.1

Realistic case in 2007



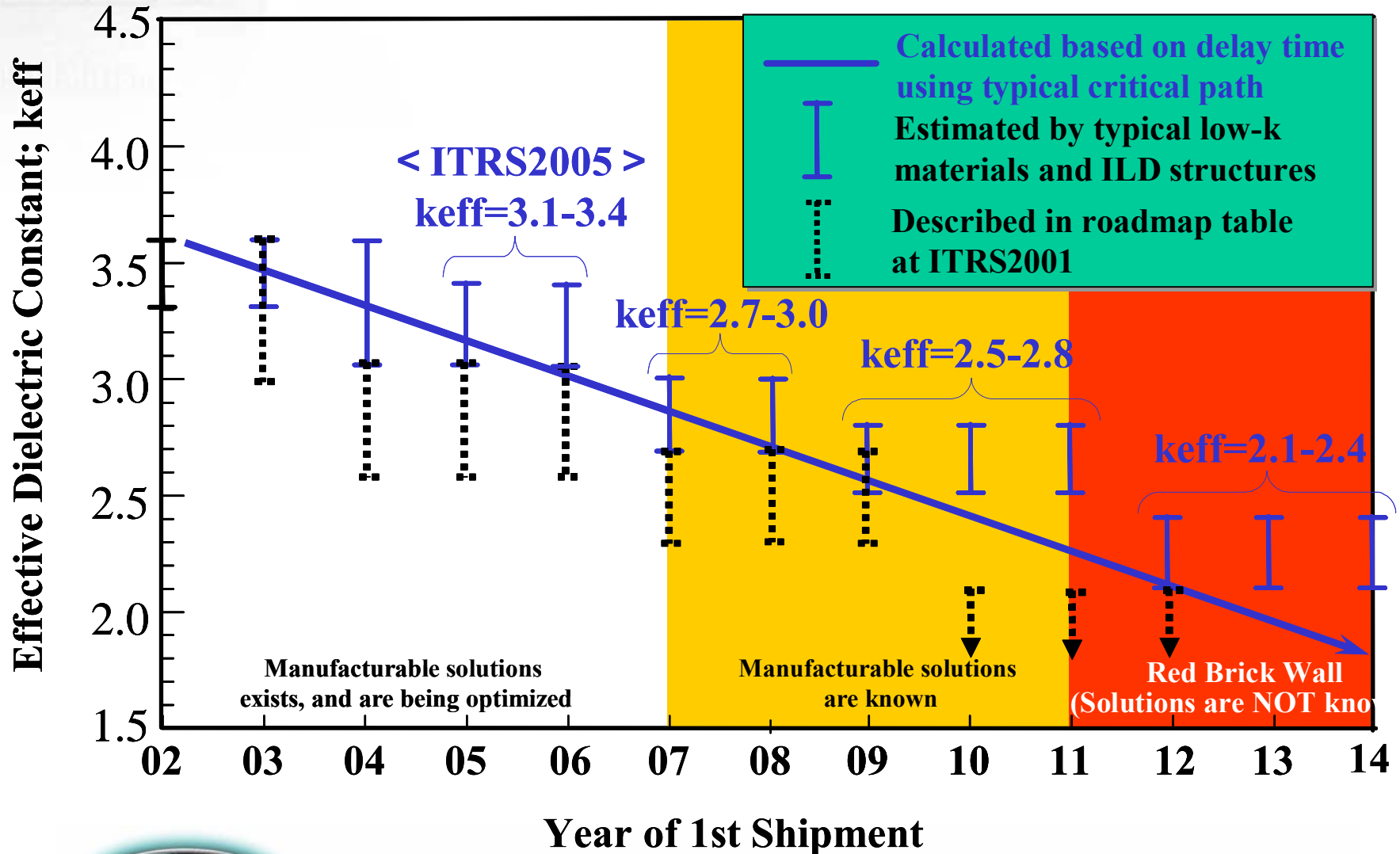
Structure	Homogeneous	Homo w/HM	Hybrid
$\kappa_{(Cu\ D.B)}$	4.0	4.0	4.0
$\kappa_{(Hardmask)}$	NA	3.0	3.0
$\kappa_{(via)}$	2.7	2.5	2.4
$\kappa_{(trench)}$	2.7	2.5	2.5
κ_{eff}	2.96	2.87	2.83

Aggressive case in 2007



Structure	Homogeneous	Homo w/HM	Hybrid
$\kappa_{(Cu\ D.B)}$	4.0	4.0	4.0
$\kappa_{(Hardmask)}$	NA	3.0	3.0
$\kappa_{(via)}$	2.5	2.3	2.3
$\kappa_{(trench)}$	2.5	2.3	2.3
κ_{eff}	2.78	2.72	2.72

Dielectric Constant Trend



Multi-core Impact on Interconnect

- Wiring lengths change
 - Critical path reduced (in core)
 - Mechanical integrity challenges will change
 - Jmax changes
 - Hierarchical structure may no longer be necessary
 - Converge to more fine pitch local/intermediate wires
 - Power and ground delivered through grid
 - Global delay challenge relaxed
 - 3D may include multi-core
- Need to consider splitting metrics into:
 - In-core (intra-tile) and Inter-core (inter-tile)
 - New bandwidth requirements

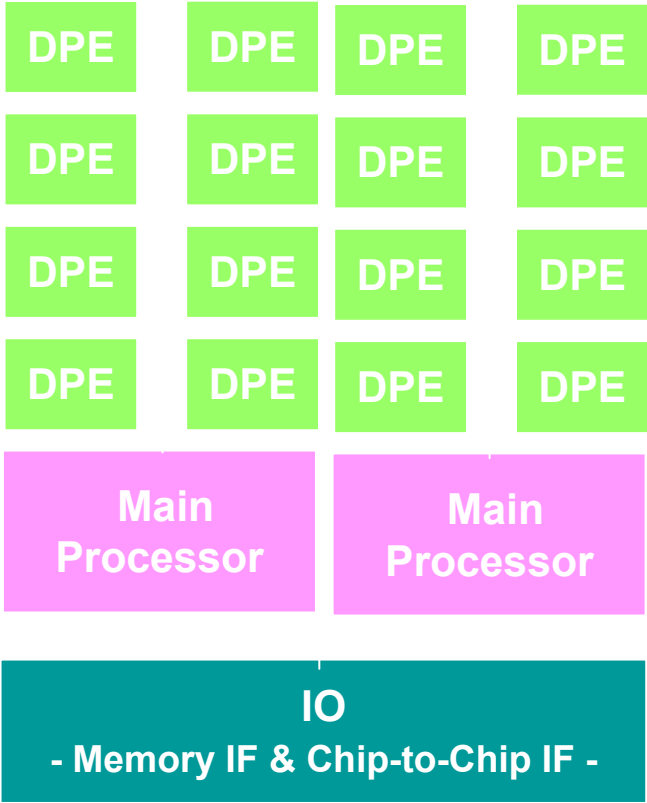


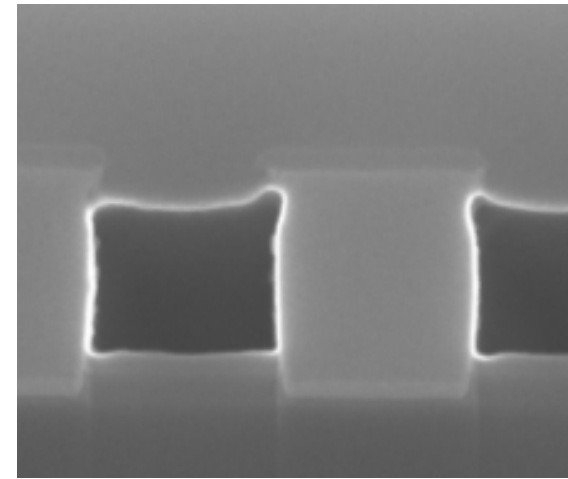
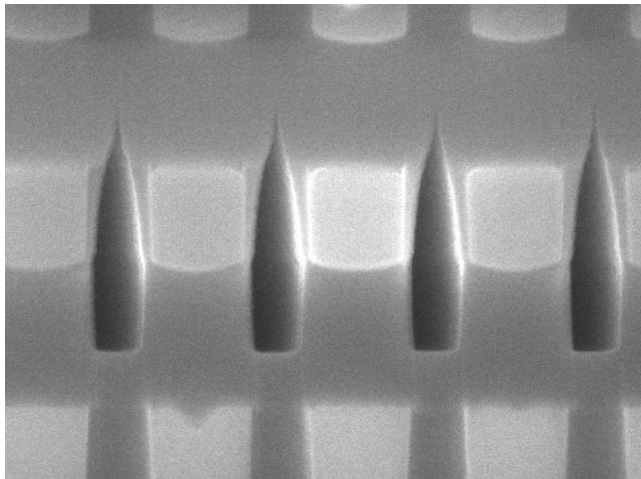
Figure From ITRS 2006 Design TWG

Emerging interconnect

- Use geometry
 - Air gap
 - 3D
- Use different physics
 - Optics (waveguides, emitters, detectors, free space, trans-impedance amps, modulators)
 - RF/microwaves (transmitters, receivers, free space, waveguides)
 - Terahertz photonics
- Radical solutions
 - Nanowires/nanotubes
 - Molecules
 - Spintronics
 - Quantum wave functions

From low κ to no κ - air gaps

- Introduction of air gap architectures
 - Creation of air gaps with non-conformal deposition
 - Removal of sacrificial materials after multi-level interconnects



- ⇒ Values of effective κ -value down to 1.7 with low crosstalk levels
- ⇒ Localized air gaps to maintain good thermal and mechanical properties

Ultra-low κ and Air gap ($\kappa < 2.0$) (CVD & Spin-on)

3D Integration – first thoughts

- Through silicon via (TSV)
 - Reliability
 - Physical metrics (pitch, diameter, density)
- Alignment tolerance
- Bond layer
 - Reliability
 - Interfacial defect density
 - Adhesion
- List of “Difficult Challenges”, e.g. TSV processes, alignment, low κ impact on TSV, etc.

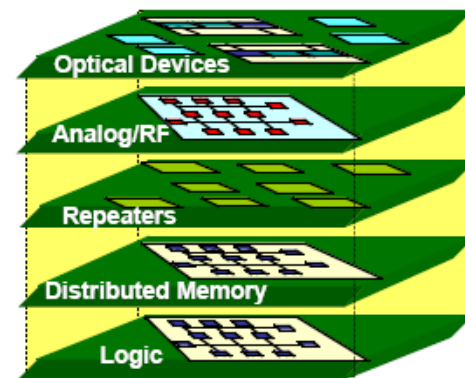


Figure From Stanford

Last words

- **Must manage the power envelope**
- **Develop solutions for emerging devices**
- **Must manage 3D-CD**
- **System level solutions must be accelerated to address the wire scaling grand challenge**
 - **Cu resistivity increase impact appears ~2006**
 - **materials solutions alone cannot deliver performance - end of traditional scaling**
 - **integrated system approach required**