

# **ITRS Design + System Drivers**

**Hsinchu, December 2006**

## **Design ITWG**

**Japan: Hiwatashi-san, Asada-san**

**Taiwan: Chung-Ping Chen**

**Europe: Wolfgang Rosenstiel**

**USA: Andrew Kahng**



# Key Thoughts

## 1. 2004-5: we created a Design Technology Roadmap

- System-level, logic/ckt/physical, DFT, Verification, DFM, ...
- *General* dependency: PIDS, Yield, Interconnect, A&P,...

## 2. 2005-6: we're creating a Systems Driver roadmap

- Consumer, stationary, networking, automotive, ...
- *Driver-specific* dependency: PIDS, interconnect, A&P,...

## 3. Added value = design technology + design innovation

- Design technology: general value add
- Design innovation: driver-specific value add
  - “more than Moore”

# Design Chapter

# Summary of Update

## **1. 2005: First quantitative DT roadmap**

World's first roadmap for DT industry

## **2. 2006: revisions of figures, dates, and challenge items**

System-Level, Verification, other

More sections include table relating challenges-solutions

## **3. 2007: increasing alternative integration methods**

More than Moore

Heterogenous systems, system-in-package (SIP), etc.

# System Drivers Chapter

# Summary of Update

## 1. 2005: Added consumer mobile driver

First new driver not based on microprocessors

## 2. 2006: added/updated drivers

Consumer stationary driver complete

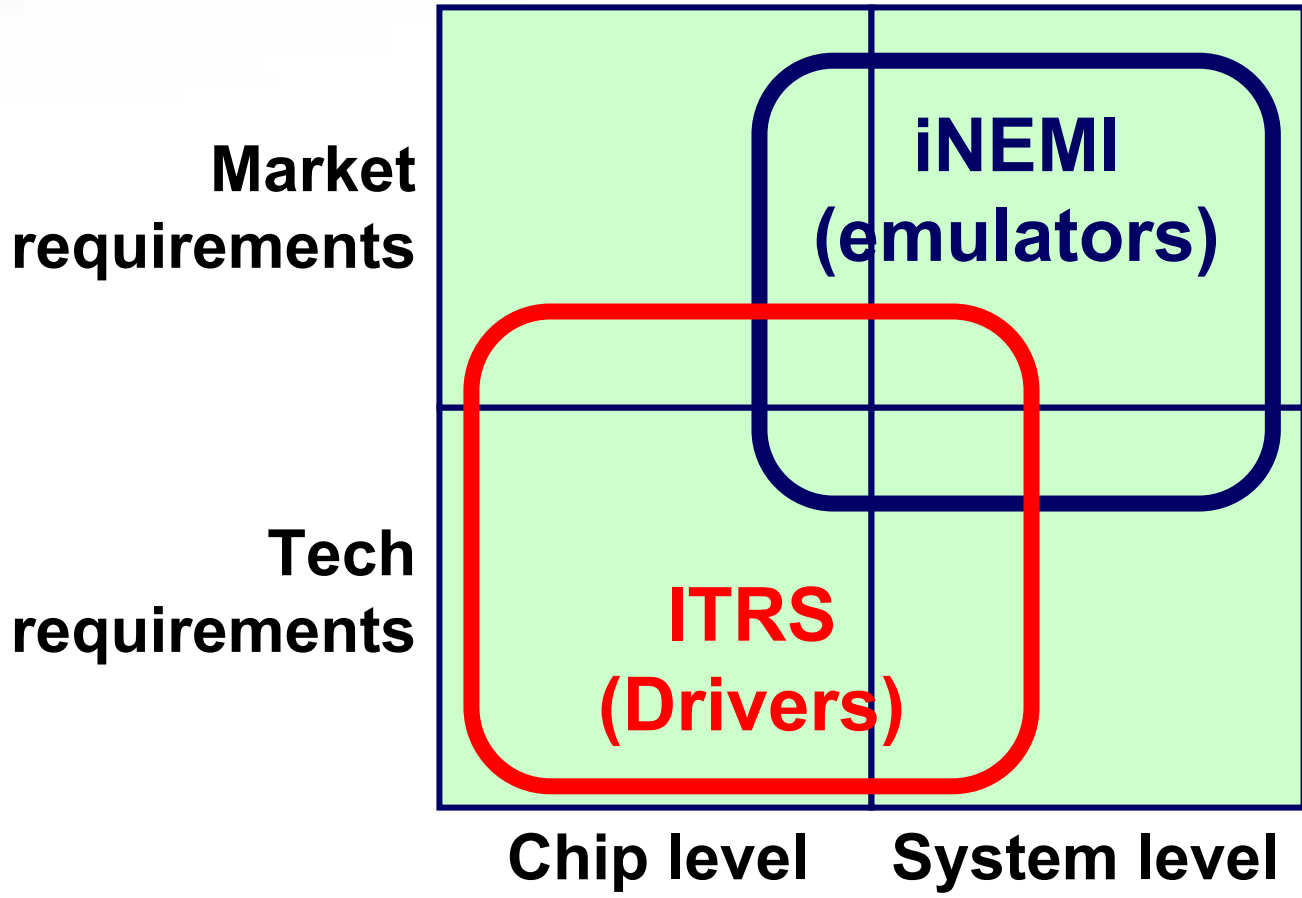
Started networking driver

## 3. 2007: complete system driver roadmap

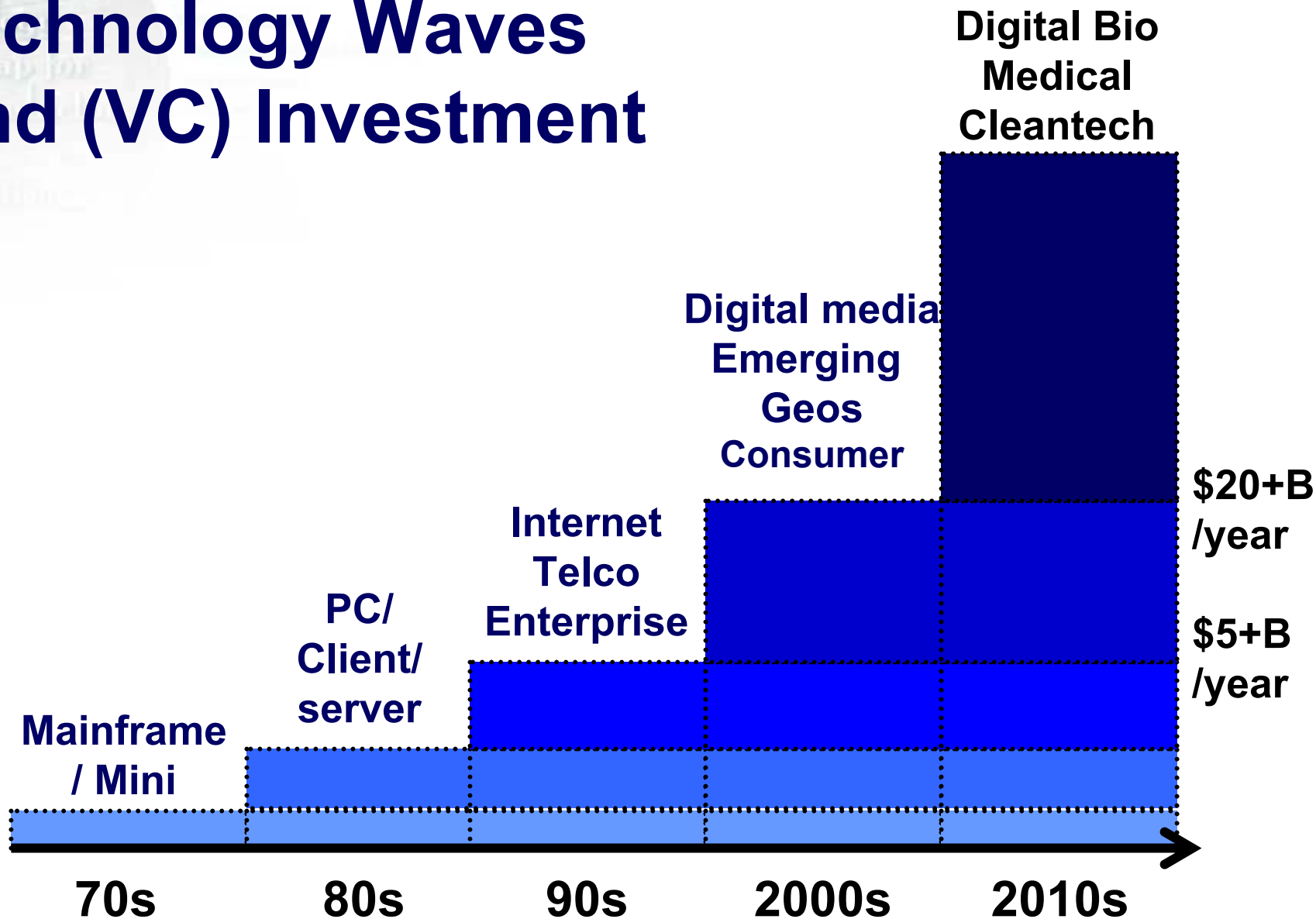
Complete networking driver, update office (processor) driver

Add rest of drivers (medical, defense, automotive)

# ITRS-iNEMI Domain Space



# Technology Waves And (VC) Investment



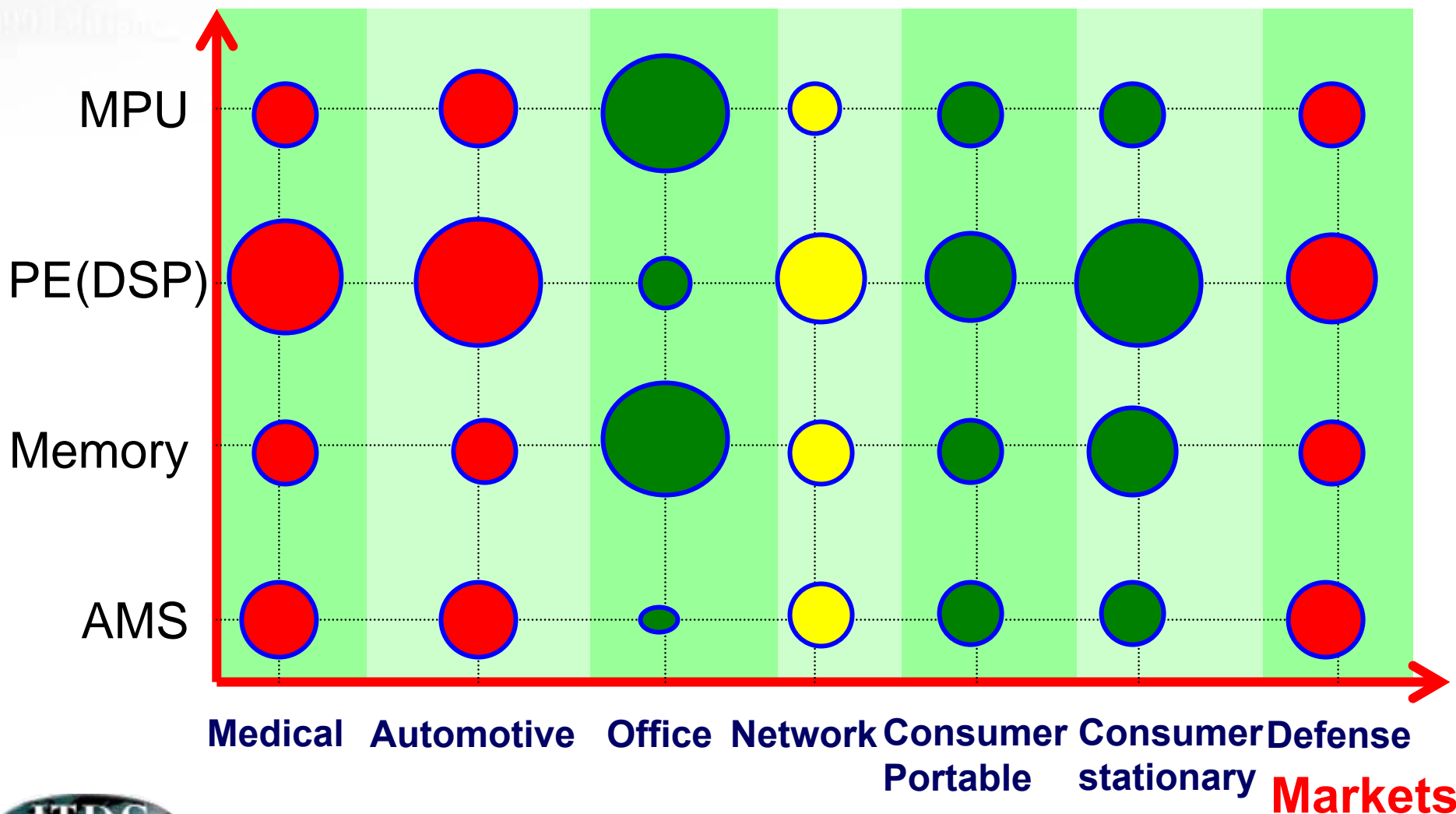
Source: insight from Top VCs including Walden



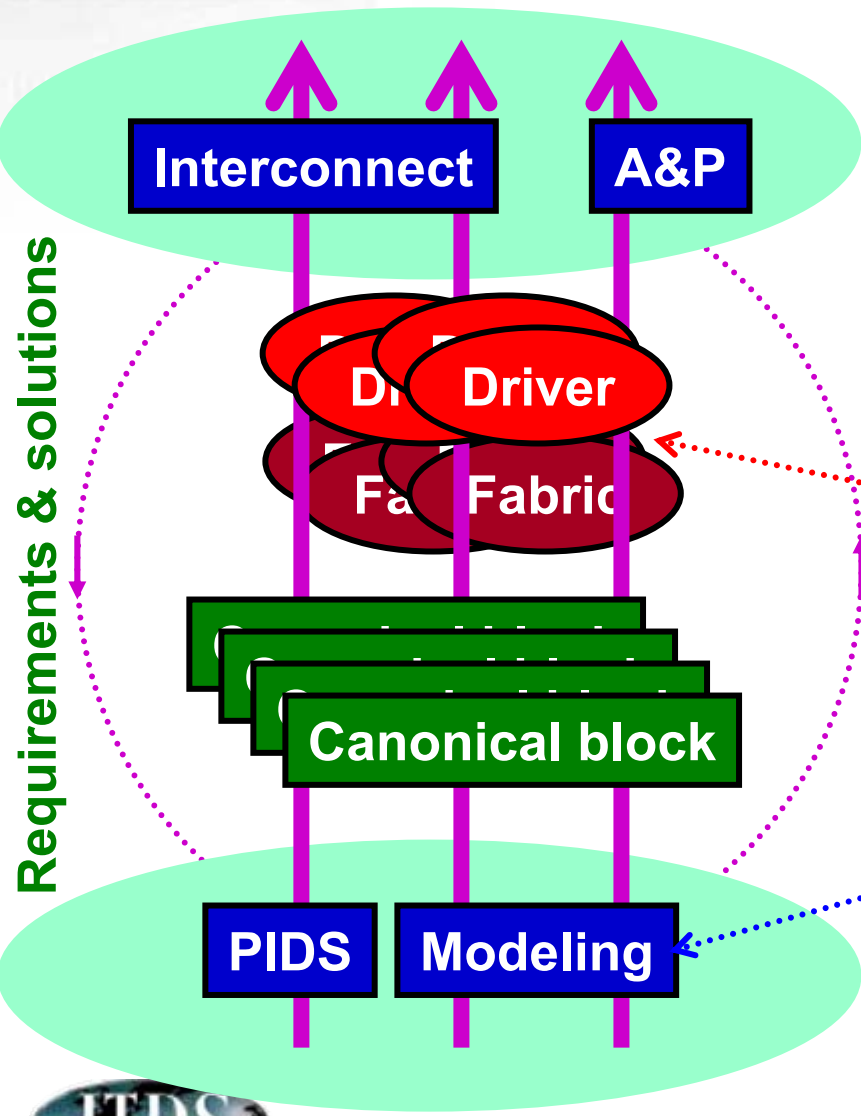
# Market Drivers Starting To Drive Roadmap

**Fabrics**

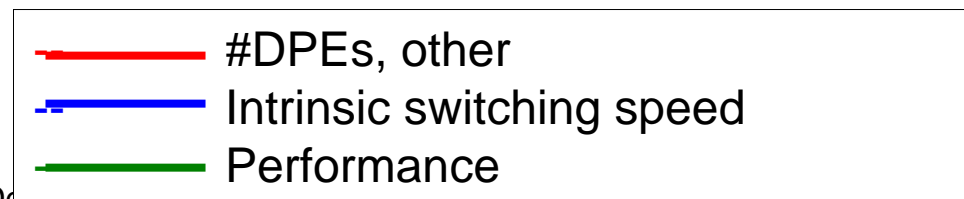
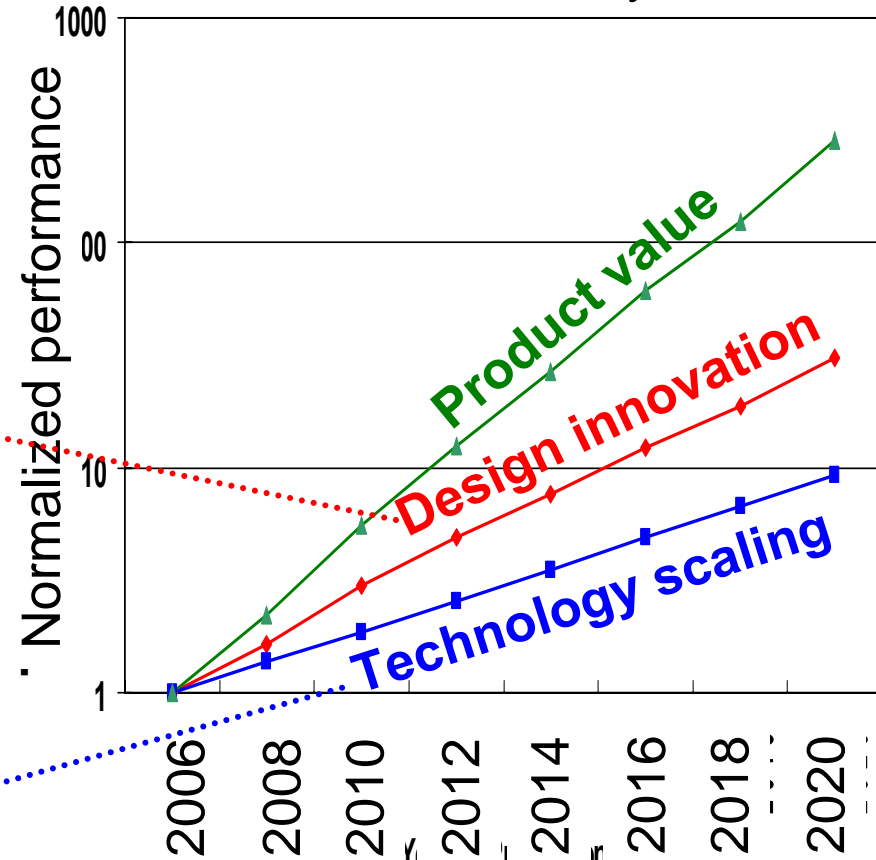
2007    2007    2006    2007    2006    2006    2007



# Market Drivers As Value Adders



Consumer stationary driver



# Driver Template

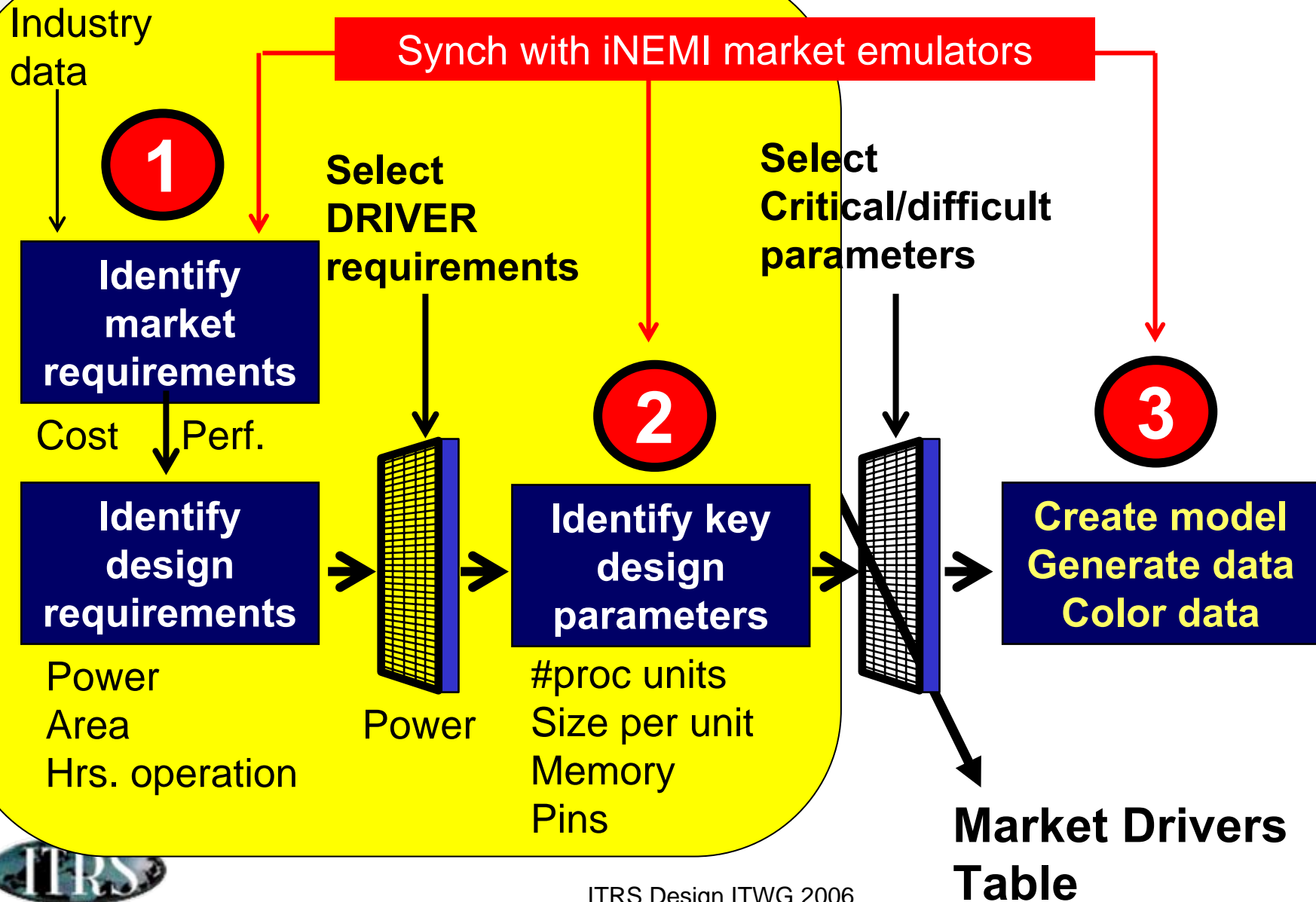
Driver parameter	Example	Units
<b>Market requirements</b> (customers AND suppliers)	Cost, Performance Energy consumption / battery life Time to market Reliability, environmental?	\$ / unit Pages / sec Hours Months Years
<b>Critical design requirements</b>	Power, Area, Time per operation / clock speed Latency / throughput / bandwidth Design productivity Hours of operation Environmental constraints	Watts, mm <sup>2</sup> ns, GHz Gbps PY/ mm <sup>2</sup> Hours <None>
<b>Critical design parameters</b>	Memory size / bandwidth # processing units, redundant units Size and clock speed/BW of each unit Number of pins	Bytes <None> mm <sup>2</sup> <None>



# System (Market) Drivers Working Table

Driver	Market ST/LT requirements	Design requirements	Design parameters
Office/PC (processor)	(General) Performance	Clock cycle MIPS, FLOPS	#of cores memory
Consumer (portable)	Energy cost	W, hours of operation (energy)	# of cores, voltage, clock cycle, etc.
Consumer (stationary)	(Media/emerg) performance	Frames/sec, FLOPS	# of SPUs, memory BW, etc., latency
Network (comms)	Bandwidth	G/Tbits/sec	# of I/Os, BW per I/O, etc.
Automotive (industrial)	Reliability Accuracy	Years, max/min T, radiation, sensing accuracy	% redundancy
Medical	Heterogeneous Integration?	Analog, digital, chemical, bio, sensors, etc.	#of (bio, chem) sensors on-chip,
Defense	Reliability (extreme)	Years, max/min T, radiation,	Redundancy

# Process For Each System Driver



# System Drivers

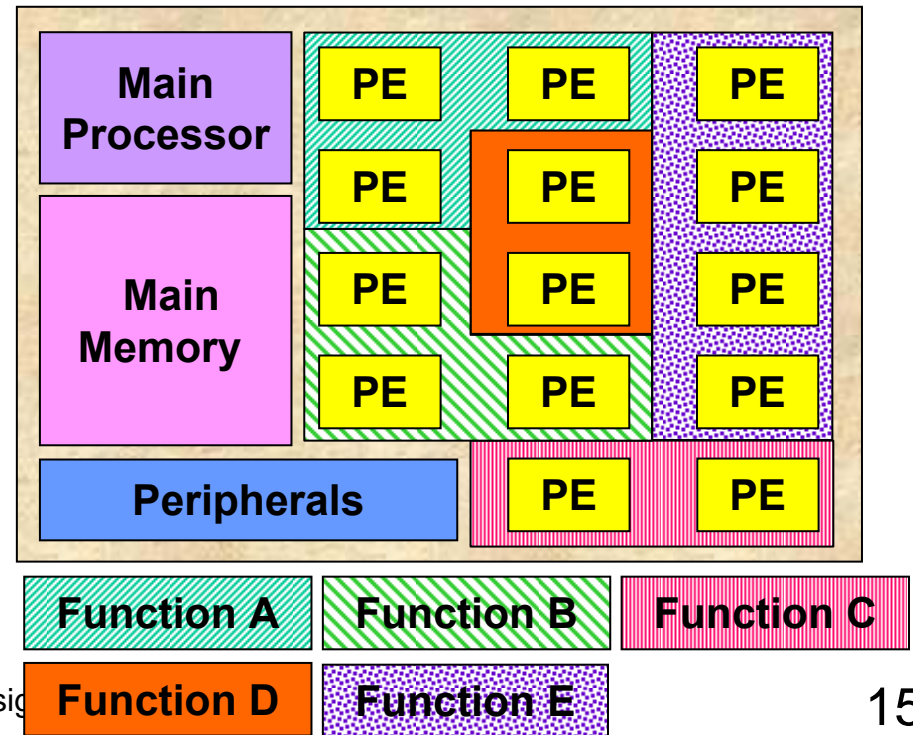
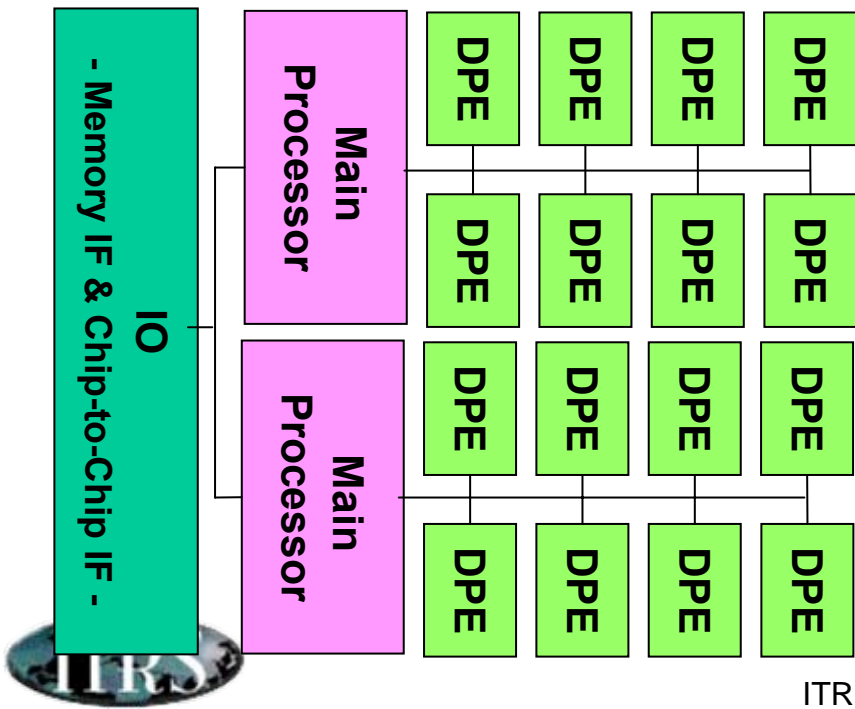
## ITRS-iNEMI *Engagement Model*

<b>Driver</b>	<b>ITRS</b>	<b>iNEMI</b>
<b>Office / large business</b>	US TWG (A. Kahng, UCSD)	Tom Pearson, Intel Erich Klink, IBM
<b>Portable / Consumer</b>	Japan TWG (Hiwatashi-san, Toshiba)	Susan Noe, 3M
<b>Networking / Communications</b>	US TWG (Joe Abler, IBM)	Tom Pearson, Intel Erich Klink, IBM
<b>Automotive</b>	EU TWG	Jim Spall, Delphi
<b>Aerospace/ Defense</b>	TBD 2007	William Murphy, Lockheed Martin
<b>Medical Products</b>	TBD 2007	Terry Dishongh, Intel

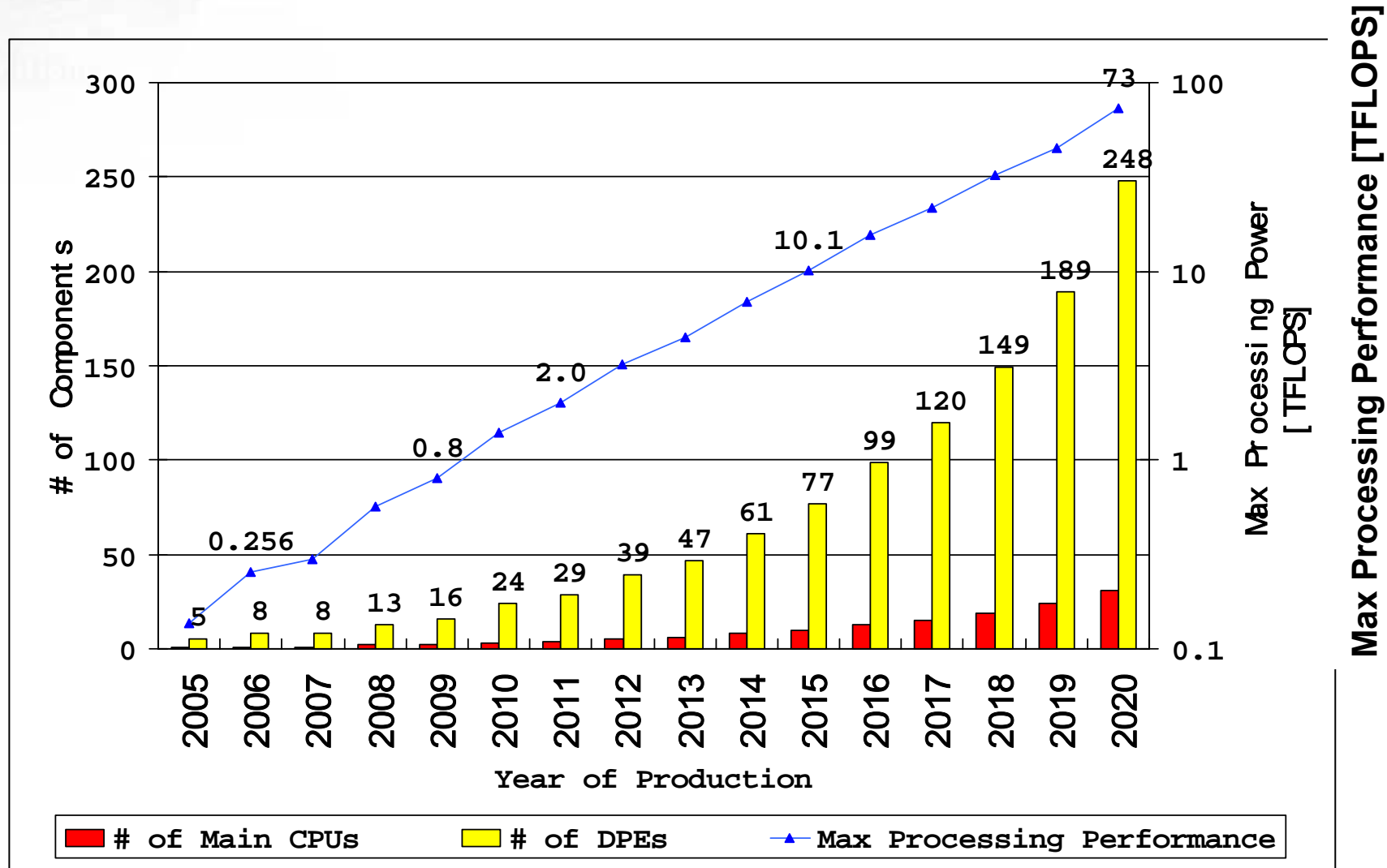


# Generic features of “SOC Consumer Stationary” Contrast with “SOC Consumer Portable”

<p><b>SOC Consumer Stationary</b></p>	<p>SOC Consumer Portable ( SOC Power Efficient)</p>
<p>Core SOC of Consumer Electronics Applications</p>	<p>Core SOC of Personal Mobile Electronics Applications</p>
<p>Many Data Processing Engines (DPE) with high processing performance to cope with high level functions implemented by SW</p>	<p>Many Processing Engines (PE) dedicated for each function to achieve low power</p>



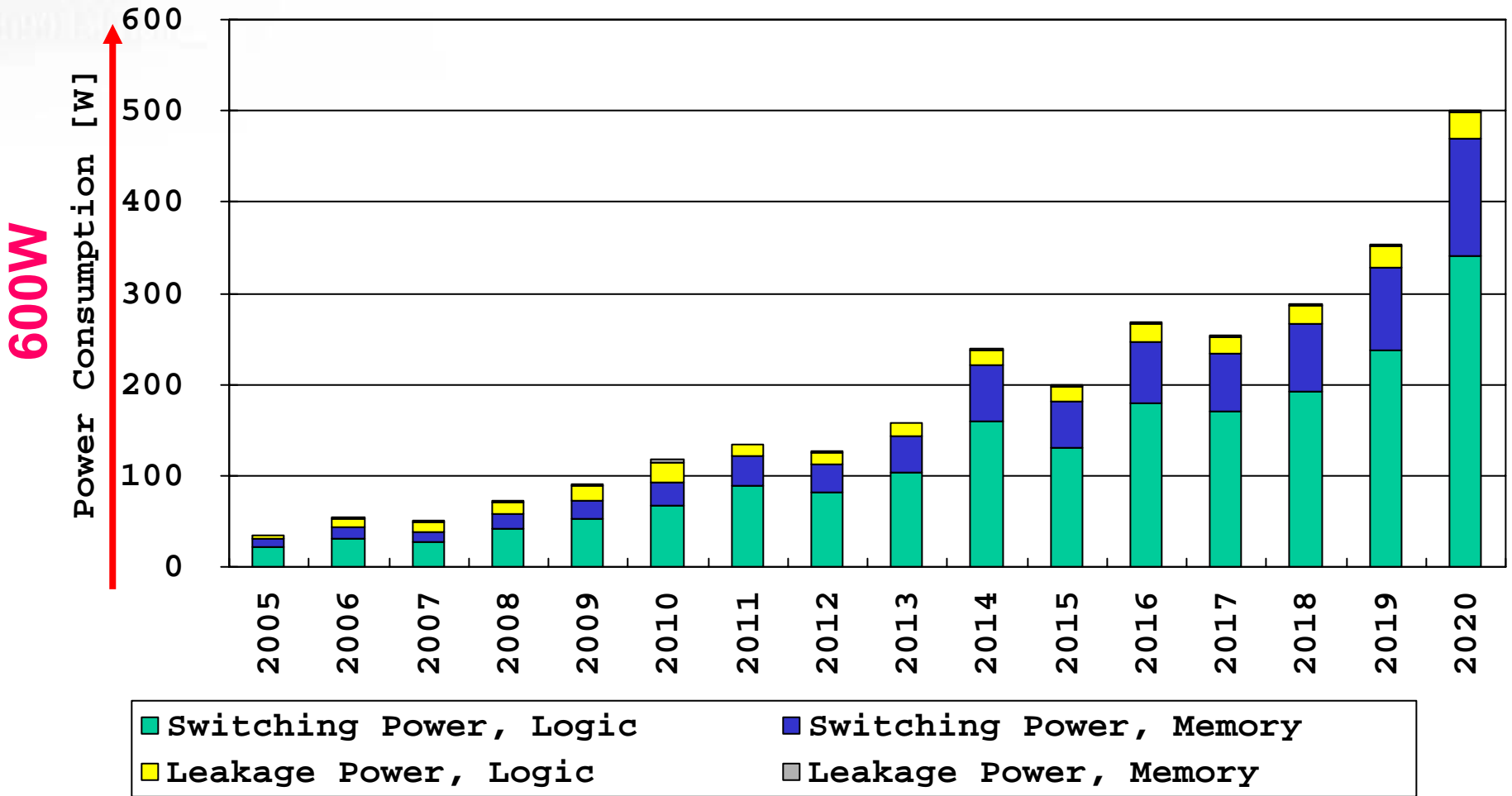
# Design Trend: # of Processors & Processing Performance

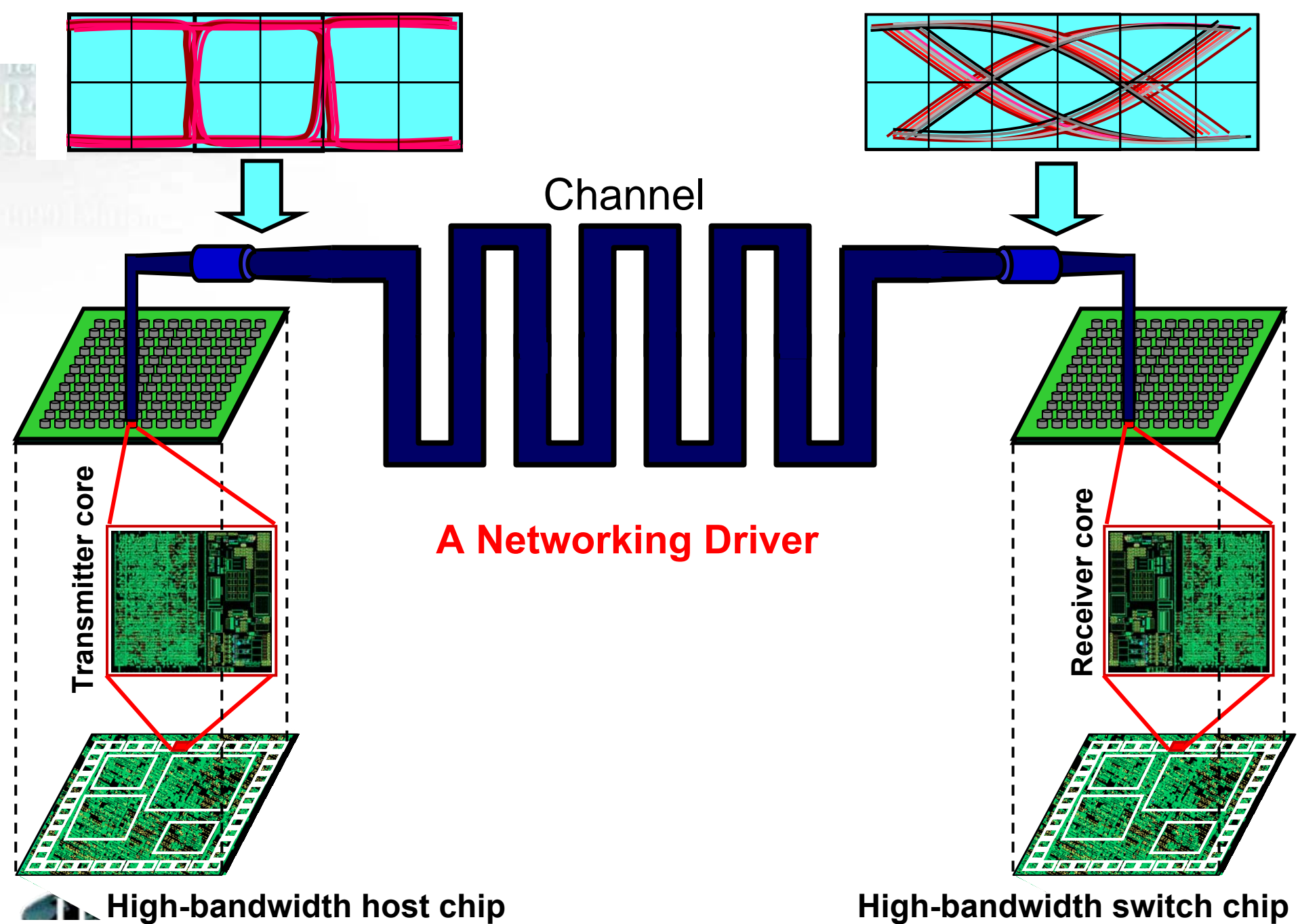


# ★ Design Trend: Power Consumption

## – SOC Total

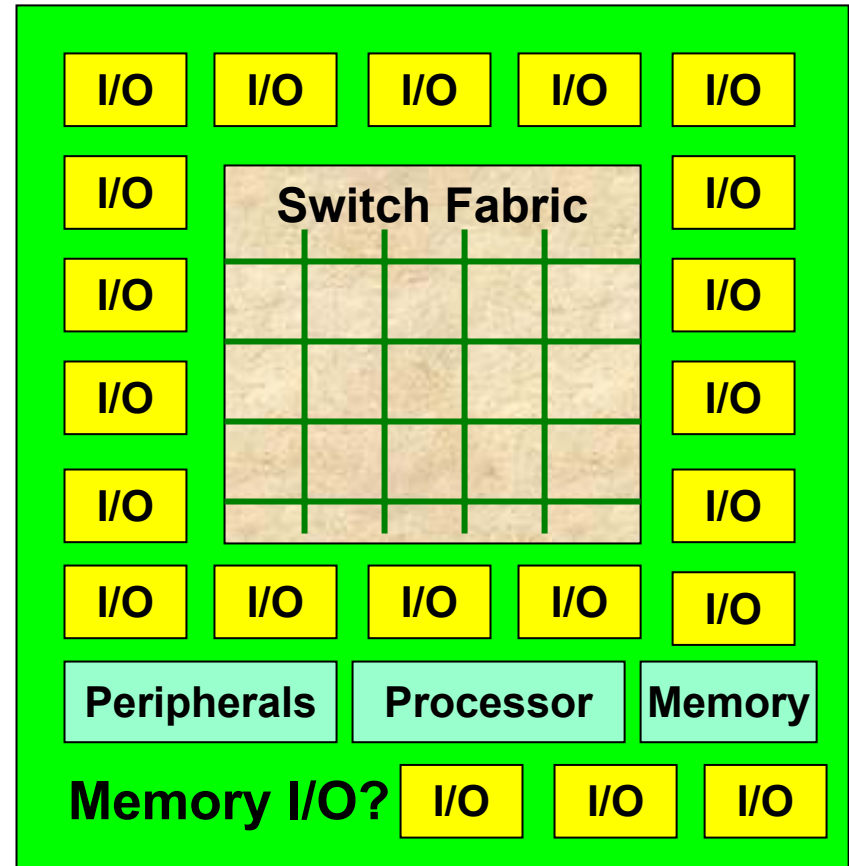
SOC total power consumption rapidly increases





# Chip Structure

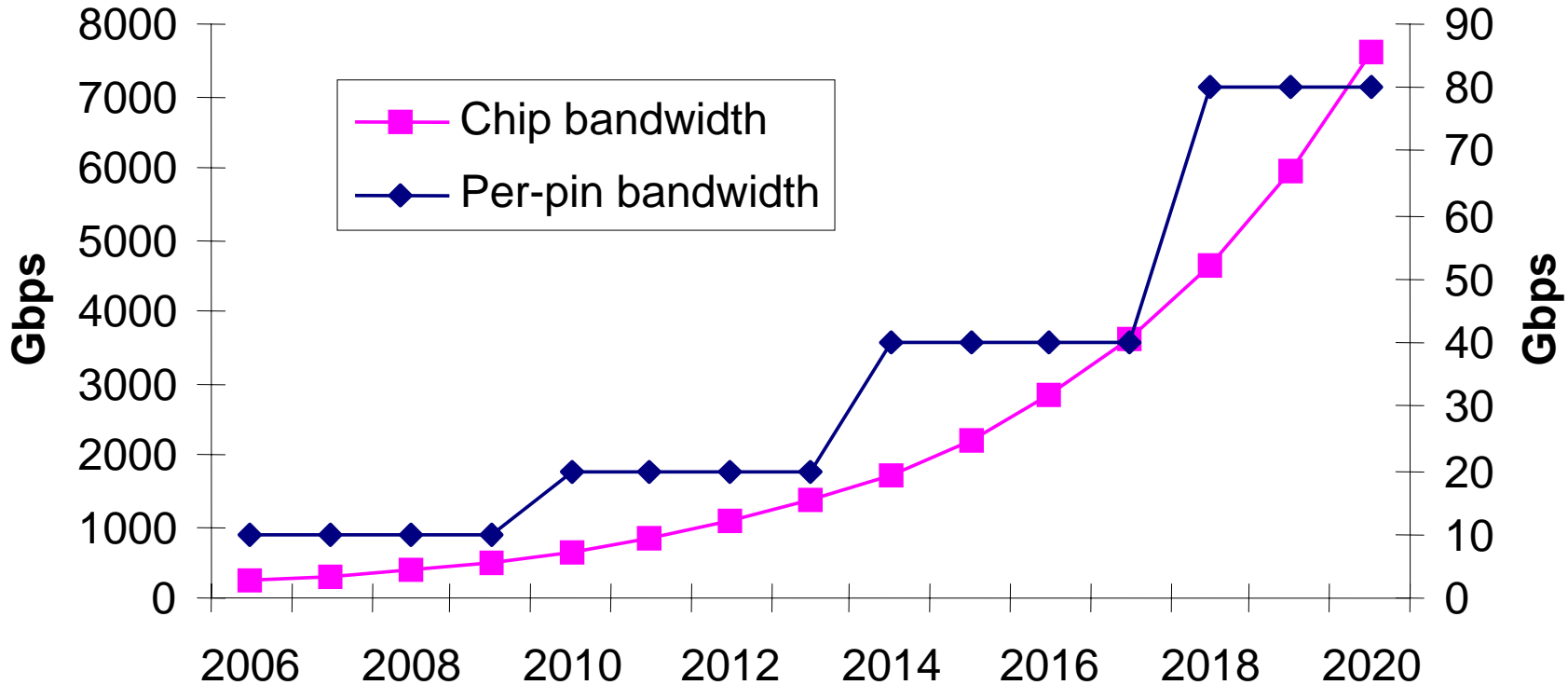
- **Very high bandwidth**
  - Key driver
- **Large size**
- **Many high-speed I/Os**
  - Mixed signal
  - Consume lots of power
- **Key components**
  - I/O
  - Switch fabric
  - Possible control processor and memory
  - CMOS technology



# Evolution of Key Parameters

## ■ Bandwidth driver

- Combination of technology scaling and bandwidth standards
- Assume I/Os dominate driver



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