2006 Test Roadmap Update

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Test TWG Membership

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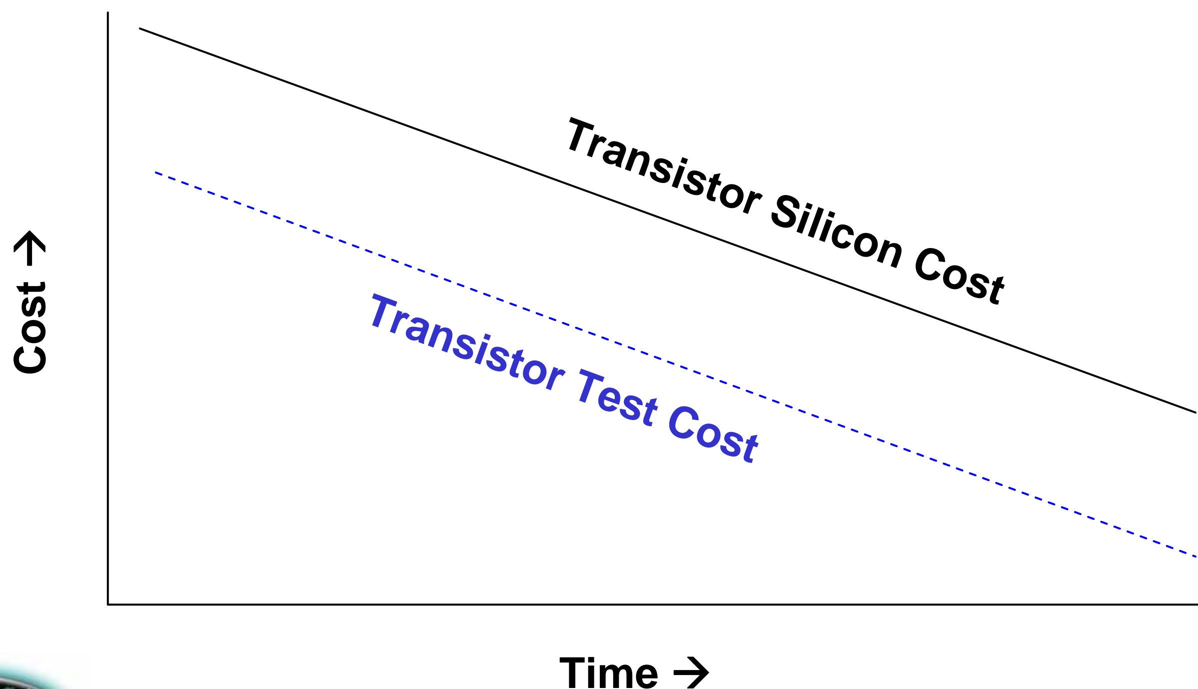
Phil Nigh	IBM	Steve Comen	TI
Jody Van Horn	IBM	Ulrich Schoettmer	Verigy
Don Wheater	IBM	Erik Volkerink	Verigy
Larry Gilg	Die Products	Yervant Zorian	Virage Logic
Peter Muhmenthaler	Infineon	Mike Rodgers	Consultant
Phil Burlison	Inovys		

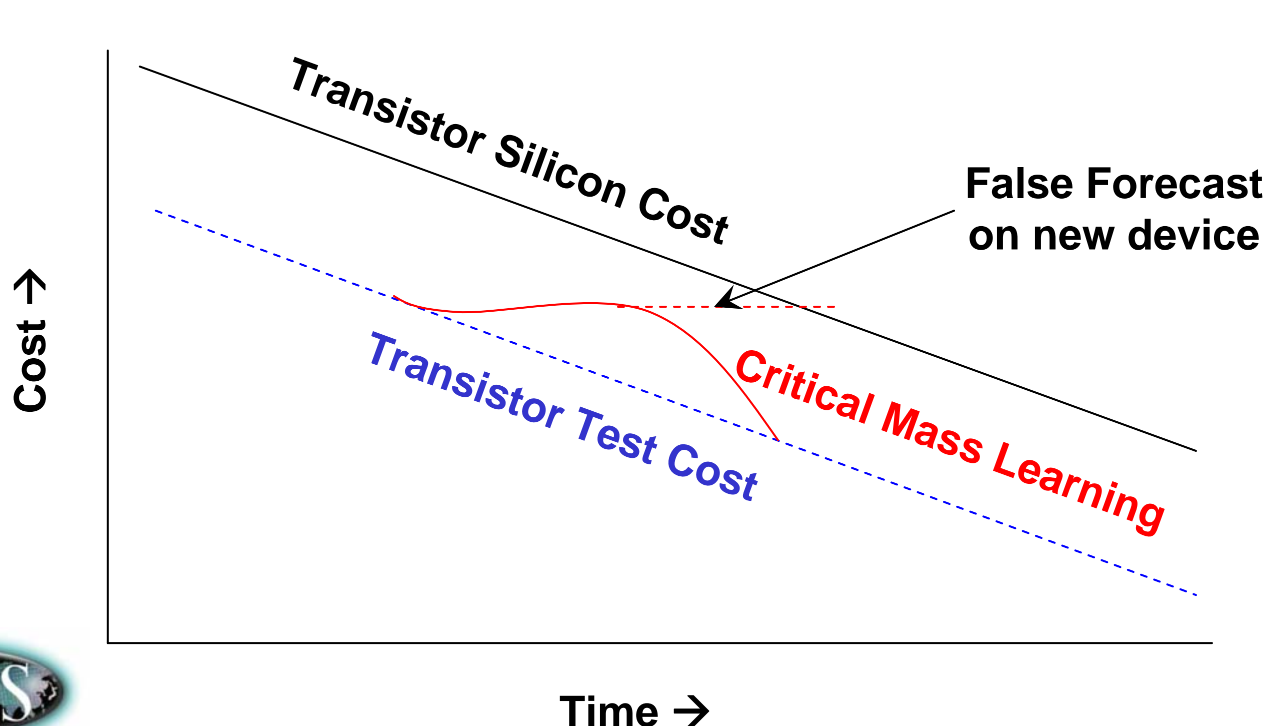
Cost of Test

- Goal: Keep test % of overall product cost flat
  - Test cost per transistor must follow Moore's Law
  - Predictable on well known devices



Cost of Test

- Test may initially lag learning curve on new devices, integrations or architectures
  - Drove mid 90's fcst of die test cost > die silicon cost
  - Low cost test methods require critical mass learning



Cost of Test Components

- Production floor test cost
  - Tester, interface, mechanical handling, consumables

- Other “test costs”
  - DFT design tools
  - Test generation and validation
  - Die area for DFT, BIST and test interfaces
  - “False Pass” customer issues due to test holes
  - Yield losses:
    - Inadequate feedback : fault detect vs. identification
    - “False Fail” due to inaccuracy, test errors
    - Mechanical damage

Economic Test Scaling

- Trading parallelism vs. performance
  - High parallelism reduces cost … but limits performance
- Managing digital logic test data volume
  - Use of compression to slow the volume growth
  - Use advantages of multi-common cores to reduce vectors
- Keeping HVM ATE performance lower than DUT
  - Reuse of slower testers necessary to control cost
  - Correct partitioning of on-DUT vs. on-tester testing
- Controlling increases in interface HW cost
  - Performance, pin count, power and reduced DUT size drive increased cost

Controlling the Cost of Test

- Test Engineers have “pushed the wall” and used evolving test methods to achieve the DPM
- DFT and BIST have reduced overall test cost when applied appropriately
- ATE cost decreasing relative to transistor count
  - Reduced pin count test methods
  - Distributed / multi-insertion test
  - High parallelism test
  - Long useful life of existing ATE

Roadmap Drivers Since 2000

- Adoption of High speed serial I/O
- Widespread use of KGD
- MCP, SOC & SIP routine
- NAND!
- Increased integration of analog and RF
- Rapid increase in test parallelism
- Litho roadmap and core voltage reduction driving tightened S/N window

2005 Changes

- Major reorganization of the Test chapter
- Consolidation of logic ATE/product tables
- Defined Test Challenges & Key Drivers
- Update of Reliability Screens
- Added new “Cost of Test” section
- Added test sockets and test interface tables
- New section on RF

2006 Update

- Minor changes made to roadmap
- Separated out Flash parallelism
  - Roadmap pulled in 2 years over NOR and DRAM
    - NAND full wafer testing likely in 2007
    - NAND Packaged test parallelism to 512
- NAND data rate increased starting in 2010
- SOC and Analog fault models delayed by two years
- Mixed signal sampling rates increased for 2007/8

2007 Drivers

- Refinement of the 2005 rewrite
  - Reduce the details in the handling roadmaps
- SOC/SIP/MCP integration and variability
- Emerging device test
- Test of Fault tolerant devices
  - Self error correction, BISR, System level tolerance
- KGD test challenges and opportunities
- Limits of high parallelism test

General Test Drivers

- Device Trends
  - Non-deterministic high speed interfaces
  - Increasing integration (SOC, MCP, SIP, 3D pkg)
  - Package form factor & electrical / mechanical characteristics
  - Lower voltages, power complexity and management modes
- Integration of Technologies / Materials in platforms
  - RF, Analog, MEMS, Optical, High/Low k dietetics
- Increasing Test Process Complexity
  - Customer specific device customization
  - Multi-insertion test to optimize cost
- Bottom Line Constraint is Test Cost
  - Affordability with maximum allowable DPM

Yield Learning, FA, and Diagnosis

- Physical FA hitting the wall
  - Significant TPT, technology, cost, & results barriers
- Advanced SW diagnostics needed for physical FA
  - Must quickly ID, locate, and accurately distinguish defect types
  - …Analog Failure Analysis remains a gap
- DFT essential to localize failures
  - Improves data collection efficiency
  - Reduces design complexities associated with test
- Litho roadmap evolving defect types
  - Novel fault models needed to address emerging defects

DUT Interface

- The DUT interface is becoming a larger portion of the overall test cell cost
  - Probecard & DUT adapter/kit cost nearing prober/handler cost
- Increased parallelism may result in lower test cost…
- …but has negatives
  - Increased interface cost and complexity
  - Reduced interface performance
  - Reduced interface reliability
  - Increased DUT loading