

Front End Processes 2006 ITRS

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Hsinchu

2006 FEP ITWG Team

- US:** Raj Jammy, Jeff Butterbaugh (presenter), Larry Larson, Mike Walden, Mike Goldstein
- Japan:** Ichiro Mizushima, Masaharu Watanabe, Masaaki Niwa
- Europe:** Mauro Alessandri, Wolfgang Mueller, Chris Stapelmann
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- Taiwan:** Simon Jang, Vincent Chang



2006 FEP Sub-TWGs and Chairs

- **Starting Materials**
 - Mike Walden(US), Mike Goldstein(US)
- **Surface Preparation**
 - Joel Barnett(US), Karen Reinhardt(US), Chris Sparks(US)
- **Thermal/Thin Films/Doping**
 - Carl Osburn(US), Hsing-Huang Tseng(US)
- **Etch**
 - Greg Smith(US), Gabe Gebara(US)
- **Stacked DRAM**
 - Michitaka Kubota(JP), Hideaki Fujiwara(JP)
- **Trench DRAM**
 - Wolfgang Mueller(EU)
- **Flash**
 - Mauro Alessandri(EU)
- **PCM**
 - Mauro Alessandri(EU)
- **FeRAM**
 - Jeffrey Cross(JP)



2006 FEP - Update Highlights

- **Starting Materials:**
 - Minor changes
- **Surface Prep:**
 - Minor changes to color coding
 - Red to Striped Yellow (work arounds) for Si/SiO₂ loss
- **Thermal/Thin Films/Doping:**
 - Push out high-k/metal gates (2010) and FDSOI (2010)
- **Etch:**
 - Added “other etch sources” section to potential solutions
- **Stacked DRAM:**
 - Proper correlation of k-value with materials
- **Trench DRAM:**
 - NO will be extended down to 70nm
- **Non-volatile memories**
 - Flash – STI aspect ratio requirements between NAND and NOR
 - PCRAM – Update requirements for phase change materials
 - FeRAM – additional notes about new materials



Starting Materials

2006 Updates: Tables 67a and 67b

- **Minor changes to 2005 ITRS**
 - Corrected colorization of particle density (Yellow to White in 2011)
 - Corrected colorization of particles per wafer (Yellow to White in 2011)
- **No other changes are applicable for the 2006 update**
- **Additional Emerging Materials presentations have been reviewed and discussed during 2006 – these will be taken into account for the 2007 publication**



Starting Materials

Plans for 2007

- Consider ERO (edge roll-off) model and identify appropriate related metrics for potential table insertion - cross-TWG discussions with Litho
- Revisit bulk Si and SOI thickness uniformity and flatness metrics – Litho TWG has indicated that current metrics may not meet requirements
- Revisit front and back surface / edge particles including cross-TWG discussions with Surface Prep - assess metrology issues
- Continue examination of 450mm including wafer deformation impact on metrology handling considerations
- Multiple materials solutions and segmentation detracts from usefulness of generic wafer parameters applicable for today's broad product mix
 - Simple SOI table may increase significantly and models require revalidation in the face of expanding device applications (i.e. embedded DRAM on SOI, 1T DRAM, etc.) and continued use of partially depleted structures
 - Emerging Materials may require separate wafer parameter list (i.e. strained Si directly on insulator)
- Simplify table footnotes for improved readability / comprehension



Surface Preparation 2006 Updates

- No Numerical Changes for 2006 Update
 - No typos, no misprints, no complaints
- Color Change for Silicon and Silicon Oxide Loss
 - From **RED** to **STRIPED YELLOW**
 - Based on information presented at conferences
- Potential Solutions
 - Implementation of supercritical fluids pushed out



Surface Preparation Plans for 2007

New Problems

- Proper Incorporation of water mark metric
- Considerations regarding cleaning and measuring of Vertical surface, SiGe and III-V surfaces
- High Aspect Ratio Drying
- Corrosion of Metal Gate / New materials
- Contact cleaning metrics

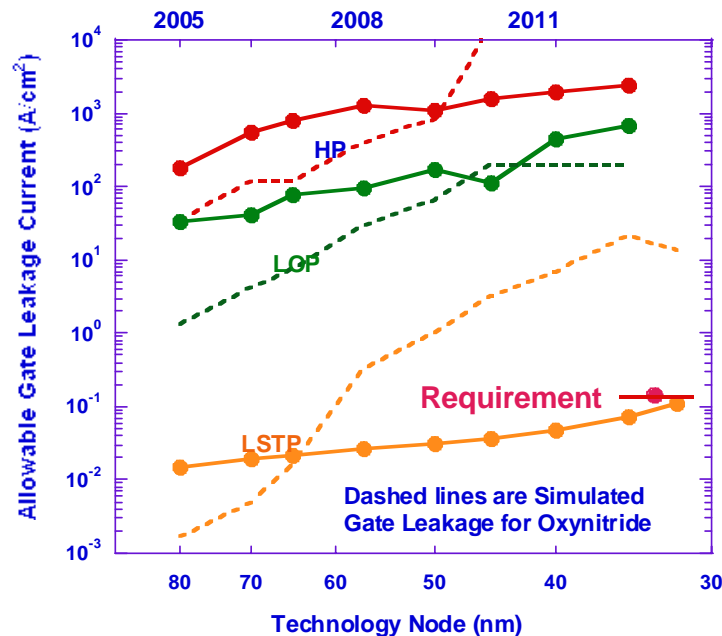
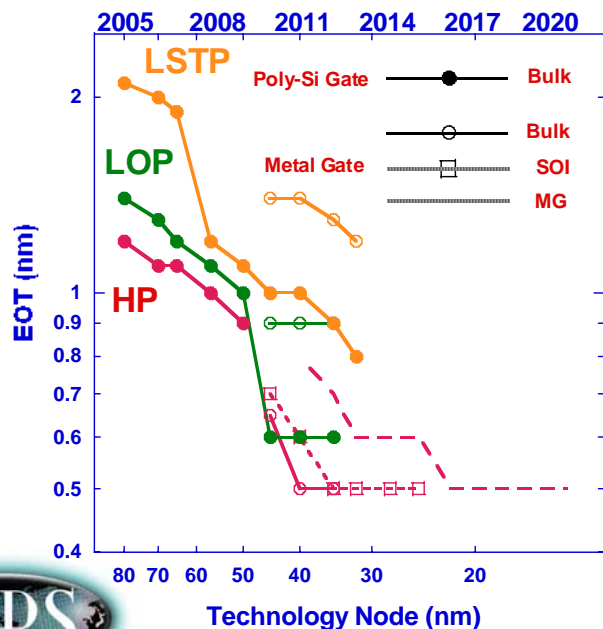
Continuing Issues

- Defect Density/Particle Models - Need more input from IC manufacturers
- Si Loss - Is 0.2\AA reasonable? Need standardization of Measurement
- Determination of Bevel Edge and Back Surface Particles Specifications
- How do C and O contamination metrics differ for High-k vs. SiON vs. Si
- Re-examine metals and mobile ion specs and classifications
 - SOI
 - other ions? – e.g. SO_4^{2-}

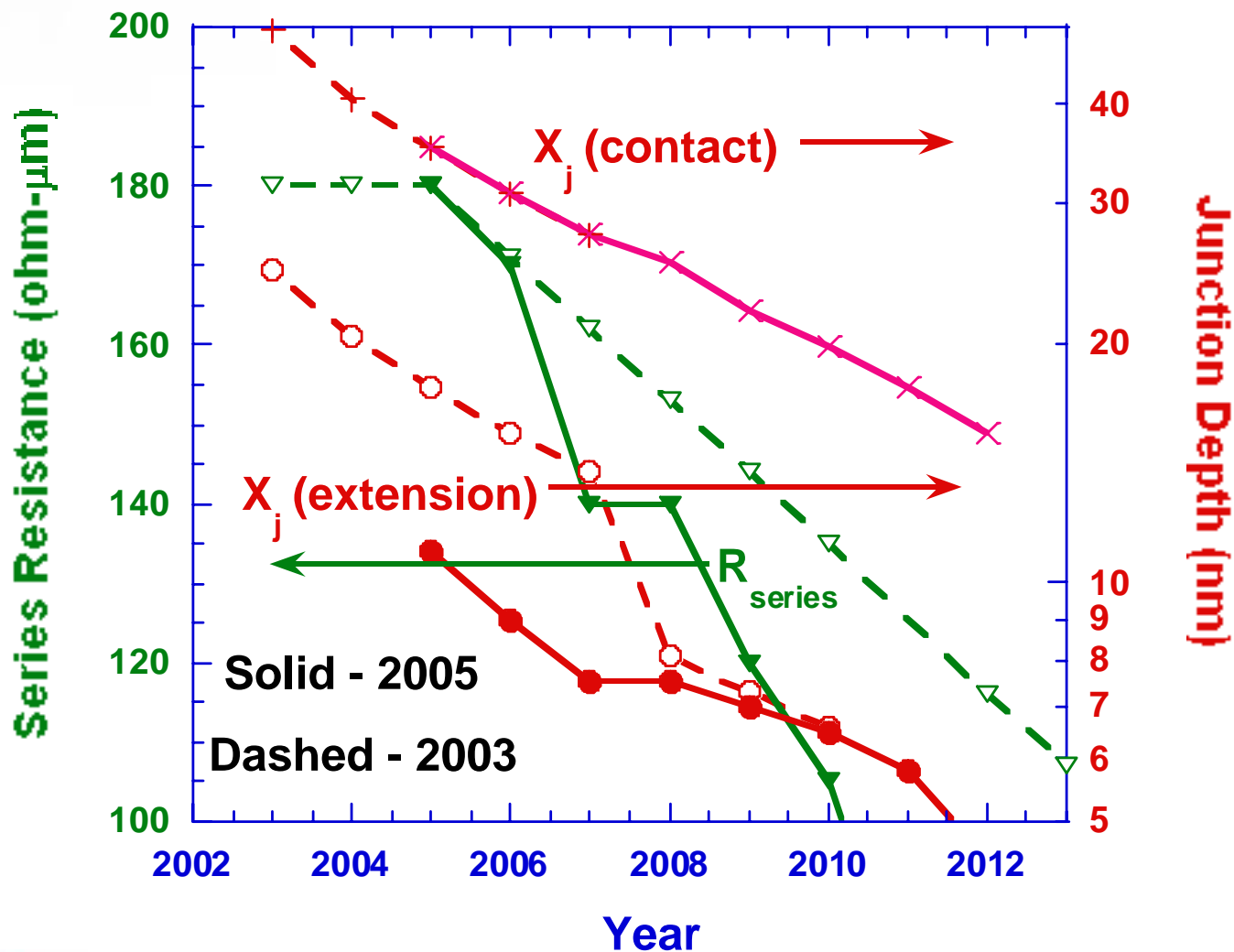


Thermal /Thin Films /Doping 2006 Updates

- Date for High-k/ Metal Gate for High Performance Moved Out from 2008 to 2010
- Date for Expected First Shift from Bulk to FDSOI Now Expected to be 2010, Rather Than 2008
- 2005 Reductions in Junction Depth and Series Resistance Remain Problematic (Unrealistically Aggressive) and are a Candidate for Revision in 2007



Comparison of 2003 and 2005 ITRS Junction Parameters



Requirements Have Dramatically Increased



Thermal/Thin Films/Doping Plans for 2007

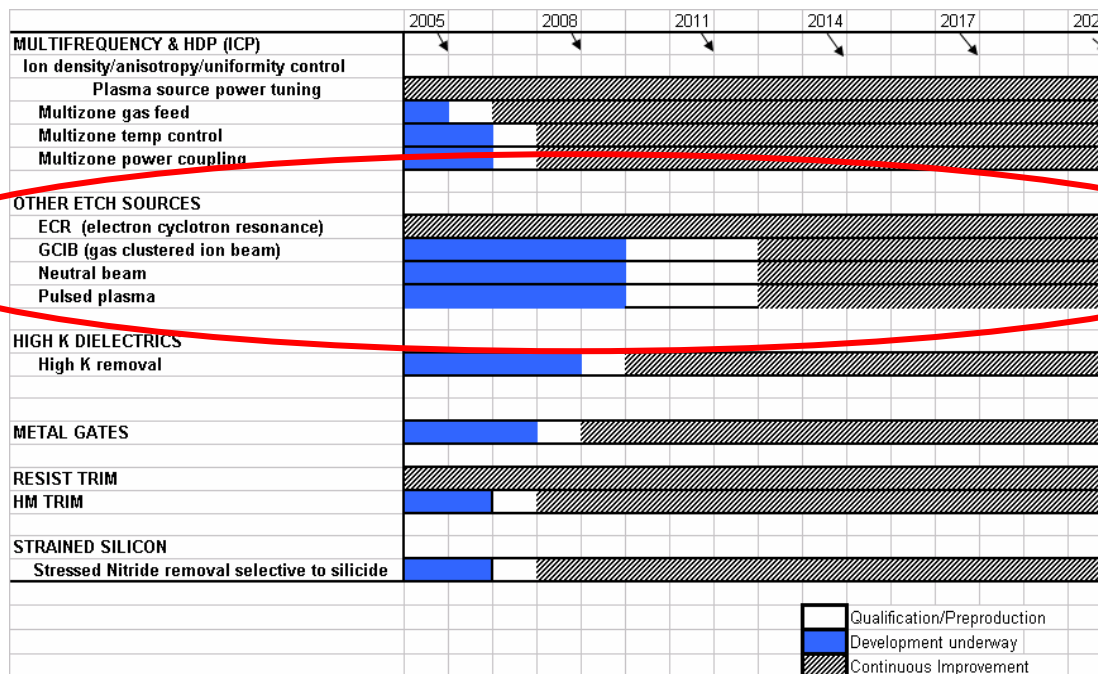
- **Ongoing Need to Re-Invigorate SubTWG Membership**
- **Assist PIDS in Complete Review of Design Points for Bulk, FDSOI, and Multi-Gate – How do we account for design innovations?**
 - Bulk was Extended Two Years out to 2010 (2006 update)
 - Evaluate Alternate Scenarios for Bulk → FDSOI → MG; SiON → Metal/High k
- **Evaluate Progress in Mobility Enhancement**
 - Update Enhancement “Requirements” – strain, orientation, body thickness
 - Consider Non-Si Channel Materials
 - Assess Impact on Gate Stack Requirements
- **Address Trench Isolation Limits**
- **Impose Gate Leakage Cap (from PIDS) on LSTP**
- **Update Physical Gate Lengths for Each Year (Hopefully without Requiring More Aggressive EOT or X_j Scaling)**
- **Work With PIDS to Provide Relief (Better “Share the Pain”) on Series Resistance, Both Extension Junction X_j - R_s and Contact Resistance**
- **With Starting Materials, Unify Treatment of FDSOI Thicknesses and Tolerances (Starting Materials vs Final Thicknesses)**



Etch

2006 Updates

- %CD variation line in (design) Table 18a changes from 10% to 12%
- **MISSED: “Etch Potential Solutions Table” for Fig. 60**
 - intended to update this figure, but mistakenly omitted from update – will update in 2007



Etch

Plans for 2007

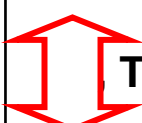
- **Review resist aspect ratio requirements for trimming, recommend inclusion of line in table.**
 - Resist collapse during trim is becoming a problem.
 - May drive multilayer resist or hard mask
 - Need to examine process parameters from litho develop and trim
 - Need to explicitly call out hard mask parameters in the table
- **Lg: scaling and CD uniformity and CD tolerance**
 - Litho improvements allow for CDU to go down from 3.6 to 3.2 nm
 - Restricting the pitch will help in improving CD uniformity
 - Multiples of narrow pitch across the chip would help litho reduce the CDU to 1.6 nm from 3.2 nm (3σ): DFM solution
 - LER – who defines? Litho-FEP-Design-PIDS? Metrology?
- **Gate Length Survey sent out in October**
 - very poor response!! – need better response to be meaningful



Stacked DRAM

2006 Updates

- No change in Table 70 and text.
- Correction in Fig. 61 is desirable to match the timing of the change of material and dielectric constant in Table 70.
 - Combination of high-k dielectrics may be used to achieve desired k

<i>Year of Production</i>	2005	2006	2007	2008	2009	2010	2011	2012	2013
DRAM M1 ½ pitch (nm)	80	70	65	57	50	45	40	36	32
<i>Dielectric constant</i>	40	50	50	50	50	50	60	60	60
Capacitor Dielectric Material	Al ₂ O ₃ , HfO ₂ , Ta ₂ O ₅			 Ta ₂ O ₅ , TiO ₂			Ultrahigh k, new materials		
Capacitor Dielectric Material	Al ₂ O ₃ , Ta ₂ O ₅	Al ₂ O ₃ , HfO ₂ , Ta ₂ O ₅ , TiO ₂ , ZrO ₂					Ultrahigh k, new materials		

WAS

IS



Stacked DRAM Plans for 2007

- Incorporate PIDs DRAM survey results in 2007 FEP
- Discussion and modification of numbers related with structure in table 72a such as capacitor height and capacitor area, EOT and dielectric constant, electrode material, etc., will be needed by considering the realistic limitation of cylindrical structure
 - A/R which does not causes SN bridge is less than 12
 - SN height can be determined by A/R 12

Year of Production	2005	2006	2007	2008	2009	2010	2011	2012	2013
DRAM λ Pitch (nm) [A]	80	70	65	57	50	45	40	36	32
Cell size factor α [B]	8	8	8	6	6	6	6	6	6
t_{eq} at 25fF (nm) [C]	1.8	1.4	1.1	0.90	0.80	0.60	0.60	0.50	0.50
Dielectric constant	40	50	50	50	50	50	60	60	60
SN height (μm)	1.4	1.4	1.2	1.6	1.8	1.9	2	2	2
Total capacitor area (μm^2)	1.38	1.22	0.62	0.55	0.55	0.52	0.48	0.43	0.38



Trench DRAM 2006 Updates

- Capacitor dielectric
 - NO extended down to 70nm.
 - High k materials such as Al_2O_3 or HfSiON will be used from 65nm onwards.
- New integration schemes to be introduced for 40nm
 - reduces temperature budget for the cell capacitor.
 - allows more aggressive scaling of the capacitance equivalent oxide thickness (CET).
 - trench aspect ratio can be kept at less than/equal to 100 down to 28nm.

Plans for 2007

- Discuss and consolidate the table parameters with Stacked DRAM
- Review with Stacked DRAM the roadmap beyond 20nm
 - Can an evolutionary roadmap be sustained beyond 20nm?
 - Have new cell structures to be included in the roadmap?



Flash Memory

2006 Updates

- Add requirements for STI isolation

<i>Year of Production</i>	2005	2006	2007	2008	2009	2010	2011	2012	2013
Flash technology	80/76	70/64	65/57	57/51	50/45	45/40	40/36	36/32	32/28
STI Filling Aspect Ratio Min-Max		3.0-4.7	3.2-5.3	3.5-5.8	3.9-6.4	4.2-7.1	4.6-7.8	5.0-8.6	5.5-9.7

Plans for 2007

- Discuss the end date for the roadmap of stacked gate Flash architecture and agree with PIDS
- Review of the evolution / requirements for tunnel and interpoly dielectrics
- Separation of NAND and NOR for STI requirements
- Implementation of more new architectures to be discussed, i.e. nanodots, nitride floating gate, etc.
 - ERD considers these options to be mature for transfer to PIDS and FEP



Phase Change Memory (PCM)

2006 Updates

- Add first requirements for phase change material

<i>Year of Production</i>	2005	2006	2007	2008	2009	2010	2011	2012	2013
PCM technology		70	65	57	50	45	40	35	32
Conformality (%)		>30	>30	>60	>60	>60	>90	>90	>90
<i>T</i> retention (°C)		>85	>85	>100	>100	>100	>125	>125	>125

Plans for 2007

- Review and expand requirements for phase change material
- Add requirements for heater material
- Definition of appropriate production volumes/year



FeRAM

2006 Updates

- No Change in Tables
- A few comments related to the 2005 text:
 - For clarification
 - Additional description about new materials

Plans for 2007

- Ongoing Survey of Commercial FeRAM Production Status
- Definition of Production Year Appropriate for FeRAM
 - 10kp/month volume by 2 companies (as with DRAM) ?
- Common Half Pitch Standard is Desirable to be applied also to other new memories
- Scaling Rate of FeRAM is Subject of Ongoing FEP/PIDS Discussion



2007 FEP – Summary of Current Plans

- **Starting Materials:**
 - Wafer shape interactions with immersion Litho
 - Possible expansion of SOI tables
 - Emerging materials may require separate wafer parameter requirements
 - 450mm considerations . . .
- **Surface Prep:**
 - May need to consider “application specific” metrics for materials loss and defectivity (e.g. pre-gate, post S/D, etc.)
 - Continued examination of back surface particles metric
- **Thermal/Thin Films/Doping:**
 - All models/assumptions to be revisited for projections and timing
 - Junction depth and series R parameters unrealistically aggressive – to be revisited
- **Etch:**
 - Review resist aspect ratio requirements for resist collapse during trim
 - Survey of actual physical gate length – trim, tolerance & uniformity



2007 FEP – Summary of Current Plans

- **DRAM:**
 - Coordinate trench and stack scaling parameters
- **Flash:**
 - Discussion on end of stacked gate flash roadmap and new cell architectures
 - Deep review of IPD and tunnel dielectric requirements/scaling options
 - Separation of NOR vs NAND scaling and impact on STI aspect ratio
- **PCRAM:**
 - Review and expand requirements for phase change and heater materials
 - Discussion on production volumes/metrics and definition of half pitch standards
- **FERAM:**
 - Continued discussion on production volumes/metrics and definition of half pitch standards

