

# **PIDS Key Results and Issues**

## **PIDS Technology Working Group**

**ITRS Public Meeting  
HsinChu Taiwan  
December 5, 2006**



# PIDS Roster

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# Outline

- *Scope and Subcategories*
- **Non-Volatile Memory**
- **DRAM**
- **Logic**
- **Reliability**



# **PIDS Scope**

- **PIDS = Process Integration, Developments, and Structures**
- **Main concerns**
  - **MOSFET, memory, and passive devices and structures**
    - **Device physical and electrical characteristics and requirements**
  - **Broad issues of device and circuit performance, density, and power dissipation, particularly as they drive overall technology requirements**
  - **Reliability**



# PIDS Subcategories

- **Logic**
  - High-performance
  - Low-power (mobile applications)
- **Memory**
  - DRAM
  - Non-volatile memory (NVM)
- **Reliability**



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# NAND Flash Roadmap: F

- F = half-pitch
  - DRAM: Metal 1
  - Flash: Poly
- Flash memory scaling has pulled ahead of DRAM scaling

	2005	2006	2007	2008	2009	2010
<i>05 NAND Flash</i>	76	64	57	51	45	40
<i>03 Flash Roadmap</i>	80	70	65	55	50	50
<i>05 DRAM 1/2pitch</i>	80	70	65	57	50	45

	2011	2012	2013	2014	2015	2016
<i>05 NAND/AND Flash</i>	36	32	28	25	23	20
<i>03Flash Roadmap</i>		39	35		28	
<i>03DRAM1/2pitch</i>		36	32		25	



## Non-Volatile Memory (con't.)

- **No interim change for NVM table for 2006**
- **Major revisions considered for 2007 NVM**
  - **Accelerating the scaling roadmap, to reflect recent PR**
  - **Separate NOR and NAND applications**
    - **Subsection including floating gate and nitride storage device**
  - **(Emerging\*)-NVM in a third categories**
    - **PCRAM, MRAM, FeRAM, (Nanocrystals\*), (R-RAM\*)**

**\*: Under discussion**



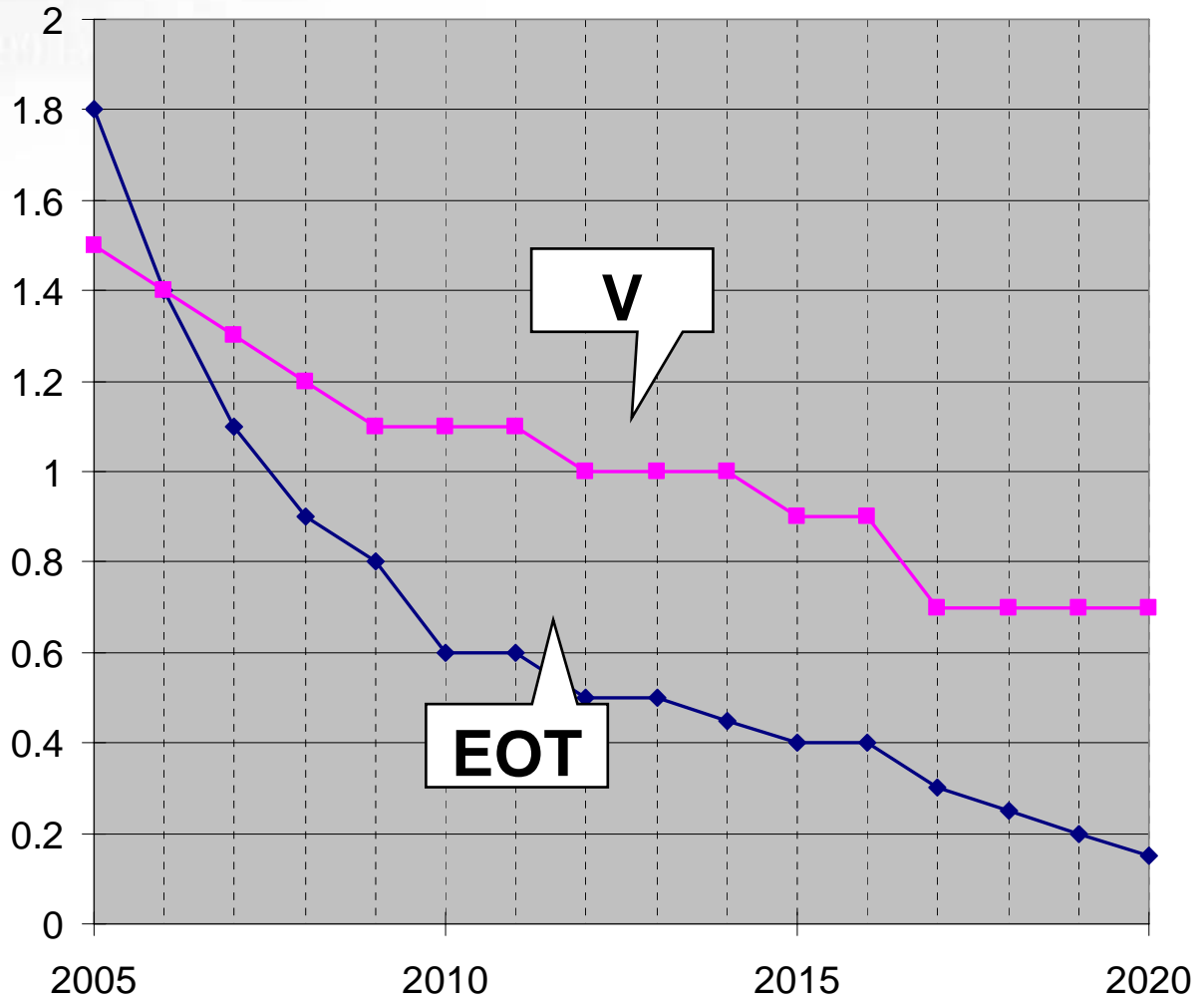
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## DRAM

- **Scaling unchanged from 2003**
  - **DRAM half-pitch (F) : 3 year cycle**
    - 65nm in 2007, 45 nm in 2010
- **Other results**
  - **$a=(\text{cell area})/F^2$ : a=8 through 2007, a=6 thereafter**
  - **Array Area efficiency (% of chip area taken up by storage cells): 63% through 2007, 56% thereafter**
  - **STC storage node dielectric: the same as 2003 ITRS**

# Scaling of DRAM Storage Dielectric

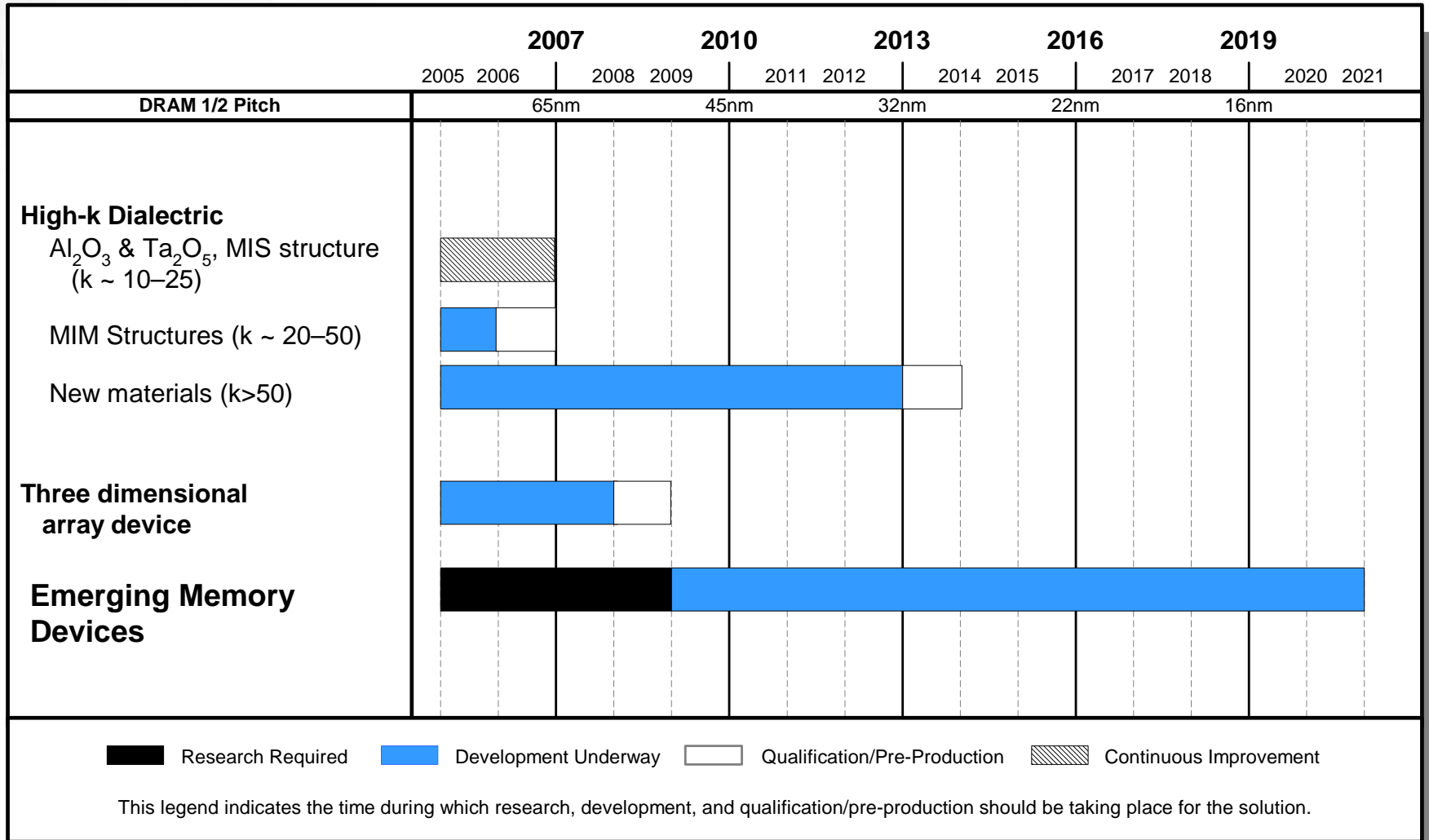


◆ DRAM storage node cell dielectric: equivalent physical thickness, EOT nm  
■ DRAM storage node capacitor voltage, V

Preliminary Results



# Potential Solutions: DRAM



# Capacitorless Floating Body Cell DRAM Proposal for 2007 ITRS Consideration

- **This is a one-transistor (1T) SOI NMOSFET: in contrast to standard approach with one capacitor and one transistor (1T1C)**
  - **Signal charge is holes injected into floating body of MOSFET, rather than charge on storage capacitance**
  - **Advantages**
    - **Potential for reduced cell area (no storage capacitor needed)**
    - **Potentially scalable like a transistor**
    - **Fabrication is very consistent with SOI Logic processing technology: advantageous for embedded memory**
  - **Will be considered for inclusion in 2007 PIDS DRAM**

## DRAM

- **2007 consideration based on survey:**
  - DRAM half pitch (M1): same as 2005 roadmap after 2007
  - DRAM product area efficiency: 1 year delay vs. 2005 roadmap
  - Cell factor: '6' start from 2006, 2 years pull in vs. 2005 roadmap
  - Capacitor Teq: same to 2010
  - Capacitor structure: cylinder and pedestal are same to 2012
  - Capacitor materials:  $\text{Ta}_2\text{O}_5 / \text{TiO}_2 \Rightarrow \text{ZrO}_2 / \text{HfO}_2$  from 2008
  - Adding SOI based 'floating body cell' (FBC)

# Outline

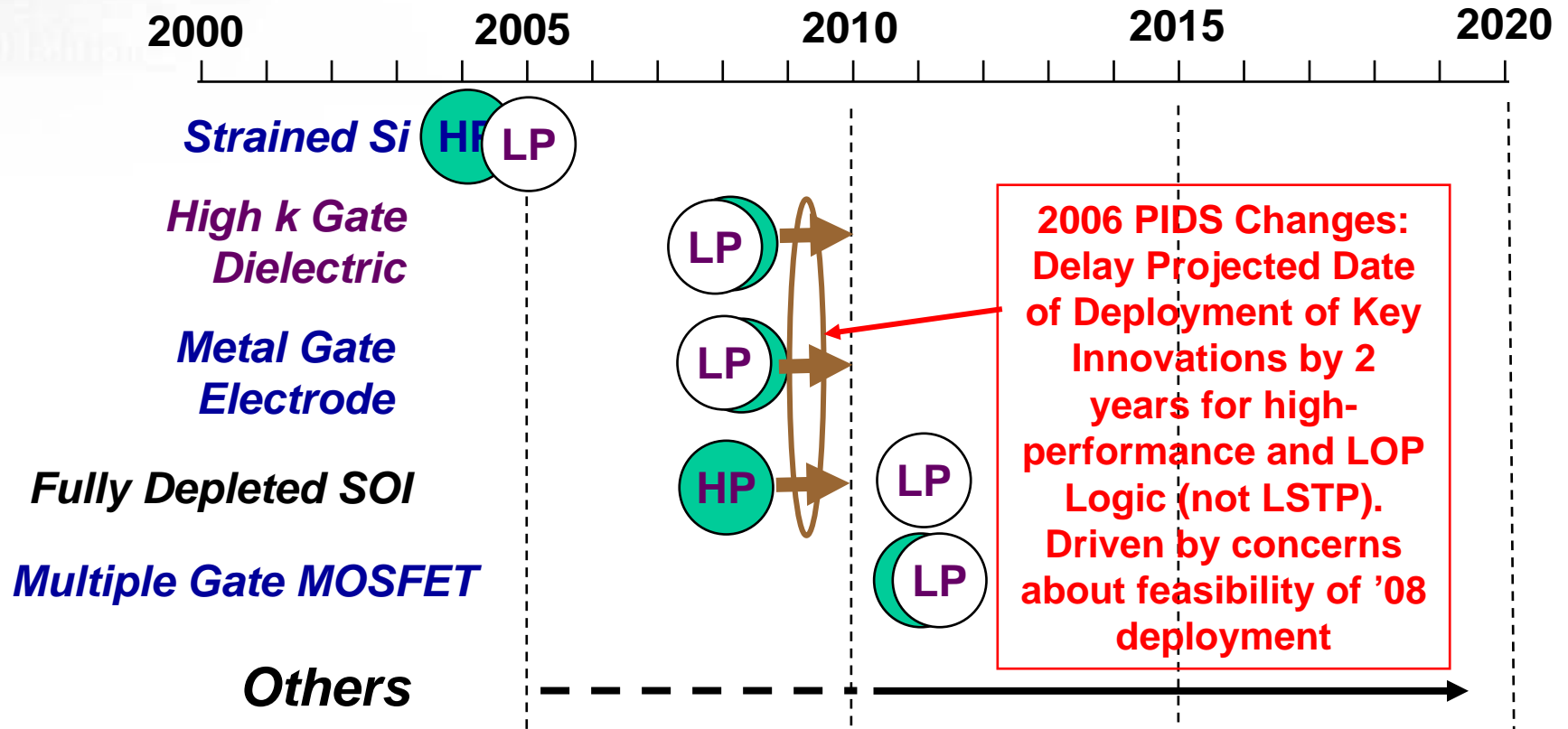
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- *Logic*
- **Reliability**

# Logic: Scaling Approach and Categories

- **MASTAR (detailed analytic device model from STM and corporate partners) was used**
  - MASTAR has been extensively verified against literature and other data
  - Initial choice of scaled MOSFET parameters is made
  - Using MASTAR, MOSFET parameters are iteratively varied to meet ITRS targets → examine tradeoffs
- **Types of Logic**
  - High Performance (HP) (e.g., MPU): target is historical 17%/year transistor performance increase
  - Low Power (for mobile applications): target is specific, low level of leakage current
    - **Low Standby Power (LSTP):** very low leakage; for lower performance, consumer applications (e.g., cellphone)
    - **Low Operating Power (LOP):** low dynamic power, rel. high performance (e.g., notebook computer)

# The “CMOS Change Crunch” Multiple, Big Technology Innovations Over Next 5 Years

*First Year of “Volume Production”*

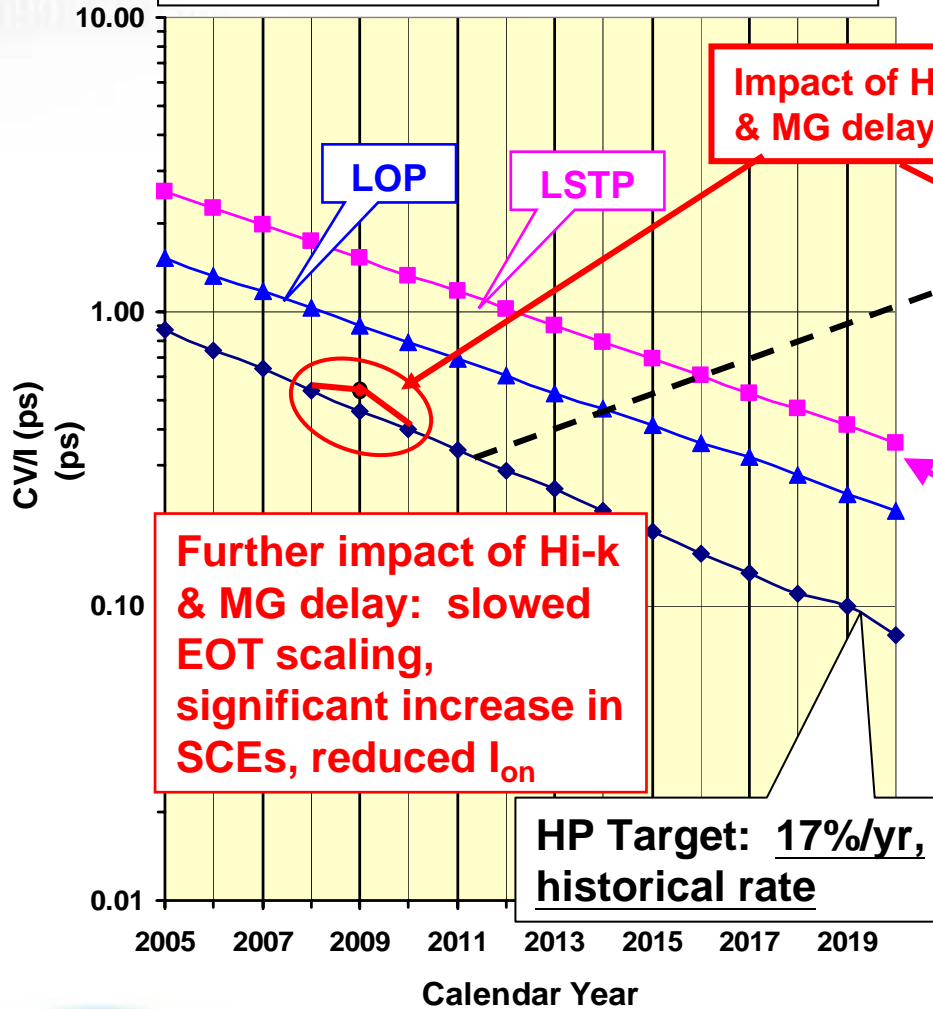


Driver: (HP) = High Performance Applications (LP) = Low Power Applications

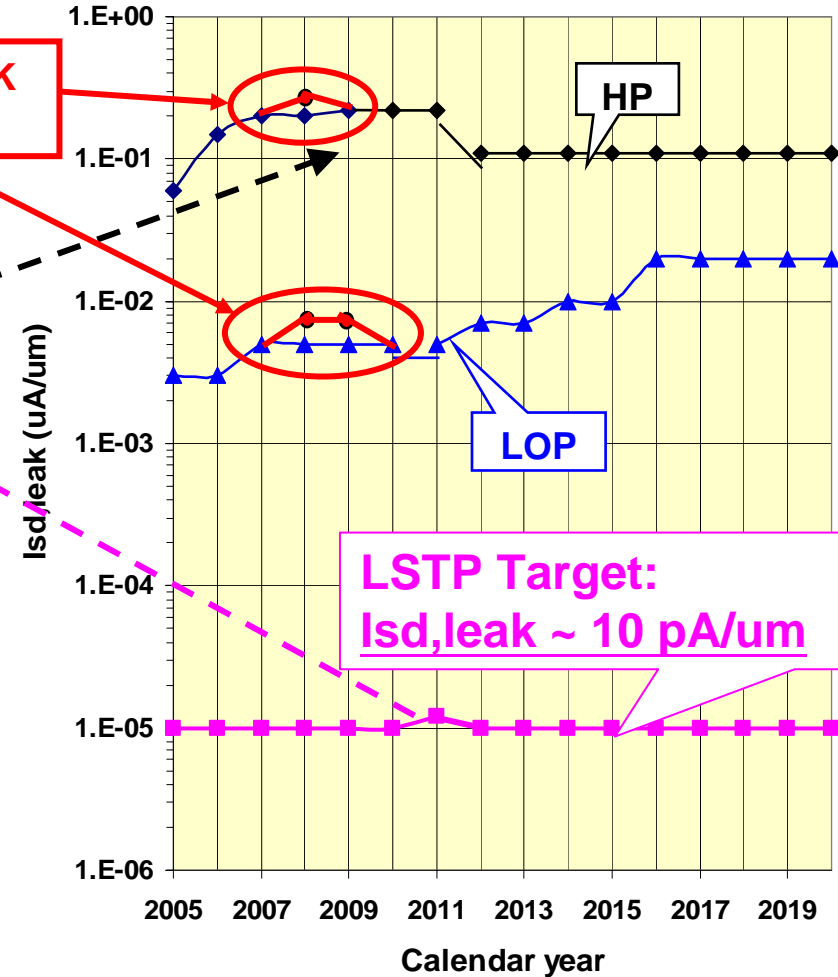


# Low Power & High Performance (HP): Impact of High-k & Metal Gate Deployment Delay

**Intrinsic Transistor Delay,**  
 $\tau = CV/I$   
 (lower delay = higher speed)

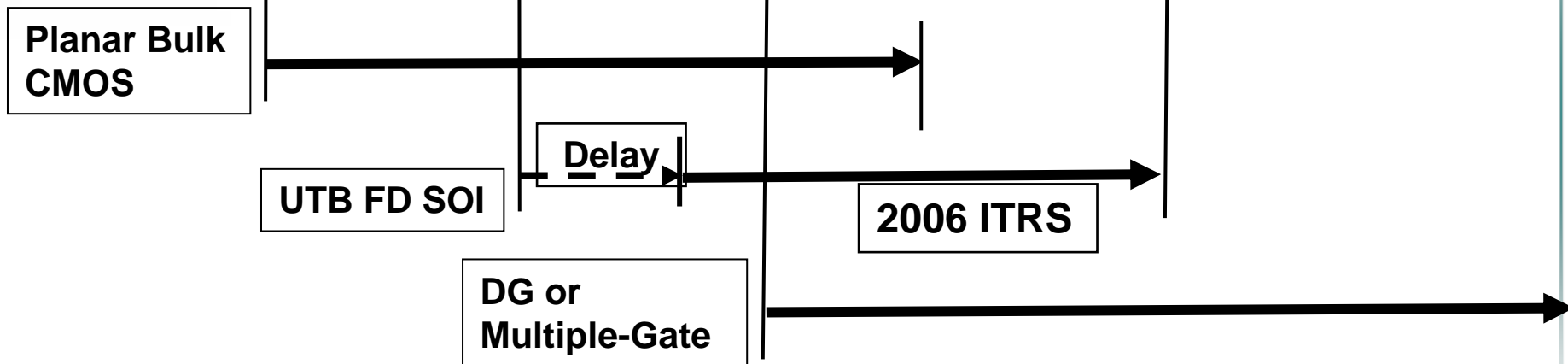


## Leakage Current



# Multiple Parallel Paths for High-Performance Logic in ITRS

Year in Production		2005	2006	2007	2008	2009	2010	2011	2012	2013	2014	2015	2016	2017	2018	2019	2020
Physical Lgate (High Performance)	nm	32	28	25	22	20	18	16	14	13	11	10	9	8	7	6	5



## Multiple parallel paths reflects most likely scenario:

- Some companies will extend planar bulk CMOS as long as possible
- Others will switch to FDSOI and/or multiple gate earlier
  - Initial deployment of FDSOI is delayed in 2006 ITRS
- Ultimate MOSFET is multiple gate
- Similar multiple paths for low-power logic



## Logic:

- **2007 revision considerations:**
  - Continue to update new technology (e.g. HK&MG) deployment schedule
  - Revise mobility enhancement factor
  - Revisit below scaling roadmaps to be realistic (interaction with multiple ITWGs)
    - Gate length/ LWR
    - Speed ( $1/\tau$ , 17% for HP)
    - Leakage (10pA/  $\mu\text{m}$  for LSTP)
    - Rsd , poly depletion
  - Separate PMOS table needs to be further explored
  - Parallel path period?
    - Life time bulk Si/ planar prolonged by u enhancement & Ge, IIIV

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# Reliability: Top 5 Near-Term Challenges

- **High-k Gate Dielectrics**
  - Dielectric breakdown; Transistor instability
- **Metal Gate**
  - Ion drift,  $V_{TH}$  stability, oxidation; thermal-mechanical
- **Cu/ Low k**
  - Electromigration and voiding; stability of interfaces; TDDB
  - Impact of porous, weaker, less thermally conductive dielectrics
- **Packaging**
  - Solder bumps; fracture; EM in packaging; CTE mismatch
- **Design & Test for Reliability**
  - Reliability simulation; Reliability screens

# Reliability: Key Issues

- **Reliability risk is growing**
  - **New materials (e.g., high k/metal gate; low k) and new devices (e.g., FDSOI) and new packaging**
    - **Introduce new and/or modified failure mechanisms**
    - **Mechanisms need to be identified, modeled and controlled**
    - **Have less-than-historic time and resources to ensure reliability**
  - **Difficult tradeoffs may require reduced reliability margins**
  - **Need new Design for Reliability tools and reliability screens**
- ***Need to sustain current high reliability levels in spite of unprecedented changes***



# Summary

- **Memory**
  - **DRAM: scaling continuing**
  - **Numerous different types of NVM, with unique attributes and scaling scenarios**
- **Logic**
  - **Numerous and rapid technology innovations required**
  - **2006 ITRS: delayed projected deployment of high-k and metal gate and FDSOI by 2 years, until 2010**
    - **Impacts transistor performance, leakage, and short channel effects**
    - **Reconsidering the deployment schedule in 2007**
- **Reliability**
  - **Ensuring reliability for numerous and rapid technological innovations is a critical challenge**
  - **Nevertheless, need to sustain current high reliability levels**

