

INTERNATIONAL
TECHNOLOGY ROADMAP
FOR
SEMICONDUCTORS

2006 UPDATE
FINAL DRAFT

ASSEMBLY AND PACKAGING

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ASSEMBLY AND PACKAGING

SUMMARY

The pace of change in assembly and packaging has accelerated as packaging is increasingly a limiting factor for both product cost and performance. Many of the tables have been updated to reflect these rapid changes. The major changes include:

The Difficult Challenges (Table 93) were amended to add issues associated with very small and very high frequency integrated circuits and the rapidly emerging requirements for packaging very thin die.

Extensive revisions in Tables 94 reflect changes in the projected technologies for chip to package interconnect. New entries were added for complex ICs in harsh environments since packaging requirements in this category can not be adequately covered by the existing categories.

The Materials Challenges (Table 95) update reflects the impact of changes in government regulations and the impact of demand for every thinner packages to accommodate requirements of portable consumer products.

Chip to Package Substrates (Table 96) have tape-automated bonding added reflecting the solder bump flip chip technology providing cost/performance advantages in specific packaging applications.

Package Substrate Physical Properties (Table 98) have been updated to incorporate additional parameters for thermal properties that are increasingly critical for higher temperature, smaller form factor packages.

DIFFICULT CHALLENGES

Table 93a Assembly and Packaging Difficult Challenges—Near-term UPDATED

	<i>Difficult Challenges ≥ 32 nm</i>	<i>Summary of Issues</i>
IS	Impact of BEOL incl Cu/low κ on Packaging	<ul style="list-style-type: none"> -Direct wirebond and bump to Cu or improved barrier systems bondable pads -Bump and underfill technology to assure low-κ dielectric integrity including lead free solder bump system -Improved fracture toughness of dielectrics materials -Interfacial adhesion -Reliability of first level interconnect with low κ -Mechanisms to measure the critical properties need to be developed. -Probing over copper/low κ -Singulation technology for circuits incorporating ultra-low κ dielectrics
IS	Wafer Level CSP	<ul style="list-style-type: none"> -I/O pitch for small die with high pin count -Solder joint reliability and cleaning processes for low stand-off -Wafer thinning and handling technologies -Compact ESD structures -TCE mismatch compensation for large die
IS	Coordinated Design Tools and Simulators to address Chip, Package, and Substrate Co-design	<ul style="list-style-type: none"> -Mix signal co-design and simulation environment -Rapid turn around modeling and simulation -Integrated analysis tools for transient thermal analysis and integrated thermal mechanical analysis -Electrical (power disturbs, EMI, signal and power integrity associated with higher frequency/current and lower voltage switching) -In package decoupling -System level co-design is needed now. -EDA for “native” area array is required to meet the Roadmap projections. -Models for reliability prediction
IS	Embedded Components	<ul style="list-style-type: none"> -Low cost embedded passives: R, L, C -Embedded active devices -Quality levels required not attainable on chip -Wafer level embedded components
IS	Thinned die packaging	<ul style="list-style-type: none"> - Wafer/die handling for thin die - Different carrier materials (organics, silicon, ceramics, glass, laminate core) impact -Establish infrastructure for new value chain -Establish new process flows -Reliability -Testability -Different active devices -Electrical and optical interface integration
IS	Close gap between Chip and substrate - Improved Organic Substrates	<ul style="list-style-type: none"> -Increased wireability at low cost -Improved impedance control and lower dielectric loss to support higher frequency applications -Improved planarity and low warpage at higher process temperatures -Low-moisture absorption -Increased via density in substrate core -Alternative plating finish to improve reliability -Solutions for operation temp up to C5-Interconnect density scaled to silicon (silicon I/O density increasing faster than the package substrate technology -Production techniques will require silicon-like production and process technologies after 2005. -Tg compatible with Pb free solder processing (including rework @260C)
IS	High Current Density Packages	<ul style="list-style-type: none"> -Electromigration will become a more limiting factor. It must be addressed through materials changes together with thermal/mechanical reliability modeling. -Whisker growth -Thermal dissipation
	Flexible System Packaging	<ul style="list-style-type: none"> -Conformal low cost organic substrates -Small and thin die assembly -Handling in low cost operation
	3D Packaging	<ul style="list-style-type: none"> -Thermal management -Design and simulation tools -Wafer to wafer bonding -Through wafer Via structure and via fill process -Bumpless interconnect architecture
	Fine Pitch Packaging	

Table 93b Assembly and Packaging Difficult Challenges—Long-term *UPDATED*

<i>Difficult Challenges</i> <i><32 nm</i>	<i>Summary of Issues</i>
Package Cost does not follow the Die Cost Reduction Curve	-Margin in packaging is inadequate to support investment required to reduce cost -Increased device complexity requires higher cost packaging solutions
Small Die with High Pad Count and/or High Power Density	These devices may exceed the capabilities of current assembly and packaging technology requiring new solder/UBM with: -Improved current density capabilities -Higher operating temperature
IS High Frequency Die	-Substrate wiring density to support >20 lines/mm -Lower loss dielectrics—skin effect above 10 GHz“ -Hot spot” thermal management <u>There is currently a “brick wall” at five-micron lines and spaces.</u>
System-level Design Capability to Integrated Chips, Passives, and Substrates	-Partitioning of system designs and manufacturing across numerous companies will make required optimization for performance, reliability, and cost of complex systems very difficult. -Complex standards for information types and management of information quality along with a structure for moving this information will be required. -Embedded passives may be integrated into the “bumps” as well as the substrates.
Emerging Device Types (Organic, Nanostructures, Biological) that require New Packaging Technologies	-Organic device packaging requirements not yet defined (will chips grow their own packages) -Biological interfaces will require new interface types

TECHNOLOGY REQUIREMENTS AND POTENTIAL SOLUTIONS

Table 94a Single-chip Packages Technology Requirements—Near-term Years **UPDATED**

Year of Production	2005	2006	2007	2008	2009	2010	2011	2012	2013
DRAM ½ Pitch (nm) (contacted)	80	70	65	57	50	45	40	35	32
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	90	78	68	59	52	45	40	36	32
MPU Physical Gate Length (nm)	32	28	25	22	20	18	16	14	13
Cost per Pin Minimum for Contract Assembly [1,2] (Cents/Pin)									
IS Low-cost, hand-held and memory	.27-.50	.28-.53	.27-.50	.25-.48	.24-.46	.23-.44	.22-.42	.21-.40	.20-.38
IS Cost-performance	.67-1.17	.72-1.26	.69-1.19	.66-1.13	.63-1.70	.60-1.20	.57-.97	.54-.92	.51-.87
IS High-performance	1.78	1.92	1.83	1.73	1.64	1.56	1.48	1.41	1.34
IS Harsh	0.29-2.60	0.28-2.33	0.27-2.11	0.25-2.00	0.24-1.90	0.23-1.54	.22-1.81	.21-1.71	.20-1.63
Chip size (mm ²)									
Lowcost/hand held	100	100	100	100	100	100	100	100	100
Cost performance	140	140	140	140	140	140	140	140	140
High performance	600	630	662	695	729	766	804	750	750
Harsh	100	100	100	100	100	100	100	100	100
Maximum Power (Watts/mm ²) [4]									
Hand held and memory (Watts) [1]	2.8	3	3	3	3	3	3	3	3
Cost-performance	0.65	0.7	0.74	0.79	0.83	0.85	0.85	0.89	0.98
High-performance	0.54	0.58	0.61	0.64	0.64	0.64	0.64	0.64	0.64
Harsh	0.16	0.18	0.18	0.2	0.2	0.22	0.22	0.24	0.25
Core Voltage (Volts)									
IS Low-cost	1	0.9	0.9	0.8	0.7	0.6	0.6	0.6	0.5
Hand-held and memory	0.9	0.8	0.7	0.6	0.6	0.5	0.5	0.5	0.5
Cost-performance	1	0.9	0.9	0.8	0.8	0.6	0.6	0.6	0.6
IS High-performance	1	0.9	0.9	0.8	0.8	0.6	0.6	0.6	0.6
IS Harsh	1.2	1.2	1.2	1.2	1.2	1.2	1	1	0.9
Package Pincount Maximum [5][6]									
Low-cost/ Hand held	134-550	140-578	148-606	150-636	160-668	170-700	180-738	188-774	198-812
IS Cost performance	550-900	550-1936	600-2140	600-2400	660-2801	660-2783	720-3061	720-3367	800-3704
IS High performance	3400	3800	4000	4400	4620	4851	5094	5348	5616
Harsh	350	368	386	405	425	447	469	492	517
Minimum Overall Package Profile (mm)									
Low-cost, hand held and memory	0.4	0.4	0.4	0.3	0.3	0.3	0.3	0.3	0.3
IS Cost-performance	0.8	0.8	0.8	0.65	0.65	0.65	0.65	0.5	0.5
High-performance	1.4	1.4	1.4	1.4	1.4	1.2	1.2	1	1
IS Harsh	0.8	0.8	0.8	0.8	0.8	0.8	0.7	0.7	0.7
Performance: On-Chip (MHz)[7]									
ADD Low-cost/Hand held	607/386 5	668/425 1	735/467 6	808/514 4	889/566 0	978-6224	1076 - 6846	1183 - 7530	1243-7903
ADD Cost-performance	5170	5687	6824	8189	9827	11793	14151	16981	18679
ADD High-performance	5170	5687	6824	8189	9827	11793	14151	16981	20378
ADD Harsh	88	96	106	117	128	141	155	171	188

Table 94a Single-chip Packages Technology Requirements—Near-term Years *UPDATED*

<i>Performance: Chip-to-Board for Peripheral Buses (MHz) [7]</i>										
IS	Low-cost Logic/Memory	100/400	100/533	100/667	100/800	100/800	125/800	125/800	125/1000	125/1000
	Cost-performance (for multi-drop nets)	533	667	733	800	800	800	800	1000	1000
IS	High-performance (for differential-pair point-to-point nets)	3125	3906	4883	6104	7629	9537	11921	14901	18626
	Harsh	88	96	106	106	115	125	125	125	125
	<i>Maximum Junction Temperature</i>									
IS	Low-cost, Hand Held and Memory	125	125	125	125	125	125	125	125	125
	Cost performance	100	100	95	95	90	90	90	90	90
	High-performance	100	100	95	95	90	90	90	90	90
	Harsh	175	175	175	175	200	220	220	220	220
ADD	Harsh-complex ICs	175	175	175	175	175	175	175	175	175
	<i>Operating Temperature Extreme: Ambient (°C)</i>									
IS	Low-cost, Hand Held and Memory	55	55	55	55	55	55	55	55	55
IS	Cost-performance	45	45	45	45	45	45	45	45	45
IS	High-performance	55	55	55	55	55	55	55	55	55
IS	Harsh	-40 to 150	-40 to 150	-40 to 150	-40 to 150	-40 to 175	-40 to 200	-40 to 200	-40 to 200	-40 to 200
ADD	Harsh-complex ICs	-40 to 150	-40 to 150	-40 to 150	-40 to 150	-40 to 150	-40 to 150	-40 to 150	-40 to 150	-40 to 150

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Table 94b Single-chip Packages Technology Requirements—Long-term Years **UPDATED**

Year of Production	2014	2015	2016	2017	2018	2019	2020
DRAM ½ Pitch (nm) (contacted)	28	25	22	20	18	16	14
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	28	25	22	20	18	16	14
MPU Physical Gate Length (nm)	11	10	9	8	7	6	6
Cost per Pin Minimum for Contract Assembly [1,2] (Cents/Pin)							
IS Low-cost, hand-held and memory	<u>.20-.36</u>	<u>.20-.34</u>	<u>.20-.32</u>	<u>.20-.30</u>	<u>.2-.29</u>	<u>.2-.27</u>	<u>.2-.26</u>
IS Cost-performance	<u>.48-.83</u>	<u>.46-.79</u>	<u>.44-.75</u>	<u>.42-.71</u>	<u>.39-.68</u>	<u>.37-.64</u>	<u>.36-.61</u>
IS High-performance	<u>1.27</u>	<u>1.21</u>	<u>1.15</u>	<u>1.09</u>	<u>1.04</u>	<u>0.99</u>	<u>0.94</u>
IS Harsh	<u>.20-1.55</u>	<u>.20-1.47</u>	<u>.20-1.40</u>	<u>.20-1.33</u>	<u>.20-1.26</u>	<u>.20-1.20</u>	<u>.20-1.14</u>
Chip size (mm ²)							
Lowcost/hand held	100	100	100	100	100	100	100
Cost performance	140	140	140	140	140	140	140
High performance	750	750	750	750	750	750	750
Harsh	100	100	100	100	100	100	100
Maximum Power (Watts/mm ²) [4]							
Hand held and memory (Watts) [1]	3	3	3	3	3	3	3
Cost-performance	0.98	0.98	1.08	1.08	1.08	1.08	1.08
High-performance	0.64	0.64	0.64	0.64	0.64	0.64	0.64
Harsh	0.25	0.27	0.28	0.28	0.29	0.29	0.29
Core Voltage (Volts)							
IS Low-cost	0.5	0.4	0.4	0.4	0.4	0.4	0.4
Hand-held and memory	0.4	0.4	0.4	0.4	0.4	0.4	0.4
Cost-performance	0.5	0.5	0.5	0.5	0.5	0.5	0.5
IS High-performance	<u>0.5</u>	0.5	0.5	0.5	0.5	0.5	0.5
IS Harsh	<u>0.9</u>	<u>0.9</u>	<u>0.9</u>	<u>0.8</u>	<u>0.8</u>	<u>0.8</u>	<u>0.8</u>
Package Pincount Maximum [5][6]							
Low-cost/ Hand held	<u>207-853</u>	218-896	<u>229-940</u>	240-988	<u>252-1037</u>	<u>265-1089</u>	<u>278-1144</u>
IS Cost performance	<u>800-4075</u>	<u>880-4482</u>	<u>880-4930</u>	<u>960-5423</u>	<u>960-5966</u>	<u>1050-6562</u>	<u>1050-7218</u>
IS High performance	<u>5896</u>	<u>6191</u>	<u>6501</u>	<u>6826</u>	<u>7167</u>	<u>7525</u>	<u>7902</u>
Harsh	543	570	599	629	660	693	728
Minimum Overall Package Profile (mm)							
Low-cost, hand held and memory	0.2	0.2	0.2	0.2	0.2	0.2	0.2
IS Cost-performance	0.5	0.5	<u>0.4</u>	<u>0.4</u>	<u>0.4</u>	<u>0.4</u>	<u>0.4</u>
High-performance	1	1	1	1	1	1	1
IS Harsh	<u>0.7</u>	<u>0.7</u>	<u>0.6</u>	<u>0.6</u>	<u>0.6</u>	<u>0.6</u>	<u>0.6</u>
Performance: On-Chip (MHz)[7]							
ADD Low-cost/Hand held	<u>1305-8303</u>	<u>1370-8718</u>	<u>1438-9154</u>	<u>1510-9612</u>	<u>1586-10092</u>	<u>1665-10597</u>	<u>1748-11127</u>
ADD Cost-performance	<u>20547</u>	<u>22602</u>	<u>24862</u>	<u>27349</u>	<u>30083</u>	<u>33092</u>	<u>36401</u>
ADD High-performance	<u>24453</u>	<u>29344</u>	<u>34925</u>	<u>41910</u>	<u>50291</u>	<u>60350</u>	<u>72420</u>
ADD Harsh	<u>207</u>	<u>227</u>	<u>250</u>	<u>275</u>	<u>302</u>	<u>333</u>	<u>366</u>
Performance: Chip-to-Board for Peripheral Buses (MHz) [7]							
IS Low-cost Logic/Memory	<u>125/1000</u>	<u>125/1000</u>	<u>150/1200</u>	<u>150/1200</u>	<u>150/1200</u>	<u>150/1200</u>	<u>150/1200</u>
Cost-performance (for multi-drop nets)	1000	1000	1200	1200	1200	1200	1200
IS High-performance (for differential-pair point-to-point nets)	<u>23283</u>	<u>29104</u>	<u>34925</u>	<u>41910</u>	<u>50291</u>	<u>60350</u>	<u>72420</u>
Harsh	125	150	150	150	150	150	150

Table 94b Single-chip Packages Technology Requirements—Long-term Years *UPDATED*

Maximum Junction Temperature								
IS	Low-cost, Hand Held and Memory	125	125	125	125	125	125	125
	Cost performance	90	90	90	90	90	90	90
	High-performance	90	90	90	90	90	90	90
	Harsh	220	220	220	220	220	220	220
ADD	Harsh-complex ICs	175	175	175	175	175	175	175
Operating Temperature Extreme: Ambient (°C)								
IS	Low-cost, Hand Held and Memory	55	55	55	55	55	55	55
IS	Cost-performance	45	45	45	45	45	45	45
IS	High-performance	55	55	55	55	55	55	55
IS	Harsh	-40 to 200	-40 to 200	-40 to 200	-40 to 200	-40 to 200	-40 to 200	-40 to 200
ADD	Harsh-complex Ics	-40 to 150	-40 to 150	-40 to 150	-40 to 150	-40 to 150	-40 to 150	-40 to 150

BILL - WHICH NOTES DO WE KEEP?

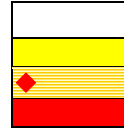
Notes for Table 94a and b:
in file for 2006:

- Maximum power is average for die area
- Hot spots may exceed average package density
- Hand held power limit is based on the product power dissipation limit

from 2005 ITRS chapter:

- Maximum chip power density will not occur in the largest die
- Power density numbers are average per die. Within the die there may be hot spots with substantially higher local power density
- Range in pin count for low cost and cost performance is due to different device types and package technologies employed
- The chip size for cost performance is driven by microprocessors and high performance is driven by FPGA and ASIC devices

- Manufacturable solutions exist, and are being optimized
- Manufacturable solutions are known
- Interim solutions are known
- Manufacturable solutions are NOT known



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Table Requirements and Difficult Challenges for MEMS Packaging

<i>MEMS Packaging</i> → ↓	<i>RF MEMS</i>	<i>BioMEMS</i>	<i>Inertial MEMS</i>	<i>Optical MEMS</i>
<i>Requirements</i>	<p>Electrical</p> <ul style="list-style-type: none"> - low insertion loss - low back reflection - low contact resistance - frequency - signal isolation - package resonance - low parasitics <p>Structural</p> <ul style="list-style-type: none"> - low stress - small form factor <p>Package</p> <ul style="list-style-type: none"> - wafer level package - small form factor - hermeticity - low loss packaging material - light weight 	<p>Fluidic</p> <ul style="list-style-type: none"> - low dead volume - sensitivity in detection - low back pressure - fluidic channel size - flow rate - heating/cooling rate <p>Electrical</p> <ul style="list-style-type: none"> - interface with electronic circuits <p>Thermal</p> <ul style="list-style-type: none"> - fast heating and cooling <p>Optical</p> <ul style="list-style-type: none"> - low optical loss <p>Structural</p> <ul style="list-style-type: none"> - low stress at fluidic joints <p>Package</p> <ul style="list-style-type: none"> - modular package - disposable 	<p>Structural</p> <ul style="list-style-type: none"> - low stress - meet reliability requirements <p>Thermal</p> <ul style="list-style-type: none"> - temperature stabilization <p>Electrical</p> <ul style="list-style-type: none"> - sensitivity - switching time - frequency - Q factor <p>Package</p> <ul style="list-style-type: none"> - plastic package - wafer level package 	<p>Optical</p> <ul style="list-style-type: none"> - low coupling loss - mirror rotation/angle <p>Structural</p> <ul style="list-style-type: none"> - low stress package - low shrinkage of UV epoxy - low warpage <p>Thermal</p> <ul style="list-style-type: none"> - thermal stabilization <p>Electrical</p> <ul style="list-style-type: none"> - switching speed and time <p>Package</p> <ul style="list-style-type: none"> - ceramic package - metal package
<i>Difficult Challenges</i>	<p>Optimization of electrical and structural parameters</p> <p>Low cost materials to reduce insertion loss</p> <p>Form factor reduction</p> <p>Passive device integration</p>	<p>Co-design of fluidic, electrical thermal, optical and structural design</p> <p>Dead vacuum reduction</p> <p>Channel size reduction</p> <p>Zero back pressure</p> <p>Flow in nano channels</p> <p>Bubble elimination</p> <p>Bio compatibility of material</p>	<p>Structural design</p> <p>Reliability of package</p> <p>Vacuum/hermeticity</p> <p>Low cost</p> <p>Small form factor</p> <p>Integration into other systems</p>	<p>Optical, structural design to meet low coupling loss/reliability</p> <p>Low cost</p> <p>Integration into other systems</p>
<i>Potential Directions</i>	<p>RF system in package</p> <p>Bio-RF integration</p>	<p>3D microfluidic package</p> <p>Bio system in package</p> <p>Plastic based fluidic systems</p>	<p>MEMS system in package</p> <ul style="list-style-type: none"> - mobile application - bio application - information technology 	<p>Wafer level package</p>

Table 95 Materials Challenges *UPDATED*

	Materials Challenges for discrete packages	Issues
IS	Wirebond	Materials that enable 25 micron pitch without wire sweep, barrier metals for Cu wirebond pads to reduce intermetallics (<u>insulated wire is a potential solution</u>)
IS	Underfills	<u>Ability to support 100 pitch on large die, reduce stress on low-K and compatibility with lead free reflow</u>
IS	Thermal Interfaces	Increased thermal conduction, improved adhesion, <u>higher modulus for thin applications</u>
IS	Materials Properties	<u>Methodology and characterization database for frequencies above 10 GHz</u>
IS	Molding Compound	Low modulus materials that reduce stress on low-κ wafer structures with low moisture absorption for high temperature lead free applications
	Leadfree Solder Flip Chip Materials	Solder and UBM the supports high current density and avoid electromigration
ADD	<u>Die attach solder for Tj >200C</u>	<u>No feasible solution seen</u>
ADD	<u>Rigid Organic substrates</u>	<u>Lower loss dielectric, lower TCE, and higher Tg at low cost</u>
	Embedded passives	Improved high frequency performance of dielectrics with κ above 1000; High reliability, better stability resistor materials. Ferromagnetics for sensor and MEMs applications
IS	LTCC	Low shrink dielectric and lower dielectric constant for high frequency application . <u>Lower firing temperature to reduce stress due to TCE mismatch</u>
ADD	<u>ROHS</u>	<u>Compliance</u>
ADD	<u>Solder replacement</u>	<u>Flexibility in joining to accommodate stress associated with TCE mismatch over the operating range</u>
ADD	<u>Die attach film</u>	<u>Thin wafers will suggest combination of dicing film and die attach film in a single film material. It is in use today to save production time.</u> <u>Materials are too thick and process convenience is not yet adequate.</u> <u>Embedded wiring in die attach film.</u> <u>Film that can be singulated by pulling for die that have been singulated with laser</u>
DEL ETE	Green Materials	"Green materials with the same or better process compatibility and cost as existing materials"
DEL ETE	WLP dielectrics	Dielectrics for WLP with curing temperatures below 200° C

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Table 96a Chip to Package Substrate—Near-term Years **UPDATED**

	Year of Production	2005	2006	2007	2008	2009	2010	2011	2012	2013
	DRAM ½ Pitch (nm) (contacted)	80	70	65	57	50	45	40	35	32
	MPU/ASIC Metal 1 (M1) ½ Pitch (nm) (f)	90	78	68	59	52	45	40	36	32
	MPU Physical Gate Length (nm)	32	28	25	22	20	18	16	14	13
IS	Wire bond—single in-line (micron)	<u>45</u>	<u>40</u>	<u>40</u>	<u>35</u>	<u>35</u>	<u>30</u>	<u>30</u>	<u>25</u>	<u>25</u>
IS	Two-row Staggered Pitch (micron)	<u>50</u>	<u>50</u>	<u>45</u>	<u>45</u>	<u>40</u>	<u>40</u>	35	35	35
IS	Three-tier Pitch (micron)	<u>60</u>	<u>55</u>	<u>50</u>	<u>50</u>	<u>45</u>	<u>45</u>	<u>40</u>	<u>40</u>	35
	Wire bond—Wedge pitch (micron)	30	25	25	25	20	20	20	20	20
ADD	Tape-automated Bonding (TAB)*	<u>30</u>	<u>30</u>	<u>25</u>	<u>25</u>	<u>25</u>	<u>20</u>	<u>20</u>	<u>20</u>	<u>20</u>
	Flying Lead (micron)	35	35	35	35	35	35	35	35	35
IS	Flip Chip Area Array (both organic and ceramic substrate)(micron)	150	130	<u>130</u>	<u>130</u>	<u>120</u>	<u>120</u>	<u>120</u>	<u>110</u>	<u>110</u>
IS	Flip Chip on Tape or Film** (micron)	35	30	<u>25</u>	25	<u>20</u>	<u>20</u>	<u>20</u>	<u>15</u>	<u>15</u>

Table 96b Chip to Package Substrate—Long-term Years **UPDATED**

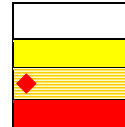
	Year of Production	2014	2015	2016	2017	2018	2019	2020
	DRAM ½ Pitch (nm) (contacted)	28	25	22	20	18	16	14
	MPU/ASIC Metal 1 (M1) ½ Pitch (nm) (f)	28	25	22	20	18	16	14
	MPU Physical Gate Length (nm)	11	10	9	8	7	6	6
IS	Wire bond—single in-line (micron)	25	25	25	25	25	25	25
IS	Two-row Staggered Pitch (micron)	35	35	35	35	35	35	35
IS	Three-tier Pitch (micron)	35	35	35	35	35	35	35
	Wire bond—Wedge pitch (micron)	20	20	20	20	20	20	20
ADD	Tape-automated Bonding (TAB)*	<u>20</u>	<u>15</u>	<u>15</u>	<u>15</u>	<u>15</u>	<u>15</u>	<u>15</u>
	Flying Lead (micron)	35	35	35	35	35	35	35
IS	Flip Chip Area Array (both organic and ceramic substrate)(micron)	<u>100</u>	<u>100</u>	<u>95</u>	<u>95</u>	<u>90</u>	<u>90</u>	<u>85</u>
IS	Flip Chip on Tape or Film** (micron)	<u>15</u>	<u>15</u>	<u>15</u>	<u>15</u>	<u>15</u>	<u>15</u>	<u>15</u>

Manufacturable solutions exist, and are being optimized

Manufacturable solutions are known

Interim solutions are known

Manufacturable solutions are NOT known



Notes for Table 96a and b:

*This is for solder bump flip chip. For extremely high current applications, solder bump pad pitch may be larger to allow bigger via opening to UBM. Conductive adhesive flip chip is not addressed but may have smaller pitches for small die applications, provided high density substrate with competitive cost is available.

** Minimum pitch is for Au/Ni bumps

Table 97a Substrate to Board Pitch—Near-term Years **UPDATED**

Year of Production	2005	2006	2007	2008	2009	2010	2011	2012	2013
DRAM ½ Pitch (nm) (contacted)	80	70	65	57	50	45	40	36	32
MPU/ASIC Metal 1 (M1) ½ Pitch (nm) (f)	90	78	68	59	52	45	40	36	32
MPU Physical Gate Length (nm)	32	28	25	23	20	18	16	14	13
BGA Solder Ball Pitch (mm) Conventional system Board									
Low-cost and hand-held*	0.8	0.65	0.65	0.65	0.65	0.65	0.5	0.5	0.5
Cost-performance	0.8	0.65	0.65	0.65	0.65	0.65	0.5	0.5	0.5
High-performance	1	1	0.8	0.8	0.8	0.8	0.65	0.65	0.5
Harsh	0.8	0.8	0.8	0.65	0.65	0.65	0.65	0.5	0.5
IS Small portable products <i>using flex or other specialized substrate</i>									
Low-cost and hand-held	0.65	0.65	0.65	0.65	0.65	0.5	0.5	0.5	0.5
IS Harsh	0.8	0.8	0.65	0.65	0.65	0.65	0.5	0.5	0.5
CSP area array pitch (mm)	0.3	0.2	0.2	0.2	0.2	0.2	0.15	0.15	0.15
QFP lead pitch (mm)	0.4	0.4	0.4	0.3	0.3	0.3	0.3	0.3	0.3
SON land pitch (mm)	0.5	0.4	0.4	0.4	0.4	0.3	0.3	0.3	0.3
QFN land pitch (mm)	0.4	0.4	0.4	0.3	0.3	0.3	0.3	0.3	0.3
P-BGA ball pitch (mm)	1.0	0.8	0.8	0.8	0.8	0.65	0.65	0.65	0.65
T-BGA ball pitch (mm)	0.8	0.65	0.65	0.65	0.65	0.5	0.5	0.5	0.5
FBGA ball pitch (mm)	0.4	0.3	0.3	0.2	0.2	0.15	0.15	0.15	0.15
FLGA land pitch (mm)	0.4	0.3	0.3	0.3	0.3	0.3	0.3	0.3	0.3

*Minimum number driven by hand held application T-BGA—tab interconnected BGA

Table 97b Substrate to Board Pitch—Long-term Years **UPDATED**

Year of Production	2014	2015	2016	2017	2018	2019	2020
DRAM ½ Pitch (nm) (contacted)	28	25	22	20	18	16	14
MPU/ASIC Metal 1 (M1) ½ Pitch (nm) (f)	28	25	22	20	18	16	14
MPU Physical Gate Length (nm)	11	10	9	8	7	6	6
BGA Solder Ball Pitch (mm) Conventional system Board							
Low-cost and hand-held*	0.5	0.5	0.5	0.5	0.5	0.5	0.5
Cost-performance	0.5	0.5	0.5	0.5	0.5	0.5	0.5
High-performance	0.5	0.5	0.5	0.5	0.5	0.5	0.5
Harsh	0.5	0.5	0.5	0.5	0.5	0.5	0.5
IS Small portable products <i>using flex or other specialized substrate</i>							
Low-cost and hand-held	0.5	0.5	0.5	0.5	0.5	0.5	0.5
IS Harsh	0.5	0.5	0.5	0.5	0.5	0.5	0.5
CSP area array pitch (mm)	0.1	0.1	0.1	0.1	0.1	0.1	0.1
QFP lead pitch (mm)	0.3	0.2	0.2	0.2	0.2	0.2	0.2
SON land pitch (mm)	0.3	0.3	0.3	0.3	0.3	0.3	0.3
QFN land pitch (mm)	0.3	0.3	0.3	0.3	0.3	0.3	0.3
P-BGA ball pitch (mm)	0.65	0.65	0.65	0.65	0.65	0.65	0.65
T-BGA ball pitch (mm)	0.5	0.5	0.5	0.5	0.5	0.5	0.5
FBGA ball pitch (mm)	0.15	0.15	0.15	0.15	0.15	0.15	0.15
FLGA land pitch (mm)	0.3	0.3	0.3	0.3	0.3	0.3	0.3

*Minimum number driven by hand held application T-BGA—tab interconnected BGA

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Materials parameters for embedded passive components

<i>Desired Figures of Merit</i>	
<i>Resistor Materials</i>	<i>Capacitor Materials</i>
Range: 10 Ω to 100K Ω	Dielectric Constant > 1000
TCR: 1000 ppm hot/cold	Thickness: ~10 Microns
CV: 5%	Breakdown Voltage > 100V
85RH/85C < 2% Drift	Ins. Resistance > 10 ¹¹ Ω
Therm. Cycle < 2% Drift	Dissipation Factor: < 3%
Solder Dips < 2% Drift	Therm. Coeff. Cap: X7R Spec.

Table 98a Package Substrate Physical Properties—Near-term Years *UPDATED*

	Year of Production	2005	2006	2007	2008	2009	2010	2011	2012	2013
	DRAM ½ Pitch (nm) (contacted)	80	70	65	57	50	45	40	36	32
	MPU/ASIC Metal 1 (M1) ½ Pitch (nm) (f)	90	78	68	59	52	45	40	36	32
	MPU Physical Gate Length (nm)	32	28	25	23	20	18	16	14	13
ADD	Glass Transition Temperature (Unit: °C)	-	-	-	-	-	-	-	-	-
ADD	State of the Art	Rigid Structure	300	300	300	350	350	350	350	350
ADD		Buildup Structure	220	220	220	250	250	250	250	250
ADD		Tape Structure	350	350	350	350	350	350	350	350
	<i>Dielectric Constant (at 1GHz)</i>									
	State of the Art	Rigid Structure*	3.1	3.1	3	3	2.7	2.7	2.7	2.7
		Buildup Structure	2.8	2.8	2.8	2.8	2.5	2.5	2.5	2.5
		Tape Structure	2.5	2.5	2.2	2.2	2.2	2.2	2.2	2.2
		Ceramics Structure/ <u>Low Dielectric Material</u>	4	4	4	4	3	3	3	3
		Ceramics Structure/High Dielectric Material	20	100	100	100	100	100	100	100
	<i>Dielectric Loss (at 1GHz)</i>									
	State of the Art	Rigid Structure	0.011	0.01	0.01	0.01	0.006	0.006	0.006	0.006
IS		Buildup-Structure	0.002	0.002	0.002	0.002	0.002	0.002	0.002	0.002
		Tape Structure	0.0005	0.0005	0.0002	0.0001	0.0001	0.0001	0.0001	0.0001
IS		Ceramics Structure	0.005	0.005	0.0005	0.005	0.0095	0.014	0.0185	0.023
ADD	-	<u>Coefficient of Thermal Expansion: X-Y Direction (Unit: ppm/°C)</u>	-	-	-	-	-	-	-	-
ADD	State of the Art	Rigid Structure	11	10	10	9	8	6	6	6
ADD		Buildup Structure	6	6	5	4	4	4	4	4
ADD		Tape Structure	15	15	10	10	10	10	10	10
ADD		Ceramics Structure	4 – 12	4 – 12	4 – 12	4 – 12	4 – 12	4 – 12	4 – 12	4 – 12
ADD	-	<u>Coefficient of Thermal Expansion: Z Direction (Unit: ppm/°C)</u>	-	-	-	-	-	-	-	-
ADD	State of the Art	Rigid Structure	30	20	20	20	20	20	20	20
ADD		Buildup Structure with core layer	20	10	10	10	10	10	10	10
ADD		Tape Structure	15	15	10	10	10	10	10	10
ADD		Ceramics Structure	4 – 12	4 – 12	4 – 12	4 – 12	4 – 12	4 – 12	4 – 12	4 – 12
	<i>Water Absorption at 23°C/24hrs Dipped (Unit: %)</i>									
	State of the Art	Rigid Structure	0.05	0.04	0.04	0.04	0.04	0.04	0.04	0.04
		Buildup with Reinforcement Material	0.05	0.04	0.04	0.04	0.04	0.04	0.04	0.04
		Buildup without Reinforcement Material	0.1	0.1	0.1	0.1	0.1	0.1	0.1	0.1
		Tape Structure	0.2	0.2	0.2	0.2	0.2	0.2	0.2	0.2
	<i>Young's Modulus (Unit: GPa)</i>									
	State of the Art	Rigid Structure	45	45	45	45	45	45	45	45
		Buildup with Reinforcement Material	30	30	35	35	35	35	35	35
		Buildup without Reinforcement Material	6	6	6	6	6	6	6	6
		Tape Structure	3	3	3	3	3	3	3	3
		Ceramics Structure	100 – 300	50 – 400	50-400	50 – 400	50 – 400	50 – 400	50-400	50 – 400
	<i>Peel Strength (Unit: kN/m)</i>									
	State of the Art	Rigid Structure	1.6	1.6	1.6	1.6	1.6	1.6	1.6	1.6
		Buildup Structure Buildup Layer	1.6	1.6	1.6	1.6	1.6	1.6	1.6	1.6
		Tape Structure	1.4	1.4	1.4	1.4	1.4	1.4	1.4	1.4

Note: State of the art materials may not be compatible with cost requirements for volume production

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Table 98b Package Substrate Physical Properties—Long-term Years **UPDATED**

	Year of Production	2014	2015	2016	2017	2018	2019	2020
	DRAM ½ Pitch (nm) (contacted)	28	25	22	20	18	16	14
	MPU/ASIC Metal 1 (M1) ½ Pitch (nm) (f)	28	25	22	20	18	16	14
	MPU Physical Gate Length (nm)	11	10	9	8	7	6	6
ADD	Glass Transition Temperature (Unit: °C)	-	-	-	-	-	-	-
ADD	State of the Art	350	350	350	350	350	350	350
ADD	Buildup Structure	250	250	250	250	250	250	250
ADD	Tape Structure	350	350	350	350	350	350	350
	Dielectric Constant (at 1GHz)							
	State of the Art							
	Rigid Structure*	2.7	2.7	2.7	2.7	2.7	2.7	2.7
	Buildup Structure	2.5	2.5	2.5	2.5	2.5	2.5	2.5
	Tape Structure	2.2	2.2	2.2	2.2	2.2	2.2	2.2
	Ceramics Structure/Low Dielectric Material	3	3	3	3	3	3	3
	Ceramics Structure/High Dielectric Material	100	100	100	100	100	100	100
	Dielectric Loss (at 1GHz)							
IS	State of the Art							
	Rigid Structure	0.006	0.006	0.006	0.006	0.006	0.006	0.006
	Buildup-Structure	0.002	0.002	0.002	0.002	0.002	0.002	0.002
	Tape Structure	0.0001	0.0001	0.0001	0.0001	0.0001	0.0001	0.0001
IS	Ceramics Structure	0.005	-0.0175	-0.04	-0.0625	-0.085	-0.1075	-0.13
ADD	Coefficient of Thermal Expansion: X-Y Direction (Unit: ppm/°C)	-	-	-	-	-	-	-
ADD	State of the Art	6	6	6	6	6	6	6
ADD	Buildup Structure	4	4	4	4	4	4	4
ADD	Tape Structure	10	10	10	10	10	10	10
ADD	Ceramics Structure	4 – 12	4 – 12	4 – 12	4 – 12	4 – 12	4 – 12	4 – 12
ADD	Coefficient of Thermal Expansion: Z Direction (Unit: ppm/°C)	-	-	-	-	-	-	-
ADD	State of the Art	20	20	20	20	20	20	20
ADD	Buildup Structure with core layer	10	10	10	10	10	10	10
ADD	Tape Structure	10	10	10	10	10	10	10
ADD	Ceramics Structure	4 – 12	4 – 12	4 – 12	4 – 12	4 – 12	4 – 12	4 – 12
	Water Absorption at 23°C/24hrs Dipped (Unit: %)							
	State of the Art							
	Rigid Structure	0.04	0.04	0.04	0.04	0.04	0.04	0.04
	Buildup with Reinforcement Material	0.04	0.04	0.04	0.04	0.04	0.04	0.04
	Buildup without Reinforcement Material	0.1	0.1	0.1	0.1	0.1	0.1	0.1
	Tape Structure	0.2	0.2	0.2	0.2	0.2	0.2	0.2
	Young's Modulus (Unit: GPa)							
	State of the Art							
	Rigid Structure	45	45	45	45	45	45	45
	Buildup with Reinforcement Material	35	35	35	35	35	35	35
	Buildup without Reinforcement Material	6	6	6	6	6	6	6
	Tape Structure	3	3	3	3	3	3	3
	Ceramics Structure	50 – 400	50-400	50 – 400	50 – 400	50-400	50 – 400	50 – 400
	Peel Strength (Unit: kN/m)							
	State of the Art							
	Rigid Structure	1.6	1.6	1.6	1.6	1.6	1.6	1.6
	Buildup Structure Buildup Layer	1.6	1.6	1.6	1.6	1.6	1.6	1.6
	Tape Structure	1.4	1.4	1.4	1.4	1.4	1.4	1.4

Note: State of the art materials may not be compatible with cost requirements for volume production

Manufacturable solutions exist, and are being optimized
 Manufacturable solutions are known
 Interim solutions are known
 Manufacturable solutions are NOT known

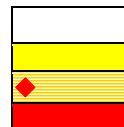


Table 98c Package Substrate Design Parameters—Near-term Years

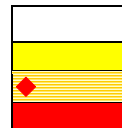
Year of Production	2005	2006	2007	2008	2009	2010	2011	2012	2013
DRAM ½ Pitch (nm) (contacted)	80	70	65	57	50	45	40	36	32
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	90	78	68	59	52	45	40	36	32
MPU Physical Gate Length (nm)	32	28	25	22	20	18	16	14	13
<i>Substrate cross-section core thickness (µm)</i>									
Handhelds	50	40	40	35	35	30	30	30	25
High density interconnect substrates	100	60	50	40	40	35	35	30	30
Build-up substrates	400	200	200	150	130	100	90	80	80
Coreless	50	50	40	40	35	35	30	30	30
<i>Blind via diameter (µm)</i>									
Handhelds	60	50	50	40	40	35	35	30	30
High density interconnect substrates	60	50	50	40	40	35	35	30	30
Build-up substrates	50	40	40	35	35	30	30	25	25
Coreless	70	60	60	50	50	40	40	35	35
<i>Blind via stacks</i>									
High density interconnect substrates	2	2	3	3	3	3	4	4	4
Build-up substrates	4	5	5	6	6	6	6	6	6
Coreless	7	9	10	11	11	11	12	12	13
<i>PTH diameter (µm)</i>									
	100	80	75	70	60	50	50	45	45
<i>PTH land (µm)</i>									
	230	180	180	160	140	120	110	105	105
<i>Bump pitch (µm)</i>									
High density interconnect substrates	230	200	190	180	170	160	150	140	140
Build-up substrates	180	150	130	120	110	100	100	90	90
Coreless	180	150	130	120	110	100	100	90	90
<i>Lines/space width (µm)</i>									
Rigid Structure	45	40	35	30	30	25	25	22	22
Build-up substrates (core layer)	45	40	35	30	30	25	25	22	22
Build-up substrate (build-up layer)	18	15	15	10	10	10	9	8	8
Coreless	25	20	20	15	15	10	9	8	8
<i>Lines/space width tolerance (%)</i>									
	10	7	7	7	7	7	7	7	6
<i>Solder mask registration ± (µm)</i>									
Handhelds	25	25	20	15	15	15	12	12	11
High density interconnect substrates	40	25	20	15	15	15	12	12	11
Build-up substrates	40	25	25	20	20	15	12	12	11

Manufacturable solutions exist, and are being optimized

Manufacturable solutions are known

Interim solutions are known

Manufacturable solutions are NOT known



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Table 98d Package Substrate Design Parameters—Long-term Years

Year of Production	2014	2015	2016	2017	2018	2019	2020
DRAM ½ Pitch (nm) (contacted)	28	25	22	20	18	16	14
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	28	25	22	20	18	16	14
MPU Physical Gate Length (nm)	11	10	9	8	7	6	6
<i>Substrate cross-section core thickness (µm)</i>							
Handhelds	25	25	25	25	25	25	25
High density interconnect substrates	30	30	30	30	30	30	30
Build-up substrates	70	70	70	70	70	70	70
Coreless	30	30	30	30	30	30	30
<i>Blind via diameter (µm)</i>							
Handhelds	25	25	25	25	25	25	25
High density interconnect substrates	25	25	25	25	25	25	25
Build-up substrates	20	20	20	20	20	20	20
Coreless	30	30	30	30	30	30	30
<i>Blind via stacks</i>							
High density interconnect substrates	4	4	4	4	4	4	4
Build-up substrates	6	6	6	6	6	6	6
Coreless	14	14	14	14	14	14	14
<i>PTH diameter (µm)</i>							
	40	40	40	40	40	40	40
<i>PTH land (µm)</i>							
	100	100	100	100	100	100	100
<i>Bump pitch (µm)</i>							
High density interconnect substrates	130	130	130	130	130	130	130
Build-up substrates	80	80	80	80	70	70	70
Coreless	80	80	80	80	70	70	70
<i>Lines/space width (µm)</i>							
Rigid Structure	20	20	20	20	20	20	20
Build-up substrates (core layer)	20	20	20	20	20	20	20
Build-up substrate (build-up layer)	8	8	8	8	8	8	8
Coreless	8	8	8	8	8	8	8
<i>Lines/space width tolerance (%)</i>							
	5	5	5	5	5	5	5
<i>Solder mask registration ±(µm)</i>							
Handhelds	10	10	10	10	10	10	10
High density interconnect substrates	10	10	10	10	10	10	10
Build-up substrates	10	10	10	10	10	10	10

Manufacturable solutions exist, and are being optimized

Manufacturable solutions are known

Interim solutions are known

Manufacturable solutions are NOT known

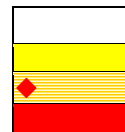


Table 99 Package Level System Integration **UPDATED**

				2005	2006	2008	2010	2012	2014
				High Performance / Low Cost, Handheld					
Passives	Capacitor	o for YES		o/o	o/o	o/o	o/o	o/o	o/o
	Resistor			o/-	o/o	o/o	o/o	o/o	o/o
	Inductor			-/o	o/o	o/o	o/o	o/o	o/o
Actives	Optical	o for YES		o/o	o/o	o/o	o/o	o/o	o/o
	CCD/CMOS Sensor			-/o	-/o	-/o	-/o	-/o	-/o
	MEMS			-/-	-/-	-/o	-/o	-/o	-/o
Package Inner Structure	IC to IC Connection	o for Applicable	Wire	-/o	-/o	-/o	-/o	-/o	-/o
			Flip Chip	-/o	o/o	o/o	o/o	o/o	o/o
			Via Hole	-/-	-/o	-/o	-/o	-/o	-/o
	IC to Substrate Connection	o for Applicable	Wire	o/o	o/o	o/o	o/o	o/o	o/o
			Flip Chip	o/o	o/o	o/o	o/o	o/o	o/o
			Via Hole	-/-	-/o	-/o	-/o	-/o	-/o
Embedded Components	IC	o for Applicable	IC	-/-	-/-	/o	/o	o/o	o/o
	Passives		Capacitor	-/-	o/o	o/o	o/o	o/o	o/o
			Resistor	-/-	o/o	o/o	o/o	o/o	o/o
			Inductor	-/-	-/o	o/o	o/o	o/o	o/o
Substrate Material	Organic	o for Applicable	Rigid	o/o	o/o	o/o	o/o	o/o	o/o
			Flexible	-/o	-/o	-/o	-/o	-/o	-/o
	Inorganic		Ceramic	o/o	o/o	o/o	o/o	o/o	o/o
			Silicon	-/-	o/o	o/o	o/o	o/o	o/o

Table 100 Processes used for SiP

Technologies and Processes for SiP	Substrate Level	Wafer Level
Pre-processing of wafers		
Thinning, dicing	ca.50 μm	< 20 μm
Wafer bumping	Low cost, pitch> 100 μm	Fine pitch and bumpless
Die attach		
Epoxy	■	
Tape	■	
Soldering		■
Polymer		■
Interconnects		
Wire bonding	Low loop bonding	/
Flip chip bump bonding	Mixed WB /FC	Size/pitch (>50 μm)
Face to face	/	Fine pitch (<10 μm) Thin interconnects
Bumpless/Seamless	Electroless	Thin film interconnects, fusion
Underfilling		
Via formation	Photo/drilling, laser	Through silicon etching, photo
Via metallization	Plating, electroless	Electroplating, CVD
Wiring	Substrate wiring (see chapter substrates)	Thin film redistribution
Encapsulation	Molding	Molding
		Wafer/wafer (glas) bonding

Legend: ■ most preferred used

18 Assembly and Packaging

Table 101a System-in-a-Package Requirements—Near-term Years *UPDATED*

Year of Production	2005	2006	2007	2008	2009	2010	2011	2012	2013
DRAM ½ Pitch (nm) (contacted)	80	70	65	57	50	45	40	36	32
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	90	78	68	59	52	45	40	36	32
MPU Physical Gate Length (nm)	32	28	25	22	20	18	16	14	13
Number of terminals—low cst handheld	600	600	700	800	800	800	800	800	800
IS Number of terminals—high performance (digital)		<u>2900</u>	<u>3050</u>	<u>3190</u>	<u>3350</u>	<u>3509</u>	<u>3684</u>	<u>3860</u>	<u>4053</u>
Number of terminals—maximum RF	200	200	200	200	200	200	200	200	200
Low cost handheld / #die / stack	6	6	7	8	9	10	11	12	13
high performance / die / stack	2	2	3	3	3	4	4	4	5
IS Low cost handheld / #die / SiP	6	8	8	8	9	11	12	13	14
high performance / #die / SiP	4	5	6	6	6	7	7	7	8
IS Minimum component size (micron)	<u>1005</u>	<u>1005</u>	<u>1005</u>	<u>600x300</u>	<u>600x300</u>	<u>400x200</u>	<u>400x200</u>	<u>400x200</u>	<u>200x100</u>
Maximum reflow temperature (°C)	260	260	260	260	260	260	260	260	260

Table 101b System-in-a-Package Requirements—Long-term Years *UPDATED*

Year of Production	2014	2015	2016	2017	2018	2019	2020
DRAM ½ Pitch (nm) (contacted)	28	25	22	20	18	16	14
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	28	25	22	20	18	16	14
MPU Physical Gate Length (nm)	11	10	9	8	7	6	6
Number of terminals—low cst handheld	800	800	800	800	800	800	800
IS Number of terminals—high performance (digital)	<u>4246</u>	<u>4458</u>	<u>4670</u>	<u>4904</u>	<u>5138</u>	<u>5394</u>	<u>5651</u>
Number of terminals—maximum RF	200	200	200	200	200	200	200
Low cost handheld / #die / stack	14	14	15	15	16	16	17
high performance / die / stack	5	5	6	6	6	7	7
IS Low cost handheld / #die / SiP	<u>14</u>	<u>14</u>	<u>15</u>	<u>15</u>	<u>16</u>	<u>16</u>	<u>17</u>
high performance / #die / SiP	8	8	9	9	9	10	10
IS Minimum component size (micron)	<u>200x100</u>	<u>200x100</u>	<u>200x100</u>	<u>200x100</u>	<u>200x100</u>	<u>200x100</u>	<u>200x100</u>
Maximum reflow temperature (°C)	260	260	260	260	260	260	260

Manufacturable solutions exist, and are being optimized

Manufacturable solutions are known

Interim solutions are known

Manufacturable solutions are NOT known

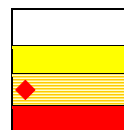


Table 102a Thinned Silicon Wafer Thickness 200 mm/300 mm—Near-term Years

Year of Production	2005	2006	2007	2008	2009	2010	2011	2012	2013
DRAM ½ Pitch (nm) (contacted)	80	70	65	57	50	45	40	36	32
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	90	78	68	59	52	45	40	36	32
MPU Physical Gate Length (nm)	32	28	25	22	20	18	16	14	13
Min. thickness of thinned wafer (general product)	75	70	65	60	55	50	45	40	40
Min. thickness of thinned wafer (For extreme thin package ex. Smart card)*	50	25	20	20	15	15	10	10	10

*Includes metallization and passivation

Table 102b Thinned Silicon Wafer Thickness 200 mm/300 mm—Long-term Years

Year of Production	2014	2015	2016	2017	2018	2019	2020
DRAM ½ Pitch (nm) (contacted)	28	25	22	20	18	16	14
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	28	25	22	20	18	16	14
MPU Physical Gate Length (nm)	11	10	9	8	7	6	6
Min. thickness of thinned wafer (general product)	40	40	40	40	40	40	40
Min. thickness of thinned wafer (For extreme thin package ex. Smart card)*	10	8	8	8	8	8	8

*Includes metallization and passivation

Manufacturable solutions exist, and are being optimized

Manufacturable solutions are known

Interim solutions are known

Manufacturable solutions are NOT known

