INTERNATIONAL
TECHNOLOGY ROADMAP
FOR
SEMICONDUCTORS

2006 UPDATE
FINAL DRAFT

FACTORY INTEGRATION

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FACTORY INTEGRATION[1]

SUMMARY

The 2006 Factory Integration section of the ITRS focuses on integrating all the factory components that are needed to efficiently produce the required products on schedule and in the right volumes while meeting cost targets. Realizing the potential of Moore's Law requires taking full advantage of device feature size reductions, new materials, yield improvement to near 100%, wafer size increases, other manufacturing productivity improvements and preserving the decades-long trend of 30% per year reduction in cost per function. To continue this pace requires the vigorous pursuit of the following fundamental manufacturing attributes: maintaining cost per unit area of silicon, decreasing factory ramp time, and increasing factory flexibility to changing technology and business needs.

Factory Integration addresses several challenges that threaten to slow the industry's growth, including:

1. Integrating complex business models with complex factories—Rapid changes in semiconductor technologies, business requirements, and the need for faster product delivery, high mix, and volatile market conditions are making it difficult for factories to effectively meet accelerated ramp and yield targets over time.
2. Production equipment reliability, utilization, and extendibility—Production equipment must keep up with availability and utilization targets, which has an enormous impact on capital and operating costs.
3. Maturing 300mm factory challenges— The semiconductor industry is now focusing on maturity of 300mm factories and hence 300mm efficiency must be improved and sustained while improving cost and cycle time targets. The ever-exploding factory data quantity and complexity need to be addressed as well.
4. Post Bulk CMOS and next wafer size manufacturing paradigm—Conversion to novel devices and the 450mm wafers represent key inflection points for semiconductor manufacturing and represents another opportunity to improve manufacturing cost effectiveness and the industry's ability to continue realizing Moore's law.

WHAT'S NEW FOR FACTORY INTEGRATION IN 2006?

The Factory Integration team completed minor updates to Operations, Equipment, Information & Control, AMHS and Facilities technology requirements tables. These changes corrected some of the errors from 2005 and also updated metric values that reflect the collective input from various members.

The team also worked on key focus areas such as: a) 300 Prime/450mm—defining requirements, constraints, partnerships with other efforts and timing, including, 300 Prime—to ensure current 300mm install base productivity improvements; b) proactive visualization—definition, impact due to high mix and small lot, factory metrics, intrinsic equipment loss through B/A metric and cycle time; c) design for facilities—adapter plate, power and water usage; d) equipment sleep mode—efforts kicked off to conserve power and time synchronization for factory applications.

In addition, Factory Integration worked with several other technology working groups (TWGs): Lithography, Front End Processes (FEP), Environment, Safety, & Health (ESH), Yield Enhancement, Assembly & Packaging, Test, Interconnect, and Metrology on cross-cut issues. Key topics were: extreme ultraviolet lithography (EUVL) requirements, the green fab initiative, 1.5mm wafer edge exclusion, adapter plate, fab humidity control, and single wafer versus batch processing for thermal processes and 450mm cross-cut issues.

In 2007, the Factory Integration team will continue to work on technology requirements, potential solutions (several updates were proposed in 2006 but are planned for insertion in 2007 since the team is working on supporting materials). The team will continue to work on key focus areas and with cross TWGs to address cross-cut issues in order to develop cogent technology requirements and potential solutions to enable our factories to effectively address the next business/manufacturing/technology challenges.

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[1] *Factory integration is the combination of factory operations, production equipment, facilities, material handling, factory information and control systems, and probe/test manufacturing working in a synchronized way to profitably produce complex products for a time-sensitive market*

Table 84a Factory Integration Difficult Challenges—Near-term

Difficult Challenges ≥32 nm	*Summary Of Issues*
Responding to rapidly changing, complex business requirements	Many new and co-existing business models including IDM, Foundry, Fabless, Joint Ventures, Collaborations, other Outsourcing, etc need to be considered in the Factory Integration Increased expectations by customers for faster delivery of new and volume products Need for improve integration of the entire product design and manufacturing process Faster design -> prototype and pilot -> volume production Enhanced customer visibility into outsourced production operations Reduced time to ramp factories, products, and processes to stay competitive within the rapidly changing business environment Building 30+ mask layer System on a Chip (SoC) with high mix manufacturing as the model in response to diversified customers' requirement Rapid and frequent factory plan changes driven by changing business needs Ability to model factory performance to optimize output and improve cycle time for high mix factories Ability to constantly adjust equipment loading to keep the factory profitable Manufacturing knowledge and control information need to be shared as required among disparate factories
Achieving growth targets while margins are declining	Implications of rising wafer, packaging, and other materials cost on meeting cost targets Meeting high factory yield much faster at startup Addressing increased complexity while keeping costs in check Reducing complexity and waste across the supply chain Inefficiencies introduced by non-product wafers (NPW) competing for resources with production wafers High cost and cycle time of mask sets for manufacturers impacting affordability of new product designs Increasing dedication of masks and equipment causing manufacturing inefficiencies Challenges introduced with sharing of mask sets Difficulty in maintaining the historical 0.7× transistor shrink per year for die size and cost efficiency
Managing ever increasing factory complexity	Quickly and effectively integrating rapid changes in process technologies Managing carriers with multiple lots, wafers with multiple products, or multiple package form factors Comprehending increased purity requirements for process and materials Need to run aluminum and copper back end in the same factory Increasing number of processing steps coupled with process and product complexity Need to concurrently manage new and legacy software and systems with increasingly high interdependencies Explosive growth of data collection/analysis requirements driven by process and modeling needs Increased requirements for high mix factories. Examples are complex process control as frequent recipe creation and changes at process tools and frequent quality control due to small lot sizes
Meeting factory and equipment reliability, capability or productivity requirements per the Roadmap	Process equipment not meeting availability, run rate, and utilization targets out of the box Stand alone and integrated reliability for equipment and systems to keep factories operating Increased impacts that single points of failure have on a highly integrated and complex factory Quality issues with production equipment embedded controllers to improve equipment process performance instability and NPW requirements Lack of good data to measure equipment and factory effectiveness for optimization and improvement programs Factory capacity planning and supply chain management systems are not continuously base lined with actual factory data creating errors Small process windows and tight process targets at >45nm in many modules make process control increasingly difficult Lack of migration paths which inhibit movement from old inefficient systems to new highly productive systems

Table 84b Factory Integration Difficult Challenges—Long-term

Difficult Challenges <32 nm	*Summary of Issues*
Meeting the flexibility, extendibility, and scalability needs of a cost-effective, leading-edge factory	Need to quickly convert factories to new process technologies while reusing equipment, facilities, and skills Minimizing downtime to on-going operations while converting factories to new technologies Scalability implications to meet large 300 mm factory needs [40K–50K WSPM] Continued need to improve both throughput and cycle time Reuse of building, production and support equipment, and factory information and control systems across multiple technology generations Understanding up-front costs to incorporate EFS (Extendibility, Flexibility and Scalability) Comprehending increased purity requirements for process and materials Accelerating the pace of standardization to meet industry needs
Meeting process requirements at 65nm and 45nm generations running production volumes	Small process windows and tight process targets at 45nm generations in many modules make process control increasingly difficult Complexity of integrating next generation lithography equipment into the factory Overall development and volume production timelines continuing to shrink Device and process complexity make the ability to trace functional problems to specific process areas difficult Difficulty in running different process parameters for each wafer while maintaining control windows and cycle time goals Reducing the impacts of parametric variation
Increasing global restrictions on environmental issues	Need to meet regulations in different geographical areas Need to meet technology restrictions in some countries while still meeting business needs Comprehending tighter ESH/Code requirements Lead free and other chemical and materials restrictions New material introduction
Post-conventional CMOS manufacturing uncertainty	Uncertainty of novel device types replacing conventional CMOS and the impact of their manufacturing requirements will have on factory design Timing uncertainty to identify new devices, create process technologies, and design factories in time for a low risk industry transition Potential difficulty in maintaining an equivalent 0.7× transistor shrink per year for given die size and cost efficiency Need to run CMOS and post CMOS processes in the same factory
Emerging factory paradigm and next wafer size change	Uncertainty about the next wafer size [450mm] and the conversion timing [See Backup material as a link in the electronic chapter at http://public.itrs.net.] Traditional strategies to scale wafers and carriers for the next wafer size conversion may not work with [450 mm] 25 wafer carriers and drive significant production equipment and material handling changes Uncertainty concerning how to reuse buildings, equipment, and systems to enable the next wafer size conversion [to 450 mm] at an affordable cost

TECHNOLOGY REQUIREMENTS

Table 85 Key Focus Areas and Issues for FI Functional Areas Beyond 2005

Functional Area	*Key focus and issues*
Factory Operations (FO)	1) Reduce mfg cycle times, 2) Improve Equipment Utilization, 3) Reduce Losses from High Mix.
Production Equipment (PE)	1) NPW reduction, 2) Reliability Improvement, 3) Run rate (throughput) improvement, 4) 1.5 mm wafer edge exclusion challenge.
Automated Material Handling Systems (AMHS)	1) Increase throughput for Traditional and Unified Transport, 2) Reduce Average Delivery times, 3) Improve Reliability
Factory Information and Control Systems (FICS)	1) Increase Reliability, 2) Increase Factory Throughput, 3) Reduce or Maintain Mask Shop Cycle Time, 4) Reduce Costs, 5) Improve product/wafer quality
Facilities	1) Factory Extendibility, 2) AMC, 3) Rapid Install/Qualification, 4) Reduce Costs

Table 86a Factory Operations Technology Requirements—Near-term Years UPDATED

	Year of Production	*2005*	*2006*	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*
	DRAM ½ Pitch (nm) (contacted)	*80*	*70*	*65*	*57*	*50*	*45*	*40*	*35*	*32*
	Wafer Diameter (mm)	*300*	*300*	*300*	*300*	*300*	*300*	*300*	*300*	*450*
	Non-hot lot (average of 94% lots)									
	Cycle time per mask layer (days).	**1.6**	**1.5**	**1.5**	**1.5**	**1.4**	**1.4**	**1.2**	**1.2**	**1.2**
	X-Factor [1]	**3.2**	**3.1**	**3.1**	**3.1**	**3.05**	**3.05**	**3.05**	**3.05**	**3.05**
	Hot lot (average top 5% of lots)									
IS	Cycle time per mask layer (days)	**0.62**	**0.55**	**0.55**	**0.55**	**0.51**	**0.51**	**0.47**	**0.47**	**0.47**
	X-Factor [1]	**1.4**	**1.3**	**1.3**	**1.3**	**1.3**	**1.3**	**1.2**	**1.2**	**1.2**
	Super hot lot (average top 1% of lots)									
	Cycle time per mask layer (days)	**0.33**	**0.32**	**0.32**	**0.32**	**0.31**	**0.31**	**0.3**	**0.3**	**0.3**
	High-mix capacity degradation	**11.67%**	**10%**	**8.33%**	**6.67%**	**5%**	**5%**	**5%**	**5%**	**5%**
	Bottleneck equipment [2] [3]									
IS	Utilization	**90%**	**92%**	**92%**	**92%**	**94%**	**94%**	**94%**	**94%**	**94%**
IS	Availability	**92%**	**94%**	**94%**	**94%**	**96%**	**96%**	**96%**	**96%**	**96%**
IS	Wafer layers/day/head count	**55**	**61**	**61**	**61**	**67**	**67**	**73**	**73**	**73**
	Number of lots per carrier (high mix) [4]	**Multiple**	**Multiple**	**Multiple**	**Multiple**	**Multiple**	**Multiple**	**Multiple**	**Multiple**	**Multiple**
	Facilities cycle time (months)									
IS	1st tool to 1st full loop wafer out	**3.5**	**3**	**3**	**2.5**	**2.5**	**2.5**	**2**	**2**	**2**
	Generation-to-generation change-over (weeks)	**13**	**12**	**12**	**12**	**11**	**11**	**10**	**10**	**10**
	Floor space effectiveness	**1×**	**1×**	**1×**	**1×**	**1×**	**1×**	**1×**	**1×**	**1×**
IS	Average number of wafers between reticle changes	**40**	**35**	**30**	**25**	**20**	**20**	**20**	**20**	**20**

Manufacturable solutions exist, and are being optimized	⬜
Manufacturable solutions are known	🟨
Interim solutions are known	◆
Manufacturable solutions are NOT known	🟥

Notes for Tables 86a and b:

[1] X-factor is shown for continuous improvement. Actual X-Factor values will depend heavily on raw process time for a given process technology or generation.

[2] A bottleneck tool usually refers to a lithography tool

[3] Utilization and Availability are shown for continuous improvement

[4] High mix is defined as the followings:

- *Running > three technology generation concurrently in the same Fab*

- *Running > ten process flows within the same technology generation*
- *Running > 50 products concurrently through the Fab*
- *Many of small lots of 1–10 wafers in size*
- *Running an average of < 50 wafers between Reticle changes for each lithography expose equipment*
- *Lot starts are based on customer orders. There is a daily variation in the number of lots you start with different products and process flows*
- *At least five large volume products (product flows) with no one product having >50% of production volume*

Table 86b Factory Operations Technology Requirements—Long-term Years

Year of Production	*2014*	*2015*	*2016*	*2017*	*2018*	*2019*	*2020*
DRAM ½ Pitch (nm) (contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
Wafer Diameter (mm)	*450*	*450*	*450*	*450*	*450*	*450*	*450*
Non-hot lot (average of 94% lots)							
Cycle time per mask layer (days).	1.13	1.13	1.13	1.05	1.05	1.05	1.05
X-Factor [1]	**3.05**	**3.05**	**3.05**	**3**	**3**	**3**	**3**
Hot lot (average top 5% of lots)							
Cycle time per mask layer (days)	**0.44**	**0.44**	**0.44**	**0.39**	**0.39**	**0.39**	**0.39**
X-Factor [1]	**1.2**	**1.2**	**1.2**	**1.1**	**1.1**	**1.1**	**1.1**
Super hot lot (average top 1% of lots)							
Cycle time per mask layer (days)	**0.3**	**0.3**	**0.3**	**0.3**	**0.3**	**0.3**	**0.3**
High-mix capacity degradation	**5%**	**5%**	**5%**	**5%**	**5%**	**5%**	**5%**
Bottleneck equipment [2] [3]							
Utilization	**94%**	**94%**	**94%**	**94%**	**94%**	**94%**	**94%**
Availability	**96%**	**96%**	**96%**	**96%**	**96%**	**96%**	**96%**
Wafer layers/day/head count	**81**	**81**	**81**	**89**	**89**	**89**	**89**
Number of lots per carrier (high mix) [4]	**Multiple**	**Multiple**	**Multiple**	**Multiple**	**Multiple**	**Multiple**	**Multiple**
Facilities cycle time (months)							
1st tool to 1st full loop wafer out (months)	**1.5**	**1.5**	**1.5**	**1**	**1**	**1**	**1**
Generation -to-generation change-over (weeks)	**9.5**	**9.5**	**9.5**	**9**	**9**	**9**	**9**
Floor space effectiveness	**1×**	**1×**	**1×**	**1×**	**1×**	**1×**	**1×**
Average number of wafers between reticle changes	**15**	**15**	**15**	**13**	**13**	**13**	**13**

Manufacturable solutions exist, and are being optimized	☐
Manufacturable solutions are known	🟨
Interim solutions are known	◆
Manufacturable solutions are NOT known	🟥

Explanation of Items for Factory Operations Requirements

Item	*Explanation*
Factory cycle time per mask layer (non-hot lot)	*Measure of total time to process a wafer lot per mask layer. Assume 25 wafers per lot. For example, if a process has 20 masking layers, and cycle time per mask layer is 1.5, then total factory (fabrication) cycle time is 20 × 1.5 = 30 days. A key metric of time to money.*
Factory cycle time per mask layer (hot lot)	*Same definition as of above. Factories typically prioritize these lots over non-hot lots. As a result, the cycle time for hot lots is < 50% of non-hot lots. Assume 25 wafers per lot. New product lots can be processed as hot lots*
Factory cycle time per mask layer (super-hot lot)	*Assume ~ five wafers per lot. Factories typically prioritize these lots over conventional lots, hold tools downstream to rapidly move them through the process flow and reduce sampling rates. As a result, the cycle time for super hot lots are shorter than hot lots.*
X-factor [1]	*X-factor is the total cycle time (queue time + hold time + raw process time + travel time) divided by the raw process time (RPT). Raw process time for a lot at a tool is the time it takes to process a lot on the tool. Generally this time will be from when the tool starts to process the lot (and thus cannot be moved to another tool for processing) until the lot is finished and can be moved to the next operation. Raw process time for a technology is the sum of the raw process times for each of the tools in the processes in the technology plus the total travel time. Raw process time is not shown in the technology table since X factor and cycle time per mask layers are shown.* *The relationship is: cycle time = raw process time × X-factor*

Item	Explanation
	Assume current cycle time is 1.6 days/mask level and the X-factor for normal lots is 3.2 at 80% utilization. Thus RPT for normal lots = 1.6/3.2 = 0.5 Assume same RPT for normal and hot lots. X-factor for hot lots is determined by "last-in-first-out" priority
High-mix capacity degradation	The penalty paid by factory operations in terms of lost capacity due to high mix (measured in %). This capacity loss is caused by reduced batch sizes, increased set ups, etc. This is the average for all tool sets in the line. Degradation increases from 5% (low mix, 25 wafers/FOUP, change recipe/setup every ten lots, single product on a wafer) to maximum. Of 15% (high-mix, <25 wafers/FOUP, change recipe/setup for every FOUP, multiple product in a lot). This metric impact the utilization of effective capacity, which is best, defined as being (1–(Idle No WIP)). Idle No WIP is the fraction of a tool's capacity that is idle when the tool is up and there is no WIP either waiting to be run on the tool or in transit to the tool. In some cases, No operator can also contribute to utilization of effective capacity.
Bottleneck equipment utilization and availability [2] [3]	Availability is defined in SEMI E10[2] as "the probability that the equipment will be in a condition to perform its intended function when required." Utilization is defined in SEMI E10 as "the percentage of time the equipment is performing its intended function during a specified time period." All based on 25-wafer lot. Availability includes setup, idle and processing time, utilization is considered as time directly adding value of constraint equipment (usually lithography tools) measured in % without sacrificing cycle time. Constraint equipment utilization (normally lithography) is the pulse of the Fab and usually determines the output capacity.
Wafer layers/day/head count	Measure of productivity that includes equipment output and direct labor staffing. Equation = total wafer processed per day in the factory × number of lithography mask layers/total number of direct labor employees per day.
Number of lots per carrier (high mix) [4]	The number of lots in each carrier that need to be tracked, monitored, and processed. For high-mix factories, the number of wafers can be <25 per lot and the production equipment must be able to run a different recipe and/or parameters for each wafer within the carrier. It also requires the factory information and control system to be able to track, monitor, and control the wafer at each point the factory and within the equipment. The factory information and control system must have the ability to drive the production equipment to run different recipes and/or parameters for each wafer. Multiple lots per carrier mean more than one product lot. High mix is at least five large volume products (product flows) with no one product has >50% of production volume.
Time to 1st wafer out time (months) –1st tool move-in to 1st full loop wafer out	A key metric of new factory ramp-up time. This is the time elapsed in months from first tool move-in to first full loop wafer out.
Generation-to-generation change-over (weeks)	The time in weeks for a new product or process to be implemented in a working factory (production equipment move-in to first lot out). About 80% of the current equipment is reused and 20% is new. Equipment already in place or available and may need to be qualified. Furnace and wet process equipment are not replaced. Not serial number 1 equipment
Floor space effectiveness	This is a measure of equipment installation density in the clean room, and drives the requirement for the smallest footprint and the fastest run rate for production equipment. Equation = (Number of processing steps in the Fab × WSPM/(floor space area × 30 days). For every major generation, one additional metal layer is added, and assuming a 4% increased run-rate improvement each year (by reduced processing time per wafer), the best that can be mathematically achieved is getting the same output per square meters of clean room for each new generation.
Average number of wafers between reticle changes	This is a measure of how efficiently high-product mix can be handled in the factory. As the metric indicates, it is the average number of wafers processed before a reticle is changed.

FOUP—front opening unified pod

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[2] *SEMI E10-0699E: Specification for Definition and Measurement of Equipment Reliability, Availability, and Maintainability (RAM).*

Table 87a Production Equipment Technology Requirements—Near-term Years

	Year of Production	*2005*	*2006*	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*
	DRAM ½ Pitch (nm) (contacted)	*80*	*70*	*65*	*57*	*50*	*45*	*40*	*35*	*32*
	Wafer Diameter (mm)	*300*	*300*	*300*	*300*	*300*	*300*	*300*	*300*	*450*
IS	Throughput improvement (run-rate) per year	**4%**	**4%**	**New base**	**4%**	**4%**	**New base**	**4%**	**4%**	**>0%**
	New non-product wafers (NPW) as a % of wafer starts per week	**<14%**	**<13%**	**<12%**	**<11%**	**<11%**	**<11%**	**<10%**	**<10%**	**<10%**
IS	Overall NPW activities versus production wafers activities	**10%**	**10%**	**7%**	**7%**	**5%**	**5%**	**5%**	**5%**	**5%**
	% capital equipment reused from previous node	**>90%**	**>90%**	**>90%**	**>90%**	**>90%**	**>90%**	**>90%**	**>90%**	**Limited**
	Wafer edge exclusion	**2 mm**	**2mm**	**1.5mm**	**1.5mm**	**1.5mm**	**1.5mm**	**1.5mm**	**1.5mm**	**1.5mm**
IS	Equipment lead time from setup to full throughput capable	**4 wks**	**4 wks**	**4 wks**	**4 wks**	**4 wks**	**4 wks**	**4 wks**	**4 wks**	**4 wks**
IS	Process equipment availability (A80)	**92%**	**92%**	**>92%**	**>94%**	**>95%**	**>95%**	**>95%**	**>95%**	**>95%**
	Metrology equipment availability (A80)	**96%**	**96%**	**96%**	**>96%**	**>97%**	**>98%**	**>98%**	**>98%**	**>98%**
IS	Intrinsic setup time reduction, versus base	**6%**	**6%**	**10%**	**12%**	**12%**	**15%**	**15%**	**17%**	**17%**
IS	Ability to run different recipes and parameters for each wafer	**Partial**	**Partial**	**Yes**	**Yes**	**Yes**	**Yes**	**Yes**	**Yes**	**Yes**
	248 nm lithography scanner productivity (wafers outs per week per tool)	**7400**	**7400**	**7700**	**7700**	**8000**	**8000**	**8000**	**8000**	**8000**
	193 nm lithography scanner productivity (wafers outs per week per tool)	**5300**	**5300**	**5600**	**5600**	**6000**	**6000**	**6000**	**6000**	**6300**
IS	Maximum allowed electrostatic field on wafer and mask surfaces (V/cm)	**90**	**80**	**70**	**63**	**55**	**50**	**44**	**38**	**35**

Manufacturable solutions exist, and are being optimized	⬜
Manufacturable solutions are known	🟨
Interim solutions are known	◆
Manufacturable solutions are NOT known	🟥

Table 87b Production Equipment Technology Requirements—Long-term Years

	Year of Production	*2014*	*2015*	*2016*	*2017*	*2018*	*2019*	*2020*
	DRAM ½ Pitch (nm) (contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
	Wafer Diameter (mm)	*450*	*450*	*450*	*450*	*450*	*450*	*450*
	Throughput improvement (run-rate) per year	**4%**	**4%**	**4%**	**4%**	**4%**	**4%**	**4%**
	New non-product wafers (NPW) as a % of wafer starts per week	**<9%**	**<9%**	**<9%**	**<9%**	**<9%**	**<9%**	**<9%**
	Overall NPW activities versus production wafers activities	**5%**	**5%**	**5%**	**5%**	**5%**	**5%**	**5%**
IS	% capital equipment reused from previous node	**Limited**	**>70%**	**>70%**	**>70%**	**>70%**	**>70%**	**>70%**
	Wafer edge exclusion	**1.5mm**	**1.5mm**	**1.5mm**	**1.5mm**	**1.5mm**	**1.5mm**	**1.5mm**
	Equipment lead time from setup to full throughput capable	**4 wks**	**4 wks**	**4 wks**	**4 wks**	**4 wks**	**4 wks**	**4 wks**
	Process equipment availability (A80)	**>95%**	**>95%**	**>95%**	**>95%**	**>95%**	**>95%**	**>95%**
	Metrology equipment availability (A80)	**>98%**	**>98%**	**>98%**	**>98%**	**>98%**	**>98%**	**>98%**
IS	Intrinsic setup time reduction, versus base	**> 17%**	**> 17%**	**>20%**	**>20%**	**>20%**	**>20%**	**>20%**
	Ability to run different recipes and parameters for each wafer	**Yes**	**Yes**	**Yes**	**Yes**	**Yes**	**Yes**	**Yes**
	248 nm lithography scanner productivity (wafers outs per week per tool)	**8000**	**8000**	**8000**	**8000**	**8000**	**8000**	**8000**
IS	193 nm lithography scanner productivity (wafers outs per week per tool)	**6300**	**6500**	**6500**	**6500**	**6500**	**6500**	**6500**
IS	Maximum allowed electrostatic field on wafer and mask surfaces (V/cm)	**31**	**28**	**25**	**22**	**20**	**18**	**15**

Manufacturable solutions exist, and are being optimized	⬜
Manufacturable solutions are known	🟨
Interim solutions are known	◆
Manufacturable solutions are NOT known	🟥

Explanation of Items for Production Equipment Requirements

Item	*Explanation*
Throughput improvement (run-rate) per year (high mix)	Throughput improvements are achieved by reducing the processing time per wafer, and optimizing non-value added wafer handling and wafer-staging steps inside the equipment and by increasing the efficiency of the equipment embedded controller. Also eliminate any dead time between sequential wafer processing steps. If current run-rate is 100 wafers/hour, the required run-rate next year is (100 × 1.04) = 104 wafers/hour and (104 × 1.04) = 108 wafers/hour the following year.
New non-product wafers (NPW) as a % of wafer starts per week	Ratio of new non-production wafer consumption divided by total production wafer started for the same period. Typical non-product wafers include test wafers, monitor wafers, calibration wafers, dummy wafers.
Overall NPW activities versus production wafers activities	Ratio of total non-production wafer activities (process moves, including recycling wafers) divided by total production wafer activities for the same period. Typical non-product wafers include test wafers, monitor wafers, calibration wafers, dummy wafers. Consumption quantity includes both new and reused (reclaimed) non-product wafers.
% capital equipment reused from previous generation	% of capital (production) equipment quantity that is reused from generation N to N+1. Example: if X number of production equipment of generation N can be reused for generation N+1 and the total number of production equipment for generation N+1 is Y, then equipment reuse % is defined as X/Y.
Wafer edge exclusion	Dimension in millimeters measured from wafer edge that is not used for printing saleable chips. Includes front and rear sides of wafer.
Equipment lead time from setup to full throughput capable	Time elapsed between when tool has been installed and production ready till the time the equipment has been qualified to run wafers at the quoted throughput (wafers per hour). This is specifically applicable for lithography tools (worst case).
Process availability (A_{80})	Availability is 100% minus (scheduled downtime % – setup% + unscheduled downtime %) of the process (non-metrology) equipment (80% percentile). Scheduled downtime and unscheduled downtimes are defined in SEMI E10.
Metrology availability (A_{80})	Availability is 100% minus (scheduled downtime % – setup% + unscheduled downtime %) of the process (non-metrology) equipment (80% percentile). Scheduled downtime and unscheduled downtimes are defined in SEMI E10.
Intrinsic setup time reduction year to year	Intrinsic setup time reduction is mainly dependent on improvements to process equipment with quick setup capability (software, hardware improvements) and faster qualification capability. This metric will impact capacity.
Ability to run different recipes and parameters for each wafer	Ability for production equipment to run a different recipe and/or parameters for each wafer within a carrier. This facilitates the ability to have multiple lots per carrier. Base requirements also include the ability to track, monitor, and control the wafer at each point the factory or within the equipment. For production equipment, it impacts the extent of “recipe cascading” that enables equipment to run in a continuous (non-stop) mode between lots in the same carrier and between sequential carriers.
248 nm lithography scanner productivity (wafers outs per week)	The average number of good photo wafer alignments performed per machine per work day, considering only photo wafer alignments performed on 248 nm scanners in the Fab.
193 nm lithography scanner productivity (wafers outs per week)	The average number of good photo wafer alignments performed per machine per work day, considering only photo wafer alignments performed on 193 nm scanners in the Fab.
Maximum allowed electrostatic field on wafer and mask surfaces (V/cm)	Wafer and mask surface electric fields measured when they are removed from their carriers. Refer SEMI standards E78[3] and E43[4] for measurement methods.

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[3] *SEMI E78: Electrostatic Compatibility – Guide to Assess and Control Electrostatic Discharge (ESD) and Electrostatic Attraction (ESA) for Equipment.*

[4] *SEMI E43: Guide for Measuring Static Charge on Objects and Surfaces.*

Table 88a Material Handling Systems Technology Requirements—Near-term Years UPDATED

	Year of Production	*2005*	*2006*	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*
	DRAM ½ Pitch (nm) (contacted)	*80*	*70*	*65*	*57*	*50*	*45*	*40*	*35*	*32*
	Wafer Diameter (mm)	*300*	*300*	*300*	*300*	*300*	*300*	*300*	*450*	*450*
IS	Transport E-MTTR (minutes) per SEMI E10	**10**	**10**	**10**	**10**	**10**	**10**	**10**	**5**	**5**
	Storage E-MTTR (minutes) per SEMI E10	**25**	**25**	**20**	**20**	**20**	**20**	**20**	**20**	**20**
IS	Transport MMBF	**8,000**	11,000	**15,000**	**25,000**	**35,000**	**35,000**	**35,000**	**45,000**	**45,000**
IS	Storage MCBF	**25,000**	35,000	**45,000**	**55,000**	**60,000**	**60,000**	**60,000**	**70,000**	**70,000**
	Peak system throughput (40K WSPM)									
IS	Interbay transport (moves/hour)	**2250**	**2250**	**2575**	**2660**	**2660**	**2660**	**2660**	**2660**	**2660**
IS	Intrabay transport (moves/hour) — high throughput bay	**250**	**250**	**270**	**280**	**290**	**300**	**300**	**300**	**300**
IS	Transport (moves/hour)—unified system	**4240**	**4740**	**4900**	**5000**	**5000**	**5000**	**5000**	**5000**	**5000**
IS	Stocker cycle time (seconds) (100 bin capacity)	**12**	**12**	**12**	**12**	**12**	**12**	**12**	**12**	**12**
IS	Average delivery time (minutes)	**6**	**5**	**5**	**5**	**5**	**5**	**5**	**5**	**5**
IS	Peak delivery time (minutes)	**12**	**12**	**10**	**10**	**10**	**10**	**10**	**10**	**10**
IS	Hot lot average delivery time (minutes)	**3**	**3**	**2**	**2**	**2**	**2**	**2**	**2**	**2**
IS	AMHS lead time (weeks)	**12**	**12**	**<8**	**<8**	**<8**	**<8**	**<8**	**<8**	**<8**
IS	AMHS install time (weeks)	**24**	**24**	**<10**	**<10**	**<10**	**<10**	**<10**	**<10**	**<10**
IS	Downtime to extend system capacity when previously planned (minutes)	**120**	**120**	**<15**	**<15**	**0**	**0**	**0**	**0**	**0**
IS	Time required to integrate process tools to AMHS (minutes per LP)	**15**	**15**	**12**	**10**	**10**	**5**	**5**	**5**	**5**

Table 88b Material Handling Systems Technology Requirements—Long-term Years UPDATED

	Year of Production	*2014*	*2015*	*2016*	*2017*	*2018*	*2019*	*2020*
	DRAM ½ Pitch (nm) (contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
	Wafer Diameter (mm)	*450*	*450*	*450*	*450*	*450*	*450*	*450*
IS	Transport E-MTTR (minutes) per SEMI E10	**5**	**5**	**5**	**5**	**5**	**5**	**5**
	Storage E-MTTR (minutes) per SEMI E10	**20**	**15**	**15**	**15**	**10**	**10**	**10**
	Transport MMBF	**45,000**	**55,000**	**55,000**	**55,000**	**65,000**	**65,000**	**65,000**
IS	Storage MCBF	**70,000**	**80,000**	**80,000**	**80,000**	**100,000**	**100,000**	**100,000**
	Peak system throughput (40K WSPM)							
	Interbay transport (moves/hour)	**2660**	**2660**	**2660**	**2660**	**2660**	**2660**	**2660**
	Intrabay transport (moves/hour) — high throughput bay	**300**	**300**	**300**	**300**	**300**	**300**	**300**
	Transport (moves/hour)—unified system	**5000**	**5000**	**5000**	**5000**	**5000**	**5000**	**5000**
IS	Stocker cycle time (seconds) (100 bin capacity)	**12**	**12**	**12**	**12**	**12**	**12**	**12**
	Average delivery time (minutes)	**5**	**5**	**5**	**5**	**5**	**5**	**5**
	Peak delivery time (minutes)	**10**	**10**	**10**	**10**	**10**	**10**	**10**
	Hot lot average delivery time (minutes)	**2**	**2**	**2**	**2**	**2**	**2**	**2**
	AMHS lead time (weeks)	**<8**	**<8**	**<8**	**<8**	**<8**	**<8**	**<8**
	AMHS install time (weeks)	**<10**	**<10**	**<10**	**<10**	**<10**	**<10**	**<10**
IS	Downtime to extend system capacity when previously planned (minutes)	**0**	**0**	**0**	**0**	**0**	**0**	**0**
	Time required to integrate process tools to AMHS (minutes per LP)	**5**	**5**	**5**	**5**	**5**	**5**	**5**

Manufacturable solutions exist, and are being optimized	⬜
Manufacturable solutions are known	🟨
Interim solutions are known	◆
Manufacturable solutions are NOT known	🟥

Explanation of Items for Material Handling Systems Requirements

Item	*Explanation*
Transport E-MTTR (min per SEMI E10)	*Mean time to repair equipment-related failures (AMHS Transport); the average time to correct an equipment-related failure and return the equipment to a condition where it can perform its intended function; the sum of all equipment-related failure time (elapsed time, not necessarily total man hours) incurred during a specified time period (including equipment and process test time, but not maintenance delay downtime), divided by the number of equipment-related failures during that period.* *Notes: Refers to unscheduled, supplier dependent failures. Includes interbay and intrabay transport systems. Offline repair of components is not included in this time. Includes embedded software control systems (transport controllers). Does not include storage AMHS equipment or errors induced by the storage equipment. Does not include load port, FOUP carrier, or MES level software issues. Does not include reticle system.*
Storage E-MTTR (min per SEMI E10)	*Mean time to repair equipment-related failures (AMHS Storage); the average time to correct an equipment-related failure and return the equipment to a condition where it can perform its intended function; the sum of all equipment-related failure time (elapsed time, not necessarily total man hours) incurred during a specified time period (including equipment and process test time, but not maintenance delay downtime), divided by the number of equipment-related failures during that period.* *Notes: Refers to unscheduled, supplier dependent failures. Includes storage equipment load ports and embedded software. Does not include interbay or intrabay transport or incidents induced by these errors. Does not include FOUP carrier or MES level software issues. Does not include reticle system.*
Transport MMBF (mean move between failure)	*Average number cycles (delivery from pt A-pt.B) made by AMHS interbay or intrabay transport equipment before a person has to intervene to fix a failure. Number of transport moves / Number of supplier dependent unscheduled failures. Reference transport MPH definition for details on move.*
Storage MCBF (mean cycle between failure)	*Average number cycles (delivery from point A to point B) made by AMHS storage equipment before a person has to intervene to fix a failure. Number of storage cycles / Number of supplier dependent unscheduled failures per quarter. Reference cycle time definition for details on stocker cycle.*
Interbay transport (moves/hour)	*Number of material handling moves per hour performed by the interbay transport system. An interbay transport move is defined as a carrier move from the loading of an interbay system at a stocker interbay port to the unloading of the same Load at the destination stocker. Moves are counted by the Host (MCS).*
Intrabay transport (moves/hour)	*Number of material handling moves per hour performed by an intrabay transport loop. An intrabay transport move is defined as a carrier move between loadports (between stocker ports and production equipment load port, between two production equipment load ports). Moves are counted by the Host (MCS).*
Tool-to-Tool Direct transport (moves/hour) – Unified system	*A transport move is defined as a transfer of a carrier between any two loadports (stocker, process tool or transfer point between transport systems). Note that stocker robot moves from/to load ports are not assumed concurrent with nor included in system throughput moves. Moves are counted by the Host (MCS).*
Stocker cycle time (seconds) (100 bin capacity)	*Stocker cycle time is defined as the time (in seconds) from when the Host(MCS) issues the move command to the time the stocker signals completion with the move complete command to the host. The physical motion is the stocker internal robot moving to a carrier at a port or storage bin, picking up the carrier, and delivering it to another port or storage bin within the same stocker. Stocker cycle time shall be determined as the average of several different types of moves over a period of time. The moves should include all ports and all shelf locations. Each move needs to alternate between different carriers. The maximum MCS communication time is assumed to be 1 second.*
Average delivery time (minutes)	*The time begins at the request for carrier movement from the MES and ends when the carrier arrives at the load port of the receiving equipment.*
Peak delivery time (minutes)	*Peak delivery time is considered the peak performance capability defined as the average delivery time plus two standard deviations.*
Hot lot average delivery time (min)	*Reference definition for Average Delivery Time. Reference Factory Operations section for further details on hot lots.*
AMHS lead time (weeks)	*Time elapsed, in weeks, between when a purchase order has been placed for a material handling system until the time the first shipment is FOB at supplier's dock. This assumes that at the time of PO placement the equipment configuration is fixed. This lead time should not be affected by market demand on supplier.*
AMHS install time (weeks)	*Time elapsed, in weeks, between when the first component of the system is moved in from the dock until the final component is fully installed, started up, and tested to meet full designed throughput capability. Assume new factory and uninterrupted installation of the material handling system (assume no facility, MCS or tool delays). Based on 20K WSPM fab of approximately 200 meters by 80 meters, with 15–20 short bays. Does not include reticle systems.*
Downtime to extend system capacity when previously planned (minutes)	*Impact to material handling system in terms of downtime, in minutes, of the material handling system, required for making connections to system track extensions or a new storage when previsions for this expansion were incorporated in the original design.*
Time required to integrate process tools to AMHS (minutes per LP)	*The Downtime to the transport system when a process tool is integrated to the AMHS. Addition of tool occurs on a track with existing vehicle traffic (no bypass units around tools). Assume tool is placed correctly and physical tool move in does not impact the AMHS. System not stopped for PIO install (tool side). Time includes: Hardware install on track, teaching LP, Software updates, Delivery Testing. Scope ends when all vehicles have capability to deliver to new LP.*

Table 89a Factory Information and Control Systems Technology Requirements—Near-term Years
UPDATED

	Year of Production	*2005*	*2006*	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*
	DRAM ½ Pitch (nm) (contacted)	*80*	*70*	*65*	*57*	*50*	*45*	*40*	*35*	*32*
	Wafer Diameter (mm)	*300*	*300*	*300*	*300*	*300*	*300*	*300*	*300*	*450*
	Availability of mission critical applications (% per year)	99.98	99.986	99.987	99.99	99.991	99.991	99.994	99.994	99.994
	Downtime of mission critical applications (minutes per year)	105 min	75 min	75 min	68 min	53 min	45 min	30 min	30 min	30 min
ADD	**Factory down due to unscheduled FICS downtime due to FICS (minutes per year)**		120 min	90 min	90 min	60 min	60 min	61 min	60 min	60 min
	Full factory down due to unscheduled FICS downtime (minutes per year)	120 min	60 min	60 min	60 min	<15 min	< 15 min	< 15 min	<15 min	<15 min
ADD	**Factory down due to scheduled FICS downtime (minutes per year)**		180 min	180 min	120 min	120 min	120 min	60 min	60 min	60 min
	Full factory down due to scheduled FICS downtime (minutes per year)	180 min	180 min	180 min	120 min	120 min	120 min	60 min	60 min	60 min
	Mean time to recover for mission critical applications (minutes down per year)	30	15	<15	<15	<15	<15	<15	<15	<15
IS	MCS design to support peak number of AMHS transport moves (moves/hr)	12.7	14.2K	14.7K	15K	15K	15K	15K	15K	15K
IS	FICS design to support peak number of AMHS direct transport moves (moves/hr)	1270	1420	1470	1500	1500	1500	1500	1500	1500
	Time to send and load tape-out data into mask shop data system (hours)	6–12	6–12	6–12	6–12	6–12	6–12	6–12	6–12	6–12
	Time for OPC calculations and data preparation for mask writer (days)	4–8	4–8	4–8	4–8	4–8	4–8	4–8	4–8	4–8
	Time for OPC calculations only (days)	3–6	3–6	3–6	3–6	3–6	3–6	3–6	3–6	3–6
	% Factory information and control systems reusable for next generation	>93%	>93%	>93%	>93%	>93%	>93%	>93%	>93%	>93%
ADD	**Ability to run/adjust different recipes/parameters within a run**		Partial	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	Wafer-level recipe/parameter adjustment	Partial	Partial	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	Within-wafer recipe/parameter adjustment	Partial	Partial	Partial	Yes	Yes	Yes	Yes	Yes	Yes

Manufacturable solutions exist, and are being optimized	⬜
Manufacturable solutions are known	🟨
Interim solutions are known	◆
Manufacturable solutions are NOT known	🟥

Table 89b Factory Information and Control Systems Technology Requirements—Long-term Years *UPDATED*

	Year of Production	*2014*	*2015*	*2016*	*2017*	*2018*	*2019*	*2020*
	DRAM ½ Pitch (nm) (contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
	Wafer Diameter (mm)	*450*	*450*	*450*	*450*	*450*	*450*	*450*
	Availability of mission critical applications (% per year)	**99.999**	**99.999**	**99.999**	**99.999**	**99.999**	**99.999**	**99.999**
IS	Downtime of mission critical applications (minutes per year)	**8 min**	**8 min**	**8 min**	**4 min**	**4 min**	**4 min**	**4 min**
ADD	**Factory down due to unscheduled FICS downtime due to FICS (minutes per year)**	**30 min**	**30 min**	**15 min**	**15 min**	**15 min**	**15 min**	**15 min**
	Full factory down due to unscheduled FICS downtime (minutes per year)	**<15 min**	**<15 min**	**<15 min**	**<15 min**	**<15 min**	**<15 min**	**<15 min**
ADD	**Factory down due to scheduled FICS downtime (minutes per year)**	**0 min**	**0 min**	**0 min**	**0 min**	**0 min**	**0 min**	**0 min**
	Full factory down due to scheduled FICS downtime (minutes per year)	**0 min**	**0 min**	**0 min**	**0 min**	**0 min**	**0 min**	**0 min**
IS	Mean time to recover for mission critical applications (minutes down per year)	**5**	**5**	**5**	**2**	**2**	**2**	**2**
IS	MCS design to support peak number of AMHS transport moves (moves/hr)	**15K**	**15K**	**15K**	**15K**	**15K**	**15K**	**15K**
IS	FICS design to support peak number of AMHS direct transport moves (moves/hr)	**1500**	**1500**	**1500**	**1500**	**1500**	**1500**	**1500**
IS	Time to send and load tape-out data into mask shop data system (hours)	**6–12**	**6–12**	**6–12**	**6–12**	**6–12**	**6–12**	**6–12**
IS	Time for OPC calculations and data preparation for mask writer (days)	**4–8**	**4–8**	**4–8**	**4–8**	**4–8**	**4–8**	**4–8**
IS	Time for OPC calculations only (days)	**3–6**	**3–6**	**3–6**	**3–6**	**3–6**	**3–6**	**3–6**
IS	% Factory information and control systems reusable for next generation	**>93%**	**>93%**	**>93%**	**>80%**	**>80%**	**>80%**	**>80%**
ADD	**Ability to run/adjust different recipes/parameters within a run**	**Yes**	**Yes**	**Yes**	**Yes**	**Yes**	**Yes**	**Yes**
	Wafer-level recipe/parameter adjustment	**Yes**	**Yes**	**Yes**	**Yes**	**Yes**	**Yes**	**Yes**
	Within-wafer recipe/parameter adjustment	**Yes**	**Yes**	**Yes**	**Yes**	**Yes**	**Yes**	**Yes**

Manufacturable solutions exist, and are being optimized	⬜
Manufacturable solutions are known	🟨
Interim solutions are known	◆
Manufacturable solutions are NOT known	🟥

Explanation of Items for Factory Information and Control Systems Requirements

Item	*Explanation*
Availability of mission critical application (% per year) *Downtime of mission critical application (minutes per year)*	*Availability (A) is 100% minus (scheduled downtime % + unscheduled downtime %). Scheduled downtime and unscheduled downtimes are defined in SEMI E10.*
Full Factory Down Incidents (per year)	*Number of full factory downtime incident per year for mission critical system due to downtime of mission critical applications. Mission critical applications are those that are required to keep the entire wafer factory operational. Depending on factory configuration, these include: MES, Scheduler / Dispatcher, MCS, Cell Controller, SPC, Reticle system, Facilities Control Systems.*
Mean Time to Recover for mission critical applications (minutes)	*Mean time to recover a mission critical application following an unscheduled downtime. Mission critical applications within the factory information and control systems are those that are required to keep the entire wafer factory operational. Mean time to recover is measured in minutes per incident.*
Availability of the total factory system (% per year) *Factory down due to unscheduled FICS (minutes per year)* *Factory down due to scheduled FICS downtime (minutes per year)*	*Availability (Ai) is 100% minus (scheduled downtime % + unscheduled downtime %) for each mission critical factory information and control system applications. Scheduled downtime and unscheduled downtimes are defined in SEMI E10. The total availability of the factory = [A1 * A2 * A3 * A4]. The metric values assume that there are up to 4 mission critical applications within a factory.*
Peak number of AMHS transport moves supported by material control system (moves/hr)	*Maximum number of transport moves per hour supported by Material Control System (MCS). Able to support: peak # of moves for unified transport system * 1.5 (to translate to separate interbay/intrabay system) * 2 (safety factor for FICS)*
Peak number of Direct Transport moves (moves/hr)	*Target number of Direct Transport moves per hour supported by FICS. Direct Transport moves are defined as carrier moves directly from one production equipment tool load port to another production equipment tool load port. Assume 10% of peak number of transport moves will require Direct Transport*
Time to send and load tape-out data into Mask Shop data system	*Time in hours to send data from mask designer to mask shop's OPC application.*
Time for OPC calculations and data preparation for mask writer (days) *OPC Time only (days)*	*Time in hours to perform OPC calculations + Time in hours to convert the output of the OPC engine to the format the mask writer understands + Time in hours to transmit the data into the mask writing system* *Time for OPC calculations only is the time in hours to perform the OPC calculations once the OPC application has received the tape-out data from the mask designer*
% Factory information and control systems reusable for next generation	*Percentage of factory information and control systems (both computer hardware and software) that is reused from process technology generation to process technology generation, measured in cost.*
Ability to adjust recipes/parameters within a run	*Ability for Factory Information and Control systems to run a different recipe and/or parameters for each wafer within a carrier. This facilitates the ability to have multiple lots per carrier. Base requirements also include the ability to track, monitor, and control the wafer at each point the factory or within the equipment.*

Table 90a Facilities Technology Requirements—Near-term Years UPDATED

	Year of Production	*2005*	*2006*	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*
	DRAM ½ Pitch (nm) (contacted)	*80*	*70*	*65*	*57*	*50*	*45*	*40*	*35*	*32*
	Wafer Diameter (mm)	*300*	*300*	*300*	*300*	*300*	*300*	*300*	*450*	*450*
	Manufacturing (cleanroom) area/wafer starts per month (m^2/WSPM) (low mix only)	**0.34**	**0.34**	**0.34**	**0.34**	**0.34**	**0.34**	**0.34**	**0.34**	**0.34**
	SubFab to Fab ratio	**1**	**1**	**0.75**	**0.75**	**0.75**	**0.75**	**0.75**	**0.75**	**0.75**
	Facility sevice life (in three-year nodes)	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**
IS	Facility cleanliness level (ISO 14644) [1]	**Class 6 at rest**	**Class 6**	**Class 6**	**Class 6**	**Class 6**	**Class 6**	**Class 6**	**Class 7**	**Class 7**
	Facility cleanliness level (Airborne molecular contamination AMC) - ppt M	Discussed in Yield Enhancement Tables								
	Facility critical vibration areas (lithography, metrology, other) (micrometers per second) [2]	**6.25 (VC D)**	**6.25 (VC D)**	**6.25 (VC D)**	**6.25 (VC D)**	**6.25 (VC D)**	**6.25 (VC D)**	**6.25 (VC D)**	**6.25 (VC D)**	**6.25 (VC D)**
	Facility non-critical vibration areas (micrometers per second) [2]	**50 (VC A)**	**50 (VC A)**	**50 (VC A)**	**50 (VC A)**	**50 (VC A)**	**50 (VC A)**	**50 (VC A)**	**50 (VC A)**	**50 (VC A)**
	Maximum allowable electrostatic field on facility surfaces (V/cm)	**90**	**80**	**70**	**63**	**55**	**50**	**44**	**38**	**35**
	Gas, water, chemical purity	Discussed in Yield Enhancement Chapter								
	Factory construction time from groundbreaking to first tool move-in (months)	**10**	**9**	**9**	**9**	**8**	**8**	**9**	**9**	**9**
	Production equipment install and qualification cost as a % of capital cost	**8%**	**8%**	**7%**	**7%**	**6%**	**6%**	**5%**	**8%**	**8%**
	Facility operating cost (including utilities) as a % of total operating cost	**13%**	**13%**	**13%**	**13%**	**13%**	**13%**	**13%**	**13%**	**13%**
	Utility cost per total factory operating cost (%)	**3%**	**3%**	**3%**	**3%**	**3%**	**3%**	**3%**	**3%**	**3%**
	Power, water, and chemical consumption	Discussed in ESH Chapter								
ADD	Energy ConsumptionTotal Fab Support System (kWh/cm^2 per wafer out)	**-**	**0.55**	**0.55**	**0.50**	**0.50**	**0.45**	**0.40**	**0.50**	**0.50**

Manufacturable solutions are known	🟨
Interim solutions are known	◆
Manufacturable solutions are NOT known	🟥

Table 90b Facilities Technology Requirements—Long-term Years UPDATED

	Year of Production	*2014*	*2015*	*2016*	*2017*	*2018*	*2019*	*2020*
	DRAM ½ Pitch (nm) (contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
	Wafer Diameter (mm)	*450*	*450*	*450*	*450*	*450*	*450*	*450*
	Manufacturing (cleanroom) area/wafer starts per month (m^2/WSPM) (low mix only)	**0.34**	**0.34**	**0.34**	**0.34**	**0.34**	**0.34**	**0.34**
	SubFab to Fab ratio	**0.75**	**0.75**	**0.75**	**0.75**	**0.75**	**0.75**	**0.75**
	Facility sevice life (in three-year nodes)	**3**	**3**	**3**	**3**	**3**	**3**	**3**
IS	Facility cleanliness level (ISO 14644) [1]	**Class 7**	**Class 7**	**Class 7**	**Class 7**	**Class 7**	**Class 8**	**Class 8**
	Facility cleanliness level (Airborne molecular contamination AMC) - ppt M	Discussed in Yield Enhancement Chapter						
	Facility critical vibration areas (lithography, metrology, other) (micrometers per second) [2]	**6.25 (VC D)**	**6.25 (VC D)**	**6.25 (VC D)**	**6.25 (VC D)**	**6.25 (VC D)**	**6.25 (VC D)**	**6.25 (VC D)**
	Facility non-critical vibration areas (micrometers per second) [2]	**50 (VC A)**	**50 (VC A)**	**50 (VC A)**	**50 (VC A)**	**50 (VC A)**	**50 (VC A)**	**50 (VC A)**
	Maximum allowable electrostatic field on facility surfaces (V/cm)	**31**	**28**	**25**	**22**	**20**	**18**	**15**
	Gas, water, chemical purity	Discussed in Yield Enhancement Chapter						
	Factory construction time from groundbreaking to first tool move-in (months)	**9**	**9**	**8**	**8**	**8**	**8**	**8**
	Production equipment install and qualification cost as a % of capital cost	**8%**	**7%**	**7%**	**6%**	**6%**	**5%**	**5%**
	Facility operating cost (including utilities) as a % of total operating cost	**13%**	**13%**	**13%**	**13%**	**13%**	**13%**	**13%**
	Utility cost per total factory operating cost (%)	**3%**	**3%**	**3%**	**3%**	**3%**	**3%**	**3%**
	Power, water, and chemical consumption	Discussed in ESH Chapter						
ADD	Energy ConsumptionTotal Fab Support System (kWh/cm^2 per wafer out)	**0.50**	**0.45**	**0.45**	**0.40**	**0.40**	**0.35**	**0.35**

Manufacturable solutions exist, and are being optimized	⬜
Manufacturable solutions are known	🟨
Interim solutions are known	◆
Manufacturable solutions are NOT known	🟥

Explanation of Items for Facilities requirements:

Item	*Explanation*
Manufacturing (cleanroom) area/wafer starts per month (m^2/WSPM)	*"Manufacturing (cleanroom) area" is defined as the space in square meters containing the process and metrology equipment used for direct manufacturing processes such as photolithograph, diffusion, etch, thin films, CMP, excluding subFab spaces containing support equipment and facility infrastructure systems.*
Wafer starts per month (WSPM)	*Wafer starts per month is defined as the number of new 300mm wafers introduced into production for processing during a given 30 day period*
Sub-Fab to Fab ratio	*"Sub-Fab to Fab ratio" is defined as the footprint of the production equipment support plan area to the manufacturing area above. Relates to and extends factory operations "floor space effectiveness."*
Facility service life (in three-year generations)	*Facility service (system) life is the number of generations (process changes) that the system is available before major renovation is required to meet process requirements.*
Facility cleanliness class (ISO 14644)	*Cleanliness classification of wafer factory manufacturing (cleanroom) area as defined by ISO 14644-1.*
Facility critical vibration areas (litho, metro, other) (micrometers per second)	*"Vibration critical" is defined as area of the primary manufacturing floor in which a significant portion of the equipment is highly sensitive to floor vibration, the mitigation was not provided at the tool itself, and excessive vibrations can have serious deleterious effects on product. Extensive measures may be required in the facility's structural and mechanical equipment design based upon the needs of this space category. Vibration criteria are limits on vibration amplitudes at the floor or other support of a tool, given as VC-x, where x is a letter designation from A through E, each corresponding to a specific vibration amplitude spectrum. Refer to IEST-RP-DTE012.1[5] for definition of amplitudes, measurement methods, and signal processing requirements*
Facility non-critical vibration areas (micrometers per second)	*"Vibration non-critical" is defined as area of the primary manufacturing floor in which all or some of the equipment is only moderately vibration sensitive, and the structural system performance can be reduced. Vibration criteria are limits on vibration amplitudes at the floor or other support of a tool, given as VC-x, where x is a letter designation from A through E, each corresponding to a specific vibration amplitude spectrum. Refer to IEST-RP-DTE012.1 for definition of amplitudes, measurement methods, and signal processing requirements.*
Maximum allowable electrostatic field on facility surfaces (V/cm)	*Facility surface electric field limits apply to all factory materials-construction materials, furniture, people, equipment and carriers Refer to SEMI standards E129[6], E78[7] and E43[8] for measurement methods.*
Factory construction time from groundbreaking to first tool move-in (months)	*Factory construction time is defined as the period of time in months from first concrete placement to the time that the first tool is moved into the manufacturing area and is ready for hookup, i.e., building systems have passed inspection sufficient to begin the tool installation process.*
Production equipment install and qualification cost as a % of total capital cost	*"Production equipment installation cost" is defined as the cost of all labor and materials necessary to accept, move-in, and connects production equipment to the facility infrastructure systems to make the production equipment operational. This includes qualification, but excludes facility infrastructure systems and upgrades, and the cost of the production equipment.*
Total Capital Cost	*Total Capital Cost is defined as all labor and material costs necessary to complete a new semiconductor factory including production equipment and facility capital cost. This excludes costs for land.*
Facility operating cost (inc. utilities) as a % of total factory operating cost	*"Facility operating cost" is defined as all facility expenses directly related to supporting manufacturing including depreciation, utility, labor and maintenance costs.*
Utility cost per total factory operating cost (%)	*"Utility cost" is defined as the cost of power, water, gases, and chemicals required to support manufacturing, including the factory material and consumables.*
Total Factory Operating Cost	*Total Factory Operating cost is defined as the total annual operating expenses necessary for operating the factory including depreciation, materials, maintenance, and labor.*

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[5] *IEST-RP-DTE012.1: Handbook for Dynamic Data Acquisition and Analysis.*

[6] *SEMI E129: Guide to Assess and Control Electrostatic Charge in A Semiconductor Manufacturing Facility.*

[7] *SEMI E78: Electrostatic Compatibility – Guide to Assess and Control Electrostatic Discharge (ESD) and Electrostatic Attraction (ESA) for Equipment.*

[8] *SEMI E43: Guide for Measuring Static Charge on Objects and Surfaces.*

Table 91 Crosscut Issues Relating to Factory Integration

Crosscut Area	*Factory integration related key challenges*
Interconnect	1.5 mm wafer edge exclusion may post challenges (need to justify additional die per wafer from 1.5mm); Overall increasing cost of abatement needs to be addressed. New materials impact.
Front end Process (FEP)	1.5 mm wafer edge exclusion is a challenge to starting material and SOI. FEP to communicate special facility AMC requirements.
Litho	Current focus on Immersion and EUVL (power, consumables); Fast reticle change; vibration specs; reticle storage issues; Need to coordinate YE inputs on water quality (temp and pH); AMC relative to the Reticle (reticle storage and in the litho equipment).
ESH	Ergonomics, Tool design, Chemical consumption concerns; AMC and particulate levels to be maintained; Regulations; ESH chemical abatement analysis needed. As per ESH, the trend is point of use versus central. Global warming ◊ Factories and Power suppliers will be asked to limit CO_2 emissions soon.
Metrology	Need for Integrated Metrology continues? Data standards; AMC relative to the Reticle (reticle storage and in the litho equipment).
Yield Enhancement	YE to maintain AMC technical requirements; traceability issues? No wafer coordinate standards exist today. Not having a data standard is inconvenience only. Need Design to Test coordinate system
Assembly & Packaging	Wafer level packaging issues (will be addressed by A&P and they will let FI know if there is any specific FI needs); Chip level (Dice) traceability.

Table 92 List of Next Wafer Size Challenges

Technology WG	*Next wafer size (450mm) challenges*
FI – Factory Operations	Business model: Need to define operations axes: High volume vs. Low volume; High mix vs. Low mix; front end vs. backend (Metal layers), Cu/Al; Logic vs. DRAM, WSPW (small versus large). Transportation lot size versus carrier lot size; More single wafer processes; 2–10 wafer lots; High mix issues; cycle time issues.
FI – Production Equipment	Mix use a certain small capacity mini-environment carrier (Ex: Bottom opening 5–10 wafer carrier); Conveyor transport; Small footprint tool buffering; 300 mm to 450 mm conversion? Equipment platform concept; Wafer gripping and edge exclusion; Alpha tool development?
FI – Factory Information & Control Systems	Factory automation (load lock, transportation method, etc.); Stringent process control needs for high mix small lot production
FI – AMHS	Conveyor transport may be required for 20k to 30k WSPM Fabs running small (5–10 wafer) Lot carriers; Impact on MPH; Transport batch size?
FI – Facilities	Extendibility of current fabs, watch out for increased sub-fab area; abatement point-of-use and new material issues; Height, vibration, floor density
Interconnect	Work with the 450mm teams on interconnect issues. Wafer edge exclusion (1.5 mm?); Cost of abatement due to NWS and new materials.
Front end Process (FEP)	450mm presents unprecedented challenges: Technical: meeting specs over larger areas); Economic: for wafer, equipment, and metrology suppliers; Critical path definition.: already late to meet development cycle; Standardization: Wafer spec (type, thickness, diameter tolerance); FEP will investigate at what generation we may have to switch to single wafer processing; 450mm issues will be highlighted in sub chapter, position paper
Lithography	Current focus on Immersion and EUVL (power, consumables); Fast reticle change; vibration specs; reticle storage issues
ESH	Ergonomics, Tool design, Chemical consumption concerns; AMC and particulate levels to be maintained; Regulations
Metrology	Need for Integrated Metrology continues? Data standards
Yield Enhancement	Wafer size configuration; traceability?
Assembly & Packaging	Wafer package (FOSB, FOUP, door configuration, etc.); traceability?
Other	Work with the 450mm teams on FI challenges. Apply lessons learned from 300 mm transition. We need to learn from LCD manufacturers.