INTERNATIONAL TECHNOLOGY ROADMAP FOR SEMICONDUCTORS

2006 UPDATE
FINAL DRAFT

INTERCONNECT

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INTERCONNECT

SUMMARY

It should be noted that for the 2006 ITRS Interconnect roadmap, the title of the primary technology requirements table has been expanded to include ASICs and is now "MPU and ASIC Interconnect Technology Requirements."

Also for 2006, in recognition of the increasing importance of the dynamic power dissipated in the interconnect structure, a new power metric has been added to the MPU and ASIC Technology Requirements Tables. The power metric is the power (measured in Watts) dissipated per Ghz of frequency and cm^2 of metal layer. The power metric is shown as a range for each of the roadmap years. Although the power metric is seen to plateau for the long-term years due to aggressive introduction of low-κ dielectrics, the power dissipated in the interconnect structure will still increase dramatically due to higher frequencies and increases in the number of metal layers. Note that this metric is a measure of the dynamic power associated with the interconnect structure and the actual power dissipation of a specific MPU or ASIC will be a function of architecture and implementation of power saving design features. This power metric will also serve as a key benchmark so that future interconnect alternatives, such as radio frequency (RF), optical or carbon nanotubes, can be compared to conventional wiring technology.

In addition to the power metric, the capacitance per unit length for Metal 1, intermediate, and minimum global wiring layers has also been added to the tables for 2006. The Cu resistivity of these layers had been added in prior years and with the addition of capacitance, the RC values can easily be calculated.

The metric for Interlevel-metal insulator—bulk dielectric constant (κ) has also been changed for 2006. In prior roadmaps, this metric had been listed as the minimum expected for each year. This metric has been replaced with a range of values depicting both the most aggressive bulk dielectric constant expected as well as a more realistic case. This range of bulk κ values was then used to calculate the metric which lists the range of κ_{eff} values for each of the roadmap years.

One of the grand challenges for interconnect is the result of the rapid introductions of new materials/processes that are necessary to meet conductivity requirements and reduce the dielectric permittivity. These create integration, cost, and reliability challenges.

Another of the grand challenges is the variability associated with line edge roughness, trench and via depth and profile, etch bias, thinning due to cleaning and CMP as well as size effects.

Traditional interconnect scaling will no longer satisfy performance requirements. Defining and finding solutions beyond copper and low κ will require material innovation, combined with accelerated design, packaging and unconventional interconnect.

DIFFICULT CHALLENGES

Table 79 Interconnect Difficult Challenges

Difficult Challenges ≥ 32 nm	*Summary of Issues*
Introduction of new materials to meet conductivity requirements and reduce the dielectric permittivity*	The rapid introductions of new materials/processes that are necessary to meet conductivity requirements and reduce the dielectric permittivity create integration and material characterization challenges.
Engineering manufacturable interconnect structures compatible with new materials and processes*	Integration complexity, CMP damage, resist poisoning, dielectric constant degradation. Lack of interconnect/packaging architecture design optimization tool
Achieving necessary reliability	New materials, structures, and processes create new chip reliability (electrical, thermal, and mechanical) exposure. Detecting, testing, modeling and control of failure mechanisms will be key.
Three-dimensional control of interconnect features (with it's associated metrology) is required to achieve necessary circuit performance and reliability.	Line edge roughness, trench depth and profile, via shape, etch bias, thinning due to cleaning, CMP effects. The multiplicity of levels combined with new materials, reduced feature size, and pattern dependent processes create this challenge.
Manufacturability and defect management that meet overall cost/performance requirements	As feature sizes shrink, interconnect processes must be compatible with device roadmaps and meet manufacturing targets at the specified wafer size. Plasma damage, contamination, thermal budgets, cleaning of high A/R features, defect tolerant processes, elimination/reduction of control wafers are key concerns. Where appropriate, global wiring and packaging concerns will be addressed in an integrated fashion.
Difficult Challenges < 32 nm	*Summary of Issues*
Mitigate impact of size effects in interconnect structures	Line and via sidewall roughness, intersection of porous low-κ voids with sidewall, barrier roughness, and copper surface roughness will all adversely affect electron scattering in copper lines and cause increases in resistivity.
Three-dimensional control of interconnect features (with it's associated metrology) is required	Line edge roughness, trench depth and profile, via shape, etch bias, thinning due to cleaning, CMP effects. The multiplicity of levels, combined with new materials, reduced feature size and pattern dependent processes, use of alternative memories, optical and RF interconnect, continues to challenge.
Patterning, cleaning, and filling at nano dimensions	As features shrink, etching, cleaning, and filling high aspect ratio structures will be challenging, especially for low-κ dual damascene metal structures and DRAM at nano-dimensions.
Integration of new processes and structures, including interconnects for emerging devices	Combinations of materials and processes used to fabricate new structures create integration complexity. The increased number of levels exacerbate thermomechanical effects. Novel/active devices may be incorporated into the interconnect.
Identify solutions which address global wiring scaling issues*	Traditional interconnect scaling will no longer satisfy performance requirements. Defining and finding solutions beyond copper and low κ will require material innovation, combined with accelerated design, packaging and unconventional interconnect.

** Top three challenges*
CMP—chemical mechanical planarization DRAM—dynamic random access memory

TECHNOLOGY REQUIREMENTS

Table 80a MPU and ASIC Interconnect Technology Requirements—Near-term Years UPDATED

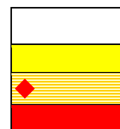
	Year of Production	*2005*	*2006*	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*
	DRAM ½ Pitch (nm) (contacted)	*80*	*70*	*65*	*57*	*50*	*45*	*40*	*36*	*32*
	MPU/ASIC Metal 1 ½ Pitch (nm)(contacted)	*90*	*78*	*68*	*59*	*52*	*45*	*40*	*36*	*32*
	MPU Physical Gate Length (nm)	*32*	*28*	*25*	*22*	*20*	*18*	*16*	*14*	*13*
	Number of metal levels	11	11	11	12	12	12	12	12	13
	Number of optional levels – ground planes/capacitors	4	4	4	4	4	4	4	4	4
	Total interconnect length (m/cm^2) – Metal 1 and five intermediate levels, active wiring only [1]	1019	1212	1439	1712	2000	2222	2500	2857	3125
	FITs/m length/cm^2 × 10^{-3} excluding global levels [2]	4.9	4.1	3.5	2.9	2.5	2.3	2	1.8	1.6
	J_{max} (A/cm^2) – intermediate wire (at 105ºC)	8.91E+05	1.37E+06	2.08E+06	3.08E+06	3.88E+06	5.15E+06	6.18E+06	6.46E+06	8.08E+06
	Metal 1 wiring pitch (nm)	180	156	136	118	104	90	80	72	64
	Metal 1 A/R (for Cu)	1.7	1.7	1.7	1.8	1.8	1.8	1.8	1.8	1.9
	Interconnect RC delay (ps) for a 1 mm Cu Metal 1 wire, assumes no scattering and an effective ρ of 2.2 μΩ-cm	307	409	486	626	783	966	1224	1357	1572
	Interconnect RC delay (ps) for 1 mm Cu Metal 1 wire, assumes width-dependent scattering and a conformal barrier of thickness specified below	440	612	767	1044	1388	1792	2392	2857	3451
	Conductor effective resistivity (μΩ–cm) Cu Metal 1 wiring including effect of width-dependent scattering and a conformal barrier of thickness specified below	3.15	3.29	3.47	3.67	3.9	4.08	4.3	4.63	4.83
ADD	Capacitance per unit length for M1 wires (pF/cm) [6]	2.0-2.2	2.0-2.2	1.8-2.0	1.9-2.1	1.8-2.0	1.8-2.0	1.8-2.0	1.6-1.8	1.6-1.8
	Barrier/cladding thickness (for Cu Metal 1 wiring) (nm) [3]	6.5	5.6	4.8	4.3	3.7	3.3	2.9	2.6	2.4
	Line length (μm) where τ = RC delay (Metal 1 wire) no scattering	53	43	36	29	24	20	17	15	13
	Line length (μm) where 25% of switching voltage is induced on victim Metal 1 wire by crosstalk [4]	136	118	107	96	90	84	79	73	61
	Cu thinning at minimum pitch due to erosion (nm), 10% × height, 50% areal density, 500 μm square array	15	13	12	11	9	8	7	6	6
	Total Metal 1 resistance variability due to CD erosion and scattering (%) [4]	28	29	28	29	30	30	31	32	32
	Intermediate wiring pitch (nm)	200	167	140	118	104	90	80	72	64
	Intermediate wiring dual damascene A/R (Cu wire/via)	1.7/1.5	1.7/1.6	1.8/1.6	1.8/1.6	1.8/1.6	1.8/1.6	1.8/1.6	1.9/1.7	1.9/1.7
	Interconnect RC delay (ps) for a 1 mm Cu intermediate wire, assumes no scattering and an effective ρ of 2.2 μΩ-cm	254	360	437	626	797	984	1246	1334	1596

	Interconnect RC delay (ps) for 1 mm Cu intermediate wire, assumes width-dependent scattering and a conformal barrier of thickness specified below	355	527	682	1039	1413	1825	2436	2784	3504
	Conductor effective resistivity (μΩ–cm) Cu intermediate wiring including effect of width-dependent scattering and a conformal barrier of thickness specified below	3.07	3.22	3.43	3.65	3.9	4.08	4.3	4.59	4.83
ADD	Capacitance per unit length for intermediate wires (pF/cm) [6]	1.9-2.0	1.9-2.0	1.7-1.8	1.7-1.8	1.5-1.7	1.5-1.7	1.5-1.7	1.3-1.5	1.3-1.5
	Barrier/cladding thickness (for Cu intermediate wiring) (nm) [3]	7.3	6	5.2	4.3	3.7	3.3	2.9	2.6	2.4
	Line length (μm) where τ = RC delay (intermediate wire) no scattering	59	45	38	29	24	20	17	15	13
	Line length (μm) where 25% of switching voltage is induced on victim intermediate wire by crosstalk [4]	235	185	165	136	126	116	106	95	80
	Cu thinning at minimum intermediate pitch due to erosion (nm), 10% × height, 50% areal density, 500 μm square array	17	14	13	11	9	8	7	7	6
	Semi-global wire pitch (nm) (ASIC only)	400	334	280	236	208	180	160	144	128
	Minimum global wiring pitch (nm)	300	250	210	177	156	135	120	108	96
	Ratio range (global wiring pitches/intermediate wiring pitch)	1.5–10	1.5–12	1.5–14	1.5–17	1.5–20	1.5–22	1.5–25	1.5–29	1.5–31
	Global wiring dual damascene A/R (Cu wire/via)	2.2/2.0	2.2/2.0	2.3/2.1	2.3/2.1	2.4/2.2	2.4/2.2	2.4/2.2	2.5/2.3	2.5/2.3
	Interconnect RC delay (ps) for a 1 mm minimum pitch Cu global wire, assumes no scattering and an effective ρ of 2.2 μΩ-cm	96	139	168	242	301	371	470	511	611
	Interconnect RC delay (ps) for 1 mm Cu min pitch global wire, assumes width-dependent scattering and a conformal barrier of thickness specified below	111	165	209	316	410	523	687	787	977
	Conductor effective resistivity (μΩ–cm) minimum pitch Cu global wiring including effect of width-dependent scattering and a conformal barrier of thickness specified below	2.53	2.62	2.73	2.87	3	3.1	3.22	3.39	3.52
ADD	Capacitance per unit length for global wires (pF/cm) [6]	2.1-2.3	2.1-2.3	1.8-2.0	1.8-2.0	1.7-1.9	1.7-1.9	1.7-1.9	1.5-1.7	1.5-1.7
	Barrier/cladding thickness (for min. pitch Cu global wiring) (nm) [3]	7.3	6	5.2	4.3	3.7	3.3	2.9	2.6	2.4
	Line length (μm) where τ = RC delay (global wire at minimum pitch – no scattering)	95	73	62	47	39	33	27	24	20
	Line length (μm) where 25% of switching voltage is induced on victim minimum global wire by crosstalk [4]	170	147	137	130	128	124	120	115	97
ADD	Power index (W/GHz-cm2) [5]	1.0-1.1	1.2-1.3	1.3-1.4	1.3-1.4	1.4-1.5	1.5-1.7	1.7-1.9	1.4-1.6	1.5-1.7
	Cu thinning of maximum width global wiring due to dishing and erosion (nm), 10% × height, 80% areal density	220	220	230	230	240	240	240	250	250
	Cu thinning global wiring due to dishing (nm), 100 μm wide feature	24	21	19	17	15	14	13	13	10
	Conductor effective resistivity (μΩ–cm) Cu wiring, assumes no scattering	2.2	2.2	2.2	2.2	2.2	2.2	2.2	2.2	2.2

	Interlevel metal insulator – effective dielectric constant (κ)	3.1–3.4	3.1–3.4	2.7–3.0	2.7–3.0	2.5–2.8	2.5–2.8	2.5–2.8	2.1–2.4	2.1–2.4
WAS	Interlevel metal insulator (minimum expected) – bulk dielectric constant (κ)	≤ 2.7	≤ 2.7	≤ 2.4	≤ 2.4	≤ 2.2	≤ 2.2	≤ 2.2	≤ 2.0	≤ 2.0
IS	Interlevel metal insulator – bulk dielectric constant (κ)	2.6-3.0	2.6-3.0	2.3-2.7	2.3-2.7	2.1-2.4	2.1-2.4	2.1-2.4	1.8-2.1	1.8-2.1

**Refer to Executive Summary Figure 4 for definition of metal 1 pitch*

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known



Notes for Tables 80a and b:
[1] Calculated by assuming that only one of every three minimum pitch wiring tracks for Metal 1 and five intermediate wiring levels are populated. The wiring lengths for each level are then summed to calculate the total interconnect length per square centimeter of active area.
[2] This metric is calculated by assuming that a 5 FIT (failure in ten thousand) reliability budget is apportioned to interconnect for the highest reliability grade MPUs. This number is then divided by the total interconnect length to arrive at the FITs per meter of wiring per one square centimeter of active area.
[3] Calculated for a conformal layer to meet minimum effective conductor resistivity with no scattering.
[4] Crosstalk is a calcumated value. This metric will be managed by IC Design.
[5] Power index = C Vdd2 a (1 GHz) ew (1 cm2)/p; p = pitch; Vdd = supply voltage; ew = wiring efficiency = 1/3; a = activity factor = 0.03. The calculated values are an approximation for the "power per GHz per cm2 of metallization layer". This index scales with the critical parameters that determine the interconnect dynamic power. NOTES: the values provided are an average for M1, Intermediate and Global interconnects. The range of values results from the maximum and minimum effective dielectric constants.
[6] The capaciance range reflects the maximum and minimum effective dielectric constants.

Table 80b MPU and ASIC Interconnect Technology Requirements—Long-term Years UPDATED

	Year of Production	*2014*	*2015*	*2016*	*2017*	*2018*	*2019*	*2020*
	DRAM ½ Pitch (nm) (contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
	MPU/ASIC Metal 1 ½ Pitch (nm)(contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
	MPU Physical Gate Length (nm)	*11*	*10*	*9*	*8*	*7*	*6*	*6*
	Number of metal levels	13	13	13	14	14	14	14
	Number of optional levels – ground planes/capacitors	4	4	4	4	4	4	4
	Total interconnect length (m/cm^2) – Metal 1 and five intermediate levels, active wiring only [1]	3571	4000	4545	5000	5555	6250	7143
	FITs/m length/$cm^2 \times 10^{-3}$ excluding global levels [2]	1.4	1.3	1.1	1	0.9	0.8	0.7
	J_{max} (A/cm^2) – intermediate wire (at 105ºC)	1.06E+07	1.14E+07	1.47E+07	1.54E+07	1.80E+07	2.23E+07	2.74E+07
	Metal 1 wiring pitch (nm)	56	50	44	40	36	32	28
	Metal 1 A/R (for Cu)	1.9	1.9	2	2	2	2	2
	Interconnect RC delay (ps) for a 1 mm Cu Metal 1 wire, assumes no scattering and an effective ρ of 2.2 μΩ-cm	2053	2346	2943	3563	3754	4752	6207
	Interconnect RC delay (ps) for 1 mm Cu Metal 1 wire, assumes width-dependent scattering and a conformal barrier of thickness specified below	4853	5951	8040	10252	11432	15853	23105
	Conductor effective resistivity (μΩ–cm) Cu Metal 1 wiring including effect of width-dependent scattering and a conformal barrier of thickness specified below	5.2	5.58	6.01	6.33	6.7	7.34	8.19
ADD	Capacitance per unit length for M1 wires (pF/cm) [6]	1.6-1.8	1.5-1.7	1.5-1.8	1.5-1.8	1.4-1.6	1.4-1.6	1.4-1.7
	Barrier/cladding thickness (for Cu Metal 1 wiring) (nm) [3]	2.1	1.9	1.7	1.5	1.3	1.2	1.1
	Line length (μm) where τ = RC delay (Metal 1 wire) no scattering	10	9	7	6	5	5	4
	Line length (μm) where 25% of switching voltage is induced on victim Metal 1 wire by crosstalk [4]	52	47	41	36	33	29	24
	Cu thinning at minimum pitch due to erosion (nm), 10% × height, 50% areal density, 500 μm square array	5	5	4	4	4	3	3
	Total Metal 1 resistance variability due to CD erosion and scattering (%) [4]	31	33	32	33	35	33	33
	Intermediate wiring pitch (nm)	56	50	44	40	36	32	28
	Intermediate wiring dual damascene A/R (Cu wire/via)	1.9/1.7	1.9/1.7	2.0/1.8	2.0/1.8	2.0/1.8	2.0/1.8	2.0/1.8
	Interconnect RC delay (ps) for a 1 mm Cu intermediate wire, assumes no scattering and an effective ρ of 2.2 μΩ-cm	2085	2382	2982	3610	3803	4813	6287
	Interconnect RC delay (ps) for 1 mm Cu intermediate wire, assumes width-dependent scattering and a conformal barrier of thickness specified below	4927	6042	8147	10386	11581	16059	23405
	Conductor effective resistivity (μΩ–cm) Cu intermediate wiring including effect of width-dependent scattering and a conformal barrier of thickness specified below	5.2	5.58	6.01	6.33	6.7	7.34	8.19
ADD	Capacitance per unit length for intermediate wires (pF/cm) [6]	1.3-1.5	1.2-1.4	1.2-1.4	1.2-1.4	1.0-1.2	1.0-1.2	1.0-1.2
	Barrier/cladding thickness (for Cu intermediate wiring) (nm) [3]	2.1	1.9	1.7	1.5	1.3	1.2	1.1
	Line length (μm) where τ = RC delay (intermediate wire) no scattering	10	9	7	6	5	5	4

	Line length (µm) where 25% of switching voltage is induced on victim intermediate wire by crosstalk [4]	68	60.5	53	46	43	40	37
	Cu thinning at minimum intermediate pitch due to erosion (nm), 10% × height, 50% areal density, 500 µm square array	6	5	4	4	4	3	3
	Semi-global wire pitch (nm) (ASIC only)	112	100	88	80	72	64	56
	Minimum global wiring pitch (nm)	84	75	66	60	54	48	42
	Ratio range (global wiring pitches/intermediate wiring pitch)	1.5–36	1.5–40	1.5–45	1.5–50	1.5–56	1.5–63	1.5–71
	Global wiring dual damascene A/R (Cu wire/via)	2.5/2.3	2.6/2.4	2.6/2.4	2.6/2.4	2.8/2.5	2.8/2.5	2.8/2.5
	Interconnect RC delay (ps) for a 1 mm minimum pitch Cu global wire, assumes no scattering and an effective ρ of 2.2 µΩ-cm	798	896	1157	1400	1433	1814	2370
	Interconnect RC delay (ps) for 1 mm Cu min pitch global wire, assumes width-dependent scattering and a conformal barrier of thickness specified below	1353	1601	2210	2794	2983	4064	5795
	Conductor effective resistivity (µΩ–cm) minimum pitch Cu global wiring including effect of width-dependent scattering and a conformal barrier of thickness specified below	3.73	3.93	4.2	4.39	4.58	4.93	5.38
ADD	Capacitance per unit length for global wires (pF/cm) [6]	1.5-1.7	1.4-1.6	1.4-1.6	1.4-1.6	1.2-1.4	1.2-1.4	1.2-1.4
	Barrier/cladding thickness (for min. pitch Cu global wiring) (nm) [3]	2.1	1.9	1.7	1.5	1.3	1.2	1.1
	Line length (µm) where τ = RC delay (global wire at minimum pitch – no scattering)	16	14	11	10	9	7	6
	Line length (µm) where 25% of switching voltage is induced on victim minimum global wire by crosstalk [4]	85	79	71	64	61	55	49
ADD	Power index (W/GHz-cm2) [5]	1.7-2.0	1.4-1.6	1.6-1.9	1.3-1.6	1.3-1.5	1.5-1.7	1.7-2.0
	Cu thinning of maximum width global wiring due to dishing and erosion (nm), 10% × height, 80% areal density	250	260	260	260	280	280	280
	Cu thinning global wiring due to dishing (nm), 100 µm wide feature	10	9	8	7	7	6	6
	Conductor effective resistivity (µΩ–cm) Cu wiring, assumes no scattering	2.2	2.2	2.2	2.2	2.2	2.2	2.2
	Interlevel metal insulator – effective dielectric constant (κ)	2.1–2.4	1.9–2.2	1.9–2.2	1.9–2.2	1.6–1.9	1.6–1.9	1.6–1.9
WAS	Interlevel metal insulator (minimum expected) – bulk dielectric constant (κ)	≤ 2.0	≤ 1.8	≤ 1.8	≤ 1.8	≤ 1.6	≤ 1.6	≤ 1.6
IS	Interlevel metal insulator – bulk dielectric constant (κ)	1.8-2.1	1.6-1.9	1.6-1.9	1.6-1.9	1.4-1.7	1.4-1.7	1.4-1.7

**Refer to Executive Summary Figure 4 for definition of metal 1 pitch*

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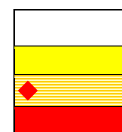

Table 81a DRAM Interconnect Technology Requirements—Near-term Years

Year of Production	*2005*	*2006*	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*
DRAM ½ Pitch (nm) (contacted)	*80*	*70*	*65*	*57*	*50*	*45*	*40*	*36*	*32*
MPU/ASIC Metal 1 ½ Pitch (nm)(contacted)	*90*	*78*	*68*	*59*	*52*	*45*	*40*	*36*	*32*
MPU Physical Gate Length (nm)	*32*	*28*	*25*	*22*	*20*	*18*	*16*	*14*	*13*
Number of metal layers	**4**	**4**	**4**	**4**	**4**	**4**	**4**	**4**	**4**
Contact A/R – stacked capacitor	**15**	**16**	**16**	**17**	**17**	**>20**	**>20**	**>20**	**>20**
Metal 1 wiring pitch (nm) *	**160**	**140**	**130**	**114**	**100**	**90**	**80**	**72**	**64**
Specific contact resistance (Ω-cm^2) for n$^+$ Si	**2.50E-08**	**2.30E-08**	**2.00E-08**	**1.70E-08**	**1.40E-08**	**1.20E-08**	**9.80E-09**	**8.20E-09**	**6.90E-09**
Specific contact resistance (Ω-cm^2) for p$^+$ Si	**4.50E-08**	**3.80E-08**	**3.20E-08**	**2.70E-08**	**2.20E-08**	**1.80E-08**	**1.50E-08**	**1.30E-08**	**1.10E-08**
Specific via resistance (Ω-cm^2)	**7.00E-10**	**6.00E-10**	**5.00E-10**	**4.00E-10**	**3.50E-10**	**2.90E-10**	**2.50E-10**	**2.10E-10**	**1.70E-10**
Conductor effective resistivity ($\mu\Omega$-cm) assumes no scattering for Cu	**3.3**	**3.3**	**2.2**	**2.2**	**2.2**	**2.2**	**2.2**	**2.2**	**2.2**
Interlevel metal insulator – effective dielectric constant (κ)	**3.6–4.1**	**3.6–4.1**	**3.6–4.1**	**3.1–3.4**	**3.1–3.4**	**3.1-3.4**	**2.7–3.0**	**2.7–3.0**	**2.7–3.0**

**Refer to Executive Summary Figure 4 for definition of Metal 1 pitch*

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Interim solutions are known
Manufacturable solutions are NOT known

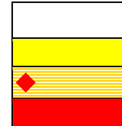


Table 81b DRAM Interconnect Technology Requirements—Long-term Years

Year of Production	*2014*	*2015*	*2016*	*2017*	*2018*	*2019*	*2020*
DRAM ½ Pitch (nm) (contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
MPU/ASIC Metal 1 Half Pitch (nm)(contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
MPU Physical Gate Length (nm)	*11*	*10*	*9*	*8*	*7*	*6*	*6*
Number of metal layers	**4**	**4**	**4**	**4**	**4**	**4**	**4**
Contact A/R – stacked capacitor	**>20**	**>20**	**>20**	**>20**	**>20**	**>20**	**>20**
Metal 1 wiring pitch (nm) *	**56**	**50**	**44**	**40**	**36**	**32**	**28**
Specific contact resistance (Ω-cm^2) for n$^+$ Si	**5.80E-09**	**4.80E-09**	**4.00E-09**	**3.40E-09**	**2.80E-09**	**2.34E-09**	**1.96E-09**
Specific contact resistance (Ω-cm^2) for p$^+$ Si	**9.20E-09**	**7.40E-09**	**6.20E-09**	**5.10E-09**	**4.30E-09**	**3.60E-09**	**3.01E-09**
Specific via resistance (Ω-cm^2)	**1.40E-10**	**1.20E-10**	**1.00E-10**	**8.40E-11**	**7.00E-11**	**5.88E-10**	**4.90E-10**
Conductor effective resistivity ($\mu\Omega$-cm) assumes no scattering for Cu	**2.2**	**2.2**	**2.2**	**2.2**	**2.2**	**2.2**	**2.2**
Interlevel metal insulator – effective dielectric constant (κ)	**2.5–2.8**	**2.5–2.8**	**2.5–2.8**	**2.3–2.6**	**2.3–2.6**	**2.3–2.6**	**2.3–2.6**

**Refer to Executive Summary Figure 4 for definition of Metal 1 pitch*

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known

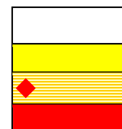
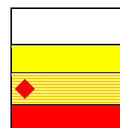


Table 82a Interconnect Surface Preparation Technology Requirements—Near-term Years*

Year of Production	*2005*	*2006*	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*	*Driver*
DRAM ½ Pitch (nm) (contacted)	*80*	*70*	*65*	*57*	*50*	*45*	*40*	*36*	*32*	*D ½*
MPU/ASIC Metal 1 ½ Pitch (nm)(contacted)	*90*	*78*	*68*	*59*	*52*	*45*	*40*	*36*	*32*	*M*
MPU Physical Gate Length (nm)	*32*	*28*	*25*	*22*	*20*	*18*	*16*	*14*	*13*	*M*
Wafer diameter (mm)	**300**	**300**	**300**	**300**	**300**	**300**	**300**	**300**	**300**	*D ½, M*
Wafer edge exclusion (mm)	**2**	**2**	**2**	**2**	**2**	**2**	**2**	**2**	**2**	*D ½, M*
Front surface particles										
Killer defect density, D_pR_p (#/cm^2) [A]	**0.028**	**0.019**	**0.023**	**0.016**	**0.02**	**0.025**	**0.016**	**0.02**	**0.025**	
Critical particle diameter, d_c (nm) [B]	**40**	**35**	**32.5**	**28.5**	**25**	**22.5**	**20**	**17.5**	**16**	
Critical particle density, D_{pw} (#/wafer) [C]	**97**	**64**	**80**	**54**	**68**	**86**	**123.3**	**155**	**195**	
Back surface particles										
Back surface critical particle diameter (nm) [D]	**0.2**	**0.16**	**0.16**	**0.16**	**0.14**	**0.14**	**0.14**	**0.14**	**NA**	
Back surface critical particle density (#/wafer) [E]	**400**	**400**	**200**	**200**	**200**	**200**	**200**	**200**	**NA**	
Edge bevel particles										
Edge bevel critical particle diameter (nm) [F]	**160**	**140**	**130**	**114**	**100**	**90**	**80**	**70**	**64**	
Particles (cm^{-2}) (G)	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	*M*
Particles (#/wafer) (G)	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	*M*
Metallic Contamination										
Critical front surface metals (10^9 atoms/cm^2) (H)	**10**	**10**	**10**	**10**	**10**	**10**	**10**	**10**	**10**	
Critical back surface metals (Cu) (10^9 atoms/cm^2) (I)	**1000**	**1000**	**500**	**500**	**500**	**250**	**250**	**250**	**100**	
Mobile ions (10^{10} atoms/cm^2) [J]	**5**	**5**	**2.5**	**2.5**	**2.5**	**2.5**	**2.5**	**2.5**	**2.4**	
Organic contamination (10^{13} C atoms/cm^2) [K]	**1.4**	**1.3**	**1.2**	**1**	**0.9**	**0.9**	**0.9**	**0.9**	**0.9**	
Cleaning Effects on Dielectric Material										
Maximum dielectric constant increase due to Etch, Strip + Clean [L]	**2.50%**	**2.50%**	**2.50%**	**2.50%**	**2.50%**	**2.00%**	**2.00%**	**2.00%**	**2.00%**	
Maximum dielectric constant increase due to rework [L]	**2.50%**	**2.50%**	**2.50%**	**2.50%**	**2.50%**	**2.00%**	**2.00%**	**2.00%**	**2.00%**	
Maximum effect on dielectric critical dimension due to Strip + Clean [M]	**2.50%**	**2.50%**	**2.50%**	**2.50%**	**2.50%**	**2.50%**	**2.50%**	**2.50%**	**2.50%**	



Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known

Notes for Tables 82a and b:

*[A] Killer defect density is calculated from the formula for 99% yield, Y=0.99=exp[-DpRpAeff]. Aeff is the effective chip area, Dp is the defect density, and Rp is a defect kill factor indicating the probability that a given defect will kill the device. The product DpRp is the density of device-killing defects on the wafer. Rp is dependent on numerous things including the size and shape of the particle, the composition of the particle, and specifics of the device layout. In previous years, Rp was assumed to be 0.2 for any particle > the critical particle size, dc. Aeff is assumed to be the same as for Front End Surface Preparation. For DRAM, Aeff=2.5F2T+(1-aF2T/Achip)*0.6Achip. where F is the minimum feature size, a is the cell fill factor, T is the number of DRAM bits (transistors) per chip, and Achip is the DRAM chip size. For MPUs, Aeff=aT(GL)2, where GL is the gate length. Because Aeff can increase or decrease with each successive technology generation, DpRp does not always decrease over time.*

[B] Critical particle diameter, dc, is defined by Yield Enhancement as ½ of the metal ½-pitch dimension. This should be considered an "effective" particle diameter as most particulate contamination is irregular in shape.

*[C] An example is provided which assumes that the kill factor, Rp, is 0.2 for all particles larger than the critical particle size. This is the assumption made in previous versions of the roadmap, but is not universally valid and is included only for purposes of an example calculation. Particles/wafer is calculated using [Rp*3.14159*(wafer radius-edge exclusion)2]. To convert from particles/wafer at the critical particle size to particles/wafer at an alternative size, a suggested conversion formula is: Dalternate=Dcritical*(dcritical/ dalternate)2.*

[D] & [E] Metrics for Backside particle critical diameter and count have been taken from the requirements from table from the FEOL surface preparation document.

[F] & [G] Edge bevel critical particle size is taken as 2 DRAM ½ Pitch. The size was determined to be particles that could be shed and then distributed onto the wafer surface causing detrimental yield reduction. Few references exist correlating edge defects with yield, however, minimization of the particle size and density is important. The levels are still under evaluation, however, and no values are presented here, although current practices indicate edge bevel particle adders for any interconnect process step, in particular CMP, should be less than 4 defects per quadrant of the wafer. Again, this value should be treated as guidance, not a specification.*

[H] Front surface metallic contamination levels are based on degradation of yield from metallic diffusion into the transistor or leakage of the device from metal migration. Data shows that Cu levels <1E13 can cause interconnect leakage and <1E10 can cause transistor degradation. The ability of the Cu to diffuse into the dielectric and then through the silicon to the transistors is questionable as many references site the fact that Cu cannot diffuse though thick silicon, nevertheless, the lower the Cu contamination the better. The levels are still under evaluation, however, and the values presented here should be treated as guidance, not a specification.

[I] Back surface Cu contamination levels are based on degradation of electrical parameters of the transistor caused by Cu diffusion through the silicon. Many studies have been undertaken that evaluate the effects of backside Cu contamination on the transistors. The most profound affect is TDDB due to electric field drift. Oxygen on the back surface prevents the diffusion into the silicon. However, once in the silicon the Cu will diffuse and precipitate, dependent on thermal treatments. Various references quote a concentration as high as 1E15 and others quote as low as 1E11 as degrading device performance, dependent on test device structures and film thicknesses. Again, the levels are still under evaluation and the values presented here should be treated as guidance, not a specification. Reference: A. A. Isrtatov and E. R. Weber, J. Electrochem. Soc. 149(1) G21(2002).

[J] Mobile ions for interconnect are less stringent than the front end line metrics. Although the mobile ions can lead to the same electrical degradation and do the same damage from migration through the dielectric, the oxide does getter some of the sodium. For backside contamination levels, use the front end values. For interconnect, the causes shown here are guidance as to allowable levels, approximately twice the value of the front end metrics.

[K] Organic contamination is usually in the form of a thin layer of hydrocarbon remaining on the wafer after resist strip and clean and after post-CMP clean. Leaving this film may result in undesirable delamination of subsequently deposited layers or "carbon spots" caused by a monolayer or more of BTA (benzotriazole)-copper complex. A monolayer, about 1 nm of BTA on copper yields a carbon atom density of about 4E14 atoms/cm2. Carbon residues may also come from inadequately stripped resist or shedding of particles from process chambers. The same metric is used for interconnect as the front end, Dc at the 180 nm corresponded to 10% carbon atom coverage of a bare silicon wafer (7.3E+13atoms/cm^2). Dc for subsequent generations was scaled linearly with the ratio of CD to 180 nm. Dc = (CD/180)(7.3E+13).

[L] Etching, stripping and cleaning processes are known to have a detrimental effect on the dielectric constant of insulating layers. This is especially true for porous dielectric materials. It is essential to minimize and eventually eliminate this effect. Rework of photolithographic patterning involves stripping and cleaning and can have similar effects on the dielectric constant. These values are guidance for allowable degradation of the dielectric constant. Changes to the dielectric constant need to be measured (at a minimum) by interdigitated trench test structures, as measurements on planar films through MIS capacitor measurements are generally not representative of integrated structures. One common approach is to compare measured RC products with those from computer simulations assuming bulk dielectric constant values. The difference between the measurement from the simulation can be representative of the etch/strip/clean damage. The color change from Yellow to Red in 2012 reflects the dielectric change to a κ-value of < 2.1.

[M] Current etch and strip methods can damage porous low-κ films through the removal of carbon species; however, the extent of this damage may not be fully determined until after subsequent wet cleans. The CD loss after etch and strip may be negligible, but, following wet clean, the CD loss may become significant. Because the clean can remove film thicknesses rendered vulnerable by the etch, the extent of CD loss after wet cleans can be the result of both the etch and cleans processes. While not explicit in measurable CD loss, bowing of the trench and via structures should be minimized to allow conformal liners and plating base deposition and to reduce copper voiding effects. The color change from Yellow to Red in 2012 reflects the dielectric change to a k-value of < 2.1.

Table 82b Interconnect Surface Preparation Technology Requirements—Long-term Years

Year of Production	*2014*	*2015*	*2016*	*2017*	*2018*	*2019*	*2020*	*Driver*
DRAM ½ Pitch (nm) (contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*	*D ½*
MPU/ASIC Metal 1 ½ Pitch (nm)(contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*	*M*
MPU Physical Gate Length (nm)	*11*	*10*	*9*	*8*	*7*	*6*	*6*	*M*
Wafer diameter (mm)	**450**	**450**	**450**	**450**	**450**			*D ½, M*
Wafer edge exclusion (mm)	**2**	**2**	**2**	**2**	**2**			*D ½, M*
Front surface particles								
Killer defect density, D_pR_p (#/cm^2) [A]	**0.016**	**0.02**	**0.014**	**0.017**	**0.022**			
Critical particle diameter, d_c (nm) [B]	**14**	**12.5**	**11**	**10**	**9**			
Critical particle density, D_{pw} (#/wafer) [C]	**123.1**	**155**	**106**	**133.4**	**168**			
Back surface particles								
Back surface critical particle diameter (nm) [D]	**NA**	**NA**	**NA**	**NA**	**NA**			
Back surface critical particle density (#/wafer) [E]	**NA**	**NA**	**NA**	**NA**				
Edge bevel particles								
Edge bevel critical particle diameter (nm) [F]	**56**	**50**	**44**	**40**	**36**			
Particles (cm^{-2}) (G)	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**			*M*
Particles (#/wafer) (G)	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**			*M*
Metallic Contamination								
Critical front surface metals (10^9 atoms/cm^2) (H)	**10**	**10**	**10**	**10**	**10**			
Critical back surface metals (Cu) (10^9 atoms/cm^2) (I)	**100**	**100**	**100**	**100**	**100**			
Mobile ions (10^{10} atoms/cm^2) [J]	**2.4**	**2.4**	**2.3**	**2.3**	**2.3**			
Organic contamination (10^{13} C atoms/cm^2) [K]	**0.9**	**0.9**	**0.9**	**0.9**	**0.9**			
Cleaning Effects on Dielectric Material								
Maximum dielectric constant increase due to Etch, Strip + Clean [L]	**2.00%**	**2.00%**	**2.00%**	**2.00%**	**2.00%**			
Maximum dielectric constant increase due to rework [L]	**2.00%**	**2.00%**	**2.00%**	**2.00%**	**2.00%**			
Maximum effect on dielectric critical dimension due to Strip + Clean [M]	**2.50%**	**2.50%**	**2.50%**	**2.50%**	**2.50%**			

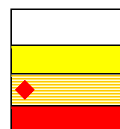


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Table 83 Options for Global Interconnects Beyond the Metal/Dielectric System

Options
Use Different Signaling Methods – Signal design – Signal coding techniques
Use innovative design and package options – Interconnect-centric design – Package intermediated interconnect – Chip-package co-design
Use Geometry – 3D
Use Different Physics – Optics (emitters, detectors, free space, waveguides) – RF/microwaves (transmitters, receivers, free space, waveguides) – Terahertz photonics
Radical Solutions – Nanowires/nanotubes – Molecules – Spin – Quantum wave functions

Table A1 Assumption on Interconnect Parameter Estimation Model

	Assumption on Interconnect Parameter Estimation
Design Rule	× 0.70/scaling, reverse scaling for GM
Chip Size	=7 mm^2 as 1-clock cycle limit
Module Size	× 0.70/scaling
Repeater	Inserted for long IM and GM wires
Gate Density	× 2.0/generation (based on ITRS 2002 MPU roadmap)
Active Power Density	× 0.6/generation with average-long IM wire
Logic Depth	× 0.75/scaling
T min.	× 0.70/scaling