INTERNATIONAL
TECHNOLOGY ROADMAP
FOR
SEMICONDUCTORS

2006 UPDATE
FINAL DRAFT

RADIO FREQUENCY AND ANALOG/MIXED-SIGNAL TECHNOLOGIES FOR WIRELESS COMMUNICATIONS

RADIO FREQUENCY AND ANALOG/MIXED-SIGNAL TECHNOLOGIES FOR WIRELESS COMMUNICATIONS

SUMMARY—STATE OF WIRELESS TECHNOLOGIES 2006 - ITRS PERSPECTIVE

Radio frequency (RF) and analog mixed-signal technologies serve the rapidly growing wireless communications market and represent essential and critical technologies for the success of many semiconductor manufacturers. Communications products may replace computers as a key driver of volume manufacturing. Consumer products now account for over half of the demand for semiconductors.[1] For example, third generation (3G) cellular phones now have a much higher semiconductor content and now are 50 % of the cellular phone market compared to only 5 % of the market a few years ago. The consumer portions of wireless communications markets are very sensitive to cost. With different technologies capable of meeting technical requirements, time to market and overall system cost will govern technology selection.

The boundary between silicon-based and III-V semiconductors continues to move to higher frequencies with time. Frequency will be less important for defining the boundaries among technologies and other parameters such as noise figure, output power, power-added efficiency, linearity and ultimately cost will become more important. This shift in importance from frequency to parameters such as those listed in the previous sentence is already occurring for power amplifiers.

For CMOS, the long term prediction of device RF and noise performance becomes more uncertain with the introduction of metal gate electrodes (2009), high permittivity (high-κ) gate dielectrics (2009), and new device structures such as fully depleted and/or double-gated silicon-on-insulator (SOI) (2015). The trend of higher integration and performance levels for logic with mixed-signal circuitry leads to steadily increasing digital processing capabilities that enable more signal treatments to be done in the digital domain.

For bipolar, the key driving forces include speed, power consumption, noise, and breakdown.

For passive devices, the biggest challenges are integrating them into a digital CMOS process and the trade-off between processing cost and device performance.

For power amplifiers—mobile, the nearly fixed battery voltages and ruggedness requirements tend to slow technology evolution. Highly integrated modules with multi-layer laminates are dramatically reducing total RF front end area.

For power amplifiers—basestation, the device cost is projected to steadily decrease from about $0.70/Watt today to less than $0.50/Watt by 2008 and the applications space is moving from 2 GHz and below to higher frequencies, such as worldwide interoperability for microwave access (WiMAX) at 3.5 GHz and from saturated power amplifiers to more linear amplifiers to support code division multiple access (CDMA) and wideband CDMA (WCDMA).

For millimeter wave applications, InP-based RF transistors have demonstrated very high frequencies and GaN transistors have demonstrated record power densities at 40 GHz of 10W/mm with 40 Volts drain bias. GaN is advancing much more quickly than predicted in 2003 and 2004.

Future wireless challenges include signal isolation and the software defined radio (SDR). A signal isolation roadmap with quantitative technical requirements is very difficulty because agreement on which figures of merit and measurements to use does not exist. The SDR presents many issues such as the analog-to-digital (ADC) performance, transmitter solutions, and cost.

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[1] *P. H. Singer, "Dramatic Gains in Performance on the Horizon," editorial in* Semiconductor International*, Vol. 29, No. 8, 29, July 2006, page 15.*

2006 UPDATE TECHNOLOGY REQUIREMENTS TABLES

Table 46a RF and Analog Mixed-Signal CMOS Technology Requirements—Near-term Years

Year of Production	*2005*	*2006*	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*
DRAM ½ Pitch (nm) (contacted)	*80*	*70*	*65*	*57*	*50*	*45*	*40*	*35*	*32*
Performance RF/Analog [1]									
Supply voltage (V) [2]	**1.2**	**1.2**	**1.2**	**1.2**	**1.1**	**1.1**	**1.1**	**1**	**1**
T_{ox} (nm) [2]	**2.2**	**2.1**	**2.0**	**1.9**	**1.6**	**1.5**	**1.4**	**1.4**	**1.3**
Gate Length (nm) [2]	**75**	**65**	**53**	**45**	**37**	**32**	**28**	**25**	**22**
g_m/g_{ds} at $5 \cdot L_{min\text{-}digital}$ [3]	**47**	**40**	**32**	**30**	**30**	**30**	**30**	**30**	**30**
1/f-noise ($\mu V^2 \cdot \mu m^2/Hz$) [4]	**190**	**180**	**160**	**140**	**100**	**90**	**80**	**80**	**70**
σ V_{th} matching ($mV \cdot \mu m$) [5]	**6**	**6**	**6**	**6**	**5**	**5**	**5**	**5**	**5**
I_{ds} ($\mu A/\mu m$) [6]	**19**	**15**	**13**	**11**	**9**	**8**	**7**	**6**	**6**
Peak F_t (GHz) [7]	**120**	**140**	**170**	**200**	**240**	**280**	**320**	**360**	**400**
Peak F_{max} (GHz) [8]	**200**	**220**	**270**	**310**	**370**	**420**	**480**	**530**	**590**
NF_{min} (dB) [9]	**0.33**	**0.3**	**0.25**	**0.22**	**0.2**	**<0.2**	**<0.2**	**<0.2**	**<0.2**
Precision Analog/RF Driver [1]									
Supply voltage (V)	**2.5**	**2.5**	**2.5**	**2.5**	**2.5**	**1.8**	**1.8**	**1.8**	**1.8**
T_{ox} (nm) [10]	**5**	**5**	**5**	**5**	**5**	**3**	**3**	**3**	**3**
Gate Length (nm) [10]	**250**	**250**	**250**	**250**	**250**	**180**	**180**	**180**	**180**
g_m/g_{ds} at $10 \cdot L_{min\text{-}digital}$ [11]	**220**	**220**	**220**	**220**	**220**	**160**	**160**	**160**	**160**
1/f Noise ($\mu V^2 \cdot \mu m^2/Hz$) [4]	**500**	**500**	**500**	**500**	**500**	**180**	**180**	**180**	**180**
σ V_{th} matching ($mV \cdot \mu m$) [5]	**9**	**9**	**9**	**9**	**9**	**6**	**6**	**6**	**6**
Peak F_t (GHz) [7]	**40**	**40**	**40**	**40**	**40**	**50**	**50**	**50**	**50**
Peak F_{max} (GHz) [8]	**70**	**70**	**70**	**70**	**70**	**90**	**90**	**90**	**90**

Manufacturable solutions exist, and are being optimized	⬜
Manufacturable solutions are known	🟨
Interim solutions are known	◆
Manufacturable solutions are NOT known	🟥

Table 46b RF and Analog Mixed-Signal CMOS Technology Requirements—Long-term Years

Year of Production	*2014*	*2015*	*2016*	*2017*	*2018*	*2019*	*2020*
DRAM ½ Pitch (nm) (contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
Performance RF/Analog [1]							
Supply voltage (V) [2]	**1**	**1**	**1**	**1**	**1**	**1**	**1**
T_{ox} (nm) [2]	**1.2**	**1.1**	**1.1**	**1.1**	**1**	**1**	**0.9**
Gate Length (nm) [2]	**20**	**18**	**16**	**14**	**13**	**12**	**11**
g_m/g_{ds} at $5 \cdot L_{min\text{-}digital}$ [3]	**30**	**30**	**30**	**30**	**30**	**30**	**30**
1/f-noise ($\mu V^2 \cdot \mu m^2$/Hz) [4]	**60**	**50**	**50**	**50**	**40**	**40**	**30**
σ V_{th} matching (mV·µm) [5]	**5**	**5**	**4**	**4**	**4**	**4**	**3**
I_{ds} (µA/µm) [6]	**5**	**4**	**4**	**3**	**3**	**3**	**2**
Peak F_t (GHz) [7]	**440**	**490**	**550**	**630**	**670**	**730**	**790**
Peak F_{max} (GHz) [8]	**650**	**710**	**790**	**890**	**950**	**1020**	**1110**
NF_{min} (dB) [9]	**<0.2**	**<0.2**	**<0.2**	**<0.2**	**<0.2**	**<0.2**	**<0.2**
Precision Analog/RF Driver [1]							
Supply voltage (V)	**1.8**	**1.8**	**1.8**	**1.8**	**1.8**	**1.5**	**1.5**
T_{ox} (nm) [10]	**3**	**3**	**3**	**3**	**3**	**2.6**	**2.6**
Gate Length (nm) [10]	**180**	**180**	**180**	**180**	**180**	**130**	**130**
g_m/g_{ds} at $10 \cdot L_{min\text{-}digital}$ [11]	**160**	**160**	**160**	**160**	**160**	**110**	**110**
1/f Noise ($\mu V^2 \cdot \mu m^2$/Hz) [4]	**180**	**180**	**180**	**180**	**180**	**135**	**135**
σ V_{th} matching (mV·µm) [5]	**6**	**6**	**6**	**6**	**6**	**5**	**5**
Peak F_t (GHz) [7]	**50**	**50**	**50**	**50**	**50**	**70**	**70**
Peak F_{max} (GHz) [8]	**90**	**90**	**90**	**90**	**90**	**120**	**120**
		switch to FD ro DG device					

Manufacturable solutions exist, and are being optimized	⬜
Manufacturable solutions are known	🟨
Interim solutions are known	◆
Manufacturable solutions are NOT known	🟥

Notes for Table 46:

[1] Year of first digital product for a given technology generation as presented in overall roadmap technology characteristics (ORTC) tables. Lithographic drivers for key technologies are indicated. Year of first RF and mixed-signal product at the same technology lag the low-standby power roadmap by one year. Beyond Planar CMOS, performance RF/Analog CMOS reflect DG CMOS, Precision Analog/RF driver device color change to yellow reflecting uncertainty on device integration. The supply voltage, T_{ox}, gate length and I_{ds}, F_t, F_{max} color codes reflected the low-standby power roadmap. The logic low standby power is the driver for this. Refer to the LSTP tables in the PIDS chapter for the latest information.

[2] Nominal supply voltage, V_{dd}, SiO_2 equivalent physical CMOS gate dielectric thickness, T_{ox}, and minimum nominal gate length from low-standby power digital roadmap.

[3] Measure for the low frequency amplification of a 5× minimum length, low-standby power CMOS transistor. Using different lengths is an extra degree of freedom in mixed signal designs. Long devices have better G_{ds} amplification (at low frequencies). Operation point taken at 200 mV above the threshold voltage, V_{th}, and at $V_{ds} = V_{dd}/2$. The minimum value of 30 exceeds the projected technology capability with continued scaling for the standard logic device. When this occurs, the standard logic device should be replaced with a unique device designed for specifically f or superior gain.

[4] 1/f noise spectral density, at a frequency of 1 Hz, normalized to an active emitter area of 1 μm^2.

[5] Matching specification for the NMOS transistor's threshold voltage, assuming "near neighbor" devices at minimum practical separation. Careful layout and photolithographic uniformity, e.g. by using dummy structures, are required. Statistical dopant fluctuations start limiting further improvement with SiO_2. Matching behavior of high-κ gate dielectrics very may be problematic. This parameter determines the lower boundary for the size of transistor in a mixed-signal circuit for a given accuracy and will limit dimensional, performance, and DC power consumption.

[6] I_{ds} for F_t of 50 GHz for a minimum transistor length. F_t of 50 GHz is chosen for being 10× the application frequency for 5 GHz. An application frequency of 5 GHz is chosen as a mid-point for the frequency range of interest (1–10 GHz).

[7] Extrapolated from 40 GHz with a 20 dB/dec slope.

[8] Peak F_{max} (measured from unilateral gain extrapolated from 40 GHz with a 20 dB/dec slope).

[9] This is the minimum transistor noise figure at 5 GHz.

[10] This device is required to achieve direct modulation of the PA for applications from 2 to 5 GHz and to support precision analog applications. With continued scaling of logic devices alternate device structures may be required to support the required specifications.

[11] Measure for the low frequency amplification of a 10× minimum length, low-standby power CMOS transistor. Using different lengths is an extra degree of freedom in mixed signal designs. Long devices have better G_{ds} amplification (at low frequencies). Operation point taken at 200 mV above the threshold voltage, V_{th}, and at $V_{ds} = V_{dd}/2$.

Table 47a 0.8 GHz–10 GHz RF and Analog Mixed-Signal Bipolar Technology Requirements—Near-term Years UPDATED

	Year of Production	*2005*	*2006*	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*
	DRAM ½ Pitch (nm) (contacted)	*80*	*70*	*65*	*57*	*50*	*45*	*40*	*36*	*32*
	General Analog NPN Parameters									
	Emitter width (um)	**0.15**	**0.14**	**0.13**	**0.12**	**0.1**	**0.1**	**0.1**	**0.09**	**0.09**
	1/f-noise ($\mu V^2 \cdot \mu m^2$/Hz)	**3**	**3**	**2**	**2**	**2**	**1.5**	**1.5**	**1.5**	**1**
	σ current matching (%·μm)	**2**	**2**	**2**	**2**	**2**	**2**	**2**	**2**	**2**
	High Speed NPN (should be common to mmWave)									
	Peak F_t (GHz) [V_{bc}=1V]	**200**	**230**	**265**	**300**	**350**	**370**	**385**	**400**	**420**
	Peak F_{max} (GHz)	**240**	**260**	**300**	**330**	**390**	**410**	**425**	**440**	**460**
	BV_{ceo}	**2**	**1.9**	**1.8**	**1.7**	**1.7**	**1.7**	**1.7**	**1.6**	**1.6**
Was	J_c at Peak F_t (mA/μm^2)	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**
Is	J_c at Peak F_t (mA/μm^2)	**10**	**12**	**14**	**17**	**20**	**21**	**22**	**23**	**25**
	RF NPN									
	Peak F_t (GHz) [V_{bc}=1V]	**80**	**80**	**90**	**90**	**100**	**100**	**110**	**110**	**120**
	Peak F_{max} (GHz)	**150**	**160**	**170**	**180**	**190**	**200**	**210**	**220**	**230**
	BV_{ceo}	**3.3**	**3.3**	**3.1**	**3.1**	**2.9**	**2.9**	**2.8**	**2.8**	**2.6**
	NF_{min} (dB) at 5GHz	**0.3**	**0.28**	**0.26**	**0.24**	**0.2**	**<0.2**	**<0.2**	**<0.2**	**<0.2**
	I_c (μA/μm) at 50GHz F_t	**43**	**37**	**28**	**22**	**16**	**15**	**14**	**13**	**12**
	High Voltage NPN (Should be common to PA)									
	Peak F_t (GHz) [V_{bc}=1V]	**30**	**32**	**34**	**36**	**38**	**40**	**42**	**44**	**46**
	Peak F_{max} (GHz)	**100**	**110**	**120**	**130**	**140**	**150**	**160**	**170**	**180**
	BV_{ceo}	**8.5**	**8.5**	**8.5**	**8.5**	**8.5**	**8.5**	**8.5**	**8.5**	**8.5**
	BV_{cbo} (V)	**18**	**18**	**18**	**18**	**16**	**16**	**16**	**16**	**16**

Table 47b 0.8 GHz–10 GHz RF and Analog Mixed-Signal Bipolar Technology Requirements—Long-term Years UPDATED

	Year of Production	*2014*	*2015*	*2016*	*2017*	*2018*	*2019*	*2020*
	DRAM ½ Pitch (nm) (contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
	General Analog NPN Parameters							
	Emitter width (um)	**0.09**	**0.08**	**0.08**	**0.08**	**0.07**	**0.07**	**0.07**
	1/f-noise (μV^2·μm^2/Hz)	**1**	**1**	**0.7**	**0.7**	**0.7**	**0.7**	**0.7**
	σ current matching (%·μm)	**2**	**2**	**2**	**2**	**2**	**2**	**2**
	High Speed NPN (should be common to mmWave)							
	Peak F$_t$ (GHz) [V$_{bc}$=1V]	**440**	**460**	**480**	**500**	**530**	**550**	**570**
	Peak F$_{max}$ (GHz)	**480**	**500**	**520**	**540**	**570**	**590**	**610**
	BV$_{ceo}$	**1.5**	**1.5**	**1.4**	**1.4**	**1.3**	**1.3**	**1.3**
Was	J$_c$ at Peak F$_t$ (mA/μm^2)	**19**	**20**	**21**	**22**	**23**	**24**	**25**
Is	J$_c$ at Peak F$_t$ (mA/μm^2)	**26**	**27**	**29**	**30**	**32**	**33**	**35**
	RF NPN							
	Peak F$_t$ (GHz) [V$_{bc}$=1V]	**120**	**130**	**130**	**140**	**140**	**150**	**150**
	Peak F$_{max}$ (GHz)	**240**	**250**	**260**	**270**	**280**	**290**	**300**
	BV$_{ceo}$	**2.6**	**2.5**	**2.5**	**2.4**	**2.4**	**2.4**	**2.4**
	NF$_{min}$ (dB) at 5GHz	**<0.2**	**<0.2**	**<0.2**	**<0.2**	**<0.2**	**<0.2**	**<0.2**
	I$_c$ (μA/μm) at 50GHz F$_t$	**11**	**10**	**9**	**8**	**7**	**6**	**5**
	High Voltage NPN (Should be common to PA)							
	Peak F$_t$ (GHz) [V$_{bc}$=1V]	**48**	**50**	**52**	**54**	**56**	**58**	**60**
	Peak F$_{max}$ (GHz)	**190**	**200**	**210**	**220**	**230**	**240**	**250**
	BV$_{ceo}$	**8.5**	**8.5**	**8.5**	**8.5**	**8.5**	**8.5**	**8.5**
	BV$_{cbo}$ (V)	**16**	**16**	**16**	**16**	**16**	**16**	**16**

Manufacturable solutions exist, and are being optimized	⬜
Manufacturable solutions are known	🟨
Interim solutions are known	◆
Manufacturable solutions are NOT known	🟥

Table 48a Passives Technology Requirements—Near-term Years

Year of Production	*2005*	*2006*	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*
DRAM ½ Pitch (nm) (contacted)	*80*	*70*	*65*	*57*	*50*	*45*	*40*	*36*	*32*
ANALOG									
MOS Capacitor									
Density (fF/μm^2) [1]	7	7	7	7	7	11	11	11	11
Leakage (A/cm^2)	<1e-9	<1e-9	<1e-9	<1e-9	<1e-9	<2e-6	<2e-6	<2e-6	<2e-6
Resistor									
Thin Film BEOL									
Parasitic capacitance (fF/μm^2)	0.03	0.03	0.03	0.03	0.05	0.05	0.05	0.05	0.08
Temp. linearity (ppm/°C)	<100	<100	<100	<100	40-80	40-80	40-80	40-80	30
1σ Matching (% μm)	0.2	0.2	0.2	0.2	0.15	0.15	0.15	0.15	0.1
Sheet resistance, Rs (Ohm/sq)	50	50	50	50	50	50	50	50	50
P+ Polysilicon									
Parasitic capacitance (fF/μm^2)	0.1	0.1	0.1	0.1	0.1	0.1	0.1	0.1	0.1
Temp. linearity (ppm/°C)	<100	<100	<100	<100	40-80	40-80	40-80	40-80	30
1σ Matching (% μm)	1.7	1.7	1.7	1.7	1.7	1.7	1.7	1.7	1
Sheet resistance, Rs (Ohm/sq)	200–300	200–300	200–300	200–300	200–300	200–300	200–300	200–300	200–300
RF									
Metal-Insulator-Metal Capacitor									
Density (fF/μm^2) [2]	2	2	2	4	4	5	5	5	7
Voltage linearity (ppm/V^2)	<100	<100	<100	<100	<100	< 100	< 100	< 100	< 100
Leakage (A/cm^2)	<1e-8	<1e-8	<1e-8	<1e-8	<1e-8	<1e-8	<1e-8	<1e-8	<1e-8
σ Matching (%·μm)	0.7	0.7	0.5	0.5	0.5	0.4	0.4	0.4	0.3
Q (5 GHz for 1pF)	>50	>50	>50	>50	>50	>50	>50	>50	>50
Inductor									
Q (5 GHz, 1nH) [3]	25	27	29	30	32	34	36	38	40
MOS Varactor									
Tuning Range [4]	5.5	5.5	5.5	5.5	5.5	5.5	5.5	5.5	5.5
Q (5 GHz, 0 V)	30	30	35	35	40	40	45	45	50
PA									
PA III-V Passives									
Inductors Q (1GHz, 5nH) [5]	15	25	25	25	25	25	25	30	30
Capacitor Q [6]	>100	>100	>100	>100	>100	>100	>100	>100	>100
RF capacitor density (fF/μm^2) [7]	0.6	2	2	2	2	2	2	2	2
PA Silicon/SiGe Passives [Table 49 a&b]									
Inductors Q (1GHz, 5nH) [5]	10	14	14	14	14	14	14	18	18
Capacitor Q [6]	>100	>100	>100	>100	>100	>100	>100	>100	>100
RF capacitor density (fF/μm^2) [7]	2	2	2	4	4	5	5	5	7

Table 48b Passives Technology Requirements—Long-term Years

Year of Production	*2014*	*2015*	*2016*	*2017*	*2018*	*2019*	*2020*
DRAM ½ Pitch (nm) (contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
ANALOG							
MOS Capacitor							
Density (fF/µm^2) [1]	11	11	11	11	11	13	13
Leakage (A/cm^2) [8]	<2e-6	<2e-6	<2e-6	<2e-6	<2e-6	<2e-5	<2e-5
Resistor							
Thin Film BEOL							
Parasitic capacitance (fF/µm^2)	0.08	0.08	0.08	0.08	0.08	0.08	0.08
Temp. linearity (ppm/°C)	30	30	30	30	30	30	30
1σ Matching (% µm)	0.1	0.1	0.1	0.1	0.1	0.1	0.1
Sheet resistance, Rs (Ohm/sq)	50	50	50	50	50	50	50
P+ Polysilicon							
Parasitic capacitance (fF/µm^2)	0.1	0.1	0.1	0.1	0.1	0.1	0.1
Temp. linearity (ppm/°C)	30	30	30	30	30	30	30
1σ Matching (% µm)	1	1	1	1	1	1	1
Sheet resistance, Rs (Ohm/sq)	200–300	200–300	200–300	200–300	200–300	200–300	200–300
RF							
Metal-Insulator-Metal Capacitor							
Density (fF/µm^2) [2]	7	7	10	10	10	12	12
Voltage linearity (ppm/V^2)	< 100	< 100	< 100	< 100	< 100	< 100	< 100
Leakage (A/cm^2) [9]	<1e-8	<1e-8	<1e-8	<1e-8	<1e-8	<1e-8	<1e-8
σ Matching (%·µm)	0.3	0.3	0.2	0.2	0.2	0.2	0.2
Q (5 GHz for 1pF)	>50	>50	>50	>50	>50	>50	>50
Inductor							
Q (5 GHz, 1nH) [3]	42	44	46	48	50	52	54
MOS Varactor							
Tuning Range [4]	5.5	5.5	5.5	5.5	5.5	5.5	5.5
Q (5 GHz, 0 V)	50	55	55	60	60	60	60
PA							
PA III-V Passives							
Inductors Q (1GHz, 5nH) [5]	30	30	30	30	30	30	30
Capacitor Q [6]	>100	>100	>100	>100	>100	>100	>100
RF capacitor density (fF/µm^2) [7]	2	2	2	2	2	2	2
PA Silicon/SiGe Passives [Table 49 a&b]							
Inductors Q (1GHz, 5nH) [5]	18	18	18	18	18	18	18
Capacitor Q [6]	>100	>100	>100	>100	>100	>100	>100
RF capacitor density (fF/µm^2) [7]	7	7	10	10	10	10	12

Manufacturable solutions exist, and are being optimized	☐
Manufacturable solutions are known	🟨
Interim solutions are known	◆
Manufacturable solutions are NOT known	🟥

Notes for Tables 48 and b:

[1] This capacitance density corresponds to the highest end of the gate oxide thickness for precision analog device in the CMOS table.

[2] No stacking (two capacitors on top of each other) is included. Coloring reflected MIM capacitor meeting all requirements including density, voltage linearity, leakage and matching on copper metallization.

[3] Q at 5 GHz for a single-ended 1nH inductor with a dedicated thick metal (analog metal).

[4] Defined as C_{max}/C_{min} *in C-V curve of the varactor. Varactor align with performance RF device in the CMOS table.*

[5] Inductor Q—quality factor of a 5nH inductor at 1 GHz achievable with the technology with a metallization suitable for handling the power requirements of the PA.

[6] Capacitor Q—quality factor of a 10 pF capacitor at 1 GHz achievable with the technology. Capacitor breakdown voltage must be rated for appropriate power amplification function.

[7] RF capacitor density—capacitor used for all other functions (matching, harmonic filtering, coupling, etc). Capacitor must have adequate breakdown for the given application. No stacking.

[8] Leakage current is defined at room temperature and for the highest end of the supply voltage range and thickness end of the gate oxide thickness for precision analog device in the CMOS table.

[9] Leakage current is defined at room temperature and for the highest end of the supply voltage range for precision analog device in the CMOS table.

Table 49a Power Amplifier Technology Requirements—Near-term Years

Year of Production	*2005*	*2006*	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*
DRAM ½ Pitch (nm) (contacted)	*80*	*70*	*65*	*57*	*50*	*45*	*40*	*36*	*32*
Nominal Battery Voltage	**3.2**	**3.2**	**3.2**	**3.2**	**2.4**	**2.4**	**2.4**	**2.4**	**2.4**
PA Product Solutions	**Single Radio SIP [1]**		**Radio/Baseband SIP [2]**					**Radio/Baseband SIP [2]**	
PA Frequency (GHz)	**0.8–6**		**0.8-6**					**0.8-6**	
III-V HBT Transistor									
F_{max} (at V_{cc}) (GHz)	**45**	**45**	**45**	**45**	**55**	**55**	**55**	**65**	**65**
BV_{CBO} (V)	**25**	**25**	**25**	**25**	**18**	**18**	**18**	**18**	**18**
Linear efficiency (%) [1]	**52**	**52**	**52**	**52**	**55**	**55**	**55**	**55**	**55**
Area (mm^2) *[2]*	**2.5**	**2.5**	**2.5**	**2.5**	**2.2**	**2.2**	**2.2**	**2.2**	**2.2**
Cost/mm^2 *(US\$) [3]*	**0.4**	**0.35**	**0.32**	**0.3**	**0.28**	**0.28**	**0.28**	**0.25**	**0.25**
III-V HBT Integration									
Power management [4]	**N/A**	**N/A**	**N/A**	**N/A**	**N/A**	**N/A**	**N/A**	**N/A**	**N/A**
Switch [5]	**E-PHEMT**	**E-PHEMT**	**E-PHEMT**	**E-PHEMT**	**E-PHEMT**	**E-PHEMT**	**E-PHEMT**	**E-PHEMT**	**E-PHEMT**
Filter [6]	**N/A**	**N/A**	**N/A**	**N/A**	**N/A**	**N/A**	**N/A**	**N/A**	**N/A**
III-V PHEMT Transistor									
F_{max} (at V_{dd}) (GHz)	**45**	**45**	**45**	**45**	**75**	**75**	**75**	**75**	**75**
BV_{DGO} (V)	**20**	**20**	**20**	**20**	**16**	**16**	**16**	**16**	**16**
Linear Efficiency (%) [1]	**55**	**55**	**55**	**55**	**58**	**58**	**58**	**58**	**58**
PA Area (mm^2) *[2]*	**4**	**4**	**4**	**4**	**3.5**	**3.5**	**3.5**	**3.5**	**3.5**
Cost/mm^2 *(US\$) [3]*	**0.4**	**0.28**	**0.28**	**0.25**	**0.24**	**0.24**	**0.24**	**0.22**	**0.22**
III-V PHEMT Integration									
Power management [6]	**N/A**	**N/A**	**N/A**	**N/A**	**N/A**	**N/A**	**N/A**	**N/A**	**N/A**
Switch [5]	**Yes**	**Yes**	**Yes**	**Yes**	**Yes**	**Yes**	**Yes**	**Yes**	**Yes**
Filter [6]	**N/A**	**N/A**	**N/A**	**N/A**	**N/A**	**N/A**	**N/A**	**N/A**	**N/A**
Silicon MOSFET Transistor									
T_{ox} (PA) (Å) [7]	**60**	**60**	**60**	**60**	**35**	**35**	**35**	**35**	**35**
F_{max} (at V_{dd})	**45**	**45**	**45**	**45**	**60**	**60**	**60**	**60**	**60**
BV_{DSS} (V)	**12**	**12**	**12**	**12**	**10**	**10**	**10**	**10**	**10**
Linear efficiency (%) [1]	**45**	**45**	**45**	**45**	**45**	**45**	**45**	**45**	**45**
PA Area (mm^2) *[2]*	**6**	**6**	**6**	**6**	**4.5**	**4.5**	**4.5**	**4.5**	**4.5**
Cost/mm^2 *(US\$) [3]*	**0.08**	**0.08**	**0.08**	**0.08**	**0.06**	**0.06**	**0.06**	**0.05**	**0.05**
Silicon MOSFET Integration									
Power management [4]	**Yes**	**Yes**	**Yes**	**Yes**	**Yes**	**Yes**	**Yes**	**Yes**	**Yes**
Switch [5]	**NO**	**NO**	**NO**	**NO**	**MEMS**	**MEMS**	**MEMS**	**MEMS**	**MEMS**
Filter [6]	**NO**	**NO**	**NO**	**NO**	**NO**	**NO**	**MEMS**	**MEMS**	**MEMS**
SiGe HBT Transistor									
F_{max} (GHz)	**60**	**60**	**60**	**60**	**80**	**80**	**80**	**80**	**80**
BV_{CBO} (V)	**18**	**18**	**18**	**18**	**16**	**16**	**16**	**16**	**16**
Linear efficiency (%) [1]	**50**	**50**	**50**	**50**	**55**	**55**	**55**	**55**	**55**
PA Area (mm^2) *[2]*	**2.5**	**2.5**	**2.5**	**2.5**	**2**	**2**	**2**	**2**	**2**
Cost/mm^2 *(US\$) [3]*	**0.12**	**0.12**	**0.12**	**0.12**	**0.11**	**0.11**	**0.11**	**0.11**	**0.11**
SiGe Integration									
Power management	**Yes**	**Yes**	**Yes**	**Yes**	**Yes**	**Yes**	**Yes**	**Yes**	**Yes**
Switch	**NO**	**NO**	**NO**	**NO**	**MEMS**	**MEMS**	**MEMS**	**MEMS**	**MEMS**
Filter	**NO**	**NO**	**NO**	**NO**	**NO**	**NO**	**MEMS**	**MEMS**	**MEMS**

Table 49b Power Amplifier Technology Requirements—Long-term Years

Year of Production	2014	2015	2016	2017	2018	2019	2020
DRAM ½ Pitch (nm) (contacted)	28	25	22	20	18	16	14
Nominal Battery Voltage	2.4	2.4	2.4	2.4	2.4	2.4	2.4
PA Product Solutions	Radio/Baseband SIP [2]						
PA Frequency (GHz)	0.8-6						
III-V HBT Transistor							
F_{max} (at V_{cc}) (GHz)	65	65	65	65	65	65	65
BV_{CBO} (V)	18	18	18	18	18	18	18
Linear efficiency (%) [1]	55	55	55	55	55	55	55
Area (mm^2) [2]	2.2	2.2	2.2	2	2	2	2
Cost/mm^2 (US$) [3]	0.25	0.25	0.25	0.25	0.25	0.25	0.25
III-V HBT Integration							
Power management [4]	N/A	N/A	N/A	N/A	N/A	N/A	N/A
Switch [5]	E-PHEMT	E-PHEMT	E-PHEMT	E-PHEMT	E-PHEMT	E-PHEMT	E-PHEMT
Filter [6]	N/A	N/A	N/A	N/A	N/A	N/A	N/A
III-V PHEMT Transistor							
F_{max} (at V_{dd}) (GHz)	75	75	75	75	75	75	75
BV_{DGO} (V)	16	16	16	16	16	16	16
Linear Efficiency (%) [1]	58	58	58	58	58	58	58
PA Area (mm^2) [2]	3.5	3.5	3.5	3.5	3.5	3.5	3.5
Cost/mm^2 (US$) [3]	0.22	0.15	0.15	0.15	0.15	0.15	0.15
III-V PHEMT Integration							
Power management [4]	N/A	N/A	N/A	N/A	N/A	N/A	N/A
Switch [5]	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Filter [6]	N/A	N/A	N/A	N/A	N/A	N/A	N/A
Silicon MOSFET Transistor							
T_{ox} (PA) (Å) [7]	35	35	35	35	35	35	35
F_{max} (at V_{dd})	60	60	60	60	60	60	60
BV_{DSS} (V)	10	10	10	10	10	10	10
Linear efficiency (%) [1]	45	45	45	45	45	45	45
PA Area (mm^2) [2]	4.5	4.5	4.5	4.5	4.5	4.5	4.5
Cost/mm^2 (US$) [3]	0.05	0.05	0.05	0.05	0.05	0.05	0.05
Silicon MOSFET Integration							
Power management [4]	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Switch [5]	MEMS	MEMS	MEMS	MEMS	MEMS	MEMS	MEMS
Filter [6]	MEMS	MEMS	MEMS	MEMS	MEMS	MEMS	MEMS
SiGe HBT Transistor							
F_{max} (GHz)	80	80	80	80	80	80	80
BV_{CBO} (V)	16	16	16	16	16	16	16
Linear efficiency (%) [1]	55	55	55	55	55	55	55
PA Area (mm^2) [2]	2	2	2	2	2	2	2
Cost/mm^2 (US$) [3]	0.11	0.11	0.11	0.11	0.11	0.11	0.11
SiGe Integration							
Power management	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Switch	MEMS	MEMS	MEMS	MEMS	MEMS	MEMS	MEMS
Filter	MEMS	MEMS	MEMS	MEMS	MEMS	MEMS	MEMS

Manufacturable solutions exist, and are being optimized	⬜
Manufacturable solutions are known	🟨
Interim solutions are known	◆
Manufacturable solutions are NOT known	🟥

Notes for Table 49a and b:

[1] *Linear efficiency—power added efficiency of the final PA stage under personal communication service (PCS) CDMA (IS-95) modulation.*

[2] *Area—total semiconductor area necessary for the implementation of the quad-band GSM/general packet radio service (GPRS)/ Enhanced Data rates for GSM Evolution (EDGE) PA function, including matching/filtering.*

[3] *Cost/mm^2—approximate commercial foundry cost of the area mentioned in [4].*

[4] *Power management—capability of the technology to provide RF power detection/DC power management for the PA.*

[5] *Switch—capability of the technology to integrate cost-effectively a transmit/receive switch into the PA active die.*

[6] *Filter—capability of the technology to integrate high-quality band selection filters needed for the assumed PA solution; currently performed with surface acoustic wave (SAW) filter technology.*

[7] *T_{ox} (PA)—thickness of the MOSFET transistor in the RF power amplifier function.*

Table 50a Base Station Devices Technology Requirements—Near-term Years

Year of Production	*2005*	*2006*	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*
DRAM ½ Pitch (nm) (contacted)	*80*	*70*	*65*	*57*	*50*	*45*	*40*	*36*	*32*
Application frequency (GHz) [1]	**0.8–2.7**		**0.8–3.5**			**0.8–5**			
Cost ($$/Watt)	**0.7**	**0.6**	**0.5**	**0.4**		**0.3**			**0.25**
Packaging (C-Ceramic, P-Plastic)	**C/P**	**Plastic**							
Si LDMOS									
Operating voltage (V)	**<40**	**<40**	**<50**	**<50**	**<50**	**<50**	**<50**	**<50**	**<50**
Saturated power (Watt)	**240**	**240**	**240**	**240**	**240**	**240**	**240**	**240**	**240**
Saturated power density (W/mm)	**1**	**1.2**	**1.4**	**1.4**	**1.4**	**1.4**	**1.4**	**1.4**	**1.4**
Saturated PAE (%)	**65**	**68**	**65**	**68**	**70**	**65**	**65**	**65**	**70**
Linear power (Watt)	**<120**	**<120**	**<120**	**<120**	**<120**	**<120**	**<120**	**<120**	**<120**
Linear PAE (%)	**50**	**52**	**50**	**52**	**54**	**50**	**50**	**50**	**52**
GaAs FET									
Operating voltage (V)	**28**	**28**	**28**	**28**	**28**	**28**	**28**	**28**	**28**
Saturated power (Watt)	**180**	**180**	**180**	**180**	**180**	**180**	**180**	**240**	**240**
Saturated power density (W/mm)	**1**	**1.2**	**1.5**	**1.5**	**1.5**	**1.8**	**1.8**	**1.8**	**1.8**
Saturated PAE (%)	**68**	**70**	**72**	**68**	**70**	**72**	**72**	**68**	**68**
Linear power (Watt)	**<60**	**<60**	**<60**	**<90**	**<90**	**<90**	**<90**	**<120**	**<120**
Linear PAE (%)	**52**	**55**	**57**	**52**	**54**	**56**	**57**	**52**	**52**
SiC FET									
Operating voltage (V)	**48**	**48**	**48**	**48**	**48**	**48**	**48**	**48**	**48**
Saturated power (Watt)	**60**	**60**	**60**	**120**	**120**	**120**	**120**	**180**	**180**
Saturated power density (W/mm)	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**4**	**4**
Saturated PAE (%)	**45**	**45**	**47**	**42**	**45**	**45**	**47**	**42**	**42**
GaN FET									
Operating voltage (V)	**28**	**28**	**48**	**48**	**48**	**48**	**48**	**48**	**48**
Saturated power (Watt)	**60**	**60**	**120**	**120**	**120**	**180**	**180**	**180**	**180**
Saturated power density (W/mm)	**3**	**3**	**4**	**4**	**5**	**5**	**5**	**5**	**5**
Saturated PAE (%)	**52**	**55**	**55**	**60**	**55**	**60**	**60**	**55**	**60**

Manufacturable solutions exist, and are being optimized	⬜
Manufacturable solutions are known	🟨
Interim solutions are known	◆
Manufacturable solutions are NOT known	🟥

Table 50b Base Station Devices Technology Requirements—Long-term Years

Year of Production	*2014*	*2015*	*2016*	*2017*	*2018*	*2019*	*2020*
DRAM ½ Pitch (nm) (contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
Application frequency (GHz) [1]	**0.8–5**						
Cost ($$/Watt)	**0.25**						
Packaging (C-Ceramic, P-Plastic)	**Plastic**						
Si LDMOS							
Operating voltage (V)	**<50**	**<50**	**<50**	**<50**	**<50**	**<50**	**<50**
Saturated power (Watt)	**240**	**240**	**240**	**240**	**240**	**240**	**240**
Saturated power density (W/mm)	**1.4**	**1.4**	**1.4**	**1.4**	**1.4**	**1.4**	**1.4**
Saturated PAE (%)	**70**	**70**	**70**	**70**	**70**	**70**	**70**
Linear power (Watt)	**<120**	**<120**	**<120**	**<120**	**<120**	**<120**	**<120**
Linear PAE (%)	**52**	**52**	**52**	**52**	**52**	**52**	**52**
GaAs FET							
Operating voltage (V)	**28**	**28**	**28**	**28**	**28**	**28**	**28**
Saturated power (Watt)	**240**	**240**	**240**	**240**	**240**	**240**	**240**
Saturated power density (W/mm)	**1.8**	**1.8**	**1.8**	**1.8**	**1.8**	**1.8**	**1.8**
Saturated PAE (%)	**70**	**70**	**70**	**72**	**72**	**72**	**72**
Linear power (Watt)	**<120**	**<120**	**<120**	**<120**	**<120**	**<120**	**<120**
Linear PAE (%)	**55**	**55**	**55**	**57**	**57**	**57**	**57**
SiC FET							
Operating voltage (V)	**48**	**48**	**48**	**48**	**48**	**48**	**48**
Saturated power (Watt)	**180**	**180**	**180**	**180**	**180**	**180**	**180**
Saturated power density (W/mm)	**4**	**4**	**4**	**4**	**4**	**4**	**4**
Saturated PAE (%)	**42**	**42**	**42**	**42**	**42**	**42**	**42**
GaN FET							
Operating voltage (V)	**48**	**48**	**48**	**48**	**48**	**48**	**48**
Saturated power (Watt)	**240**	**240**	**240**	**240**	**240**	**240**	**240**
Saturated power density (W/mm)	**5**	**5**	**5**	**5**	**5**	**5**	**5**
Saturated PAE (%)	**55**	**60**	**60**	**60**	**60**	**60**	**60**

Manufacturable solutions exist, and are being optimized	⬜
Manufacturable solutions are known	🟨
Interim solutions are known	◆
Manufacturable solutions are NOT known	🟥

Notes for Table 50:

[1] Application frequencies affected device saturated PAE scaling.

Table 51 Millimeter Wave 10 GHz–100 GHz Technology Requirements—Near-term Years UPDATED

Year of Production	*2005*	*2006*	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*
DRAM ½ Pitch (nm) (contacted)	*80*	*70*	*65*	*57*	*50*	*45*	*40*	*36*	*32*
*Device Technology—FET **									
GaAs MESFET (digital mixed-signal)									
Gate length—L physical (nm)	**150**	**150**	**-**	**-**	**-**				
Minimum M1 pitch (nm)	**680**	**680**	**-**	**-**	**-**				
F_t – enhancement mode (GHz)	**120**	**120**	**-**	**-**	**-**				
F_t – depletion mode (GHz)	**100**	**100**	**-**	**-**	**-**				
BV_{GD} (1 mA/mm, V_g=0) (volts)	**5 to 10**	**5 to 10**	**-**	**-**	**-**				
Power delay product at gate delay-FO=1 (fJ at pS)	**1.2 at 18**	**1.2 at 18**	**-**	**-**	**-**				
Shortest DCFL gate delay (pS)	**6**	**6**	**-**	**-**	**-**				
Interconnect metal layers	**5**	**5**	**-**	**-**	**-**				
Interconnect metal	**Al**	**Al**	**-**	**-**	**-**				
Inter line dielectric constant (effective)	**3.1**	**3.1**	**-**	**-**	**-**				
GaAs PHEMT (low noise)									
Gate length (nm)	**100**	**100**	**70**	**70**	**70**	**50**	**50**		
F_t (GHz)	**130**	**130**	**150**	**150**	**170**	**170**	**200**		
Breakdown (volts)	**7.5**	**7.5**	**7**	**7**	**6**	**5**	**5**		
I_{max} (mA/mm)	**700**	**700**	**600**	**600**	**600**	**550**	**550**		
G_m (S/mm)	**0.72**	**0.72**	**0.8**	**0.8**	**0.8**	**0.85**	**0.85**		
NF (dB) at 26 GHz, 18–20 dB associated gain	**2.5**	**2.5**	**2**	**2**	**2**	**1.8**	**1.8**		
NF (dB) at 94 GHz, 8–10 dB associated gain	**4**	**4**	**3.5**	**3.5**	**3.5**	**3.2**	**3.2**		
GaAs PHEMT (power)									
Gate length (nm)	**100**	**100**	**100**	**100**	**70**	**70**	**70**		
F_{max} (GHz)	**150**	**150**	**200**	**200**	**250**	**250**	**250**		
Breakdown (volts)	**11**	**11**	**9**	**9**	**7**	**7**	**7**		
I_{max} (ma/mm)	**750**	**750**	**850**	**850**	**900**	**900**	**900**		
G_m (S/mm)	**0.67**	**0.67**	**0.85**	**0.85**	**0.95**	**0.95**	**0.95**		
P_{out} at 26 GHz and peak efficiency (mW/mm)	**550**	**550**	**600**	**600**	**750**	**750**	**750**		
Peak efficiency at 26 GHz (%)	**30**	**30**	**40**	**40**	**45**	**45**	**45**		
Gain at 26 GHz, at P_{1dB} (dB)***	**12**	**12**	**14**	**14**	**16**	**16**	**16**		
P_{out} at 94 GHz and peak efficiency (mW/mm)	**300**	**300**	**350**	**350**	**350**	**350**	**350**		
Peak efficiency at 94 GHz (%)	**15**	**15**	**20**	**20**	**25**	**30**	**30**		
Gain at 94 GHz, at P_{1dB} (dB)***	**5**	**5**	**6**	**6**	**6**	**7**	**7**		
*Device Technology—FET **									
InP HEMT (low noise)									
Gate length (nm)	**100**	**100**	**70**	**70**	**70**	**50**	**50**		
F_t (GHz)	**210**	**210**	**240**	**240**	**240**	**260**	**260**		
Breakdown (volts)	**3.5**	**3.5**	**3**	**3**	**3**	**2.5**	**2.5**		
I_{max} (ma/mm)	**700**	**700**	**650**	**650**	**650**	**600**	**600**		
G_m (S/mm)	**1**	**1**	**1.2**	**1.2**	**1.2**	**1.3**	**1.3**		
NF (dB) at 26 GHz, 20–23 dB associated gain	**1.8**	**1.8**	**1.5**	**1.5**	**1.5**	**1.3**	**1.3**		
NF (dB) at 94 GHz, 10–13 dB associated gain	**2.5**	**2.5**	**2**	**2**	**2**	**1.8**	**1.8**		
InP HEMT (power)									
Gate length (nm)	**150**	**100**	**100**	**100**	**70**	**70**	**70**		
F_{max} (GHz)	**200**	**220**	**260**	**260**	**260**	**300**	**300**		
Breakdown (volts)	**5**	**5**	**6**	**6**	**6**	**7**	**7**		
I_{max} (ma/mm)	**750**	**700**	**650**	**650**	**650**	**650**	**650**		
G_m (S/mm)	**0.8**	**0.9**	**0.9**	**0.9**	**1**	**1**	**1**		

	Year of Production	*2005*	*2006*	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*
	DRAM ½ Pitch (nm) (contacted)	*80*	*70*	*65*	*57*	*50*	*45*	*40*	*36*	*32*
	P_{out} at 26 GHz and peak efficiency (mW/mm)	400	400	450	450	450	500	500		
	Peak efficiency at 26 GHz (%)	30	40	50	50	50	55	55		
	Gain at 26 GHz, at P_{1dB} (dB)***	12	14	15	15	16	16	16		
	P_{out} at 94 GHz and peak efficiency (mW/mm)	250	300	350	350	400	400	400		
	Peak efficiency at 94 GHz (%)	25	40	40	45	45	45	45		
	Gain at 94 GHz, at P_{1dB} (dB)***	6	8	10	10	12	12	12		
	GaAs MHEMT (low noise)									
	Gate length (nm)	100	100	100	70	70	50	50		
	F_t (GHz)	200	250	300	300	400	400	450		
	Breakdown (volts)	5	5	5	4	4	3	3		
	I_{max} (ma/mm)	680	680	680	680	680	680	680		
	G_m (S/mm)	1	1	1.1	1.1	1.2	1.2	1.2		
	NF (dB) at 26 GHz, 10–23 dB associated gain	1.6	1.6	1.2	1.2	1	1	0.8		
	NF (dB) at 94 GHz, 10–13 dB associated gain	2.5	2.3	2.3	2	2	1.8	1.8		
	*Device Technology—FET **									
	GaAs MHEMT (Power)									
	Gate length (nm)		150	150	100	100	70	70		
Was	F_{max} (GHz)		200	250	275	300	300	300		
Is	F_{max} (GHz)	-	200	250	275	300	300	300		
Was	Breakdown (volts)		8	8	9	9	10	10		
Is	Breakdown (volts)		9	9	11	11	12	12		
Was	I_{max} (ma/mm)		650	700	750	800	800	850		
Is	I_{max} (ma/mm)	-	700	700	750	750	750	800		
	G_m (S/mm)		0.75	0.8	0.85	0.9	0.95	1		
	P_{out} at 26 GHz and peak efficiency (mW/mm)		600	650	700	750	800	850		
	Peak efficiency at 26 GHz (%)		45	55	55	60	60	65		
	Gain at 26 GHz, at P_{1dB} (dB)***		12	15	16	16	16	17		
	P_{out} at 94 GHz and peak efficiency (mW/mm)		250	300	325	350	400	450		
	Peak efficiency at 94 GHz (%)		25	30	35	40	45	45		
	Gain at 94 GHz, at P_{1dB} (dB)***		7	8	10	10	11	12		
	GaN HEMT (low noise)									
Was	Gate length (nm)			150	100	100	70	70		
Is	Gate Length (nm)			~~150~~	150	100	100	70		
Was	F_t (GHz)			100	100	120	150	200		
Is	F_t (GHz)			~~100~~	100	120	150	200		
Was	Breakdown (volts)			40	40	40	40	40		
Is	Breakdown (volts)			~~40~~	40	40	40	40		
Was	I_{max} (ma/mm)			1000	1200	1500	1500	1500		
Is	I_{max} (ma/mm)			~~1000~~	1000	1200	1500	1500		
Was	G_m (S/mm)			0.3	0.4	0.5	0.5	0.5		
Is	G_m (S/mm)			~~0.3~~	0.4	0.4	0.5	0.6		
Was	NF (dB) at 26 GHz, 14 dB gain			2	2	1.5	1	0.8		
Is	NF (dB) at 26 GHz, 14 dB gain			~~2~~	2	1.5	1.5	1		
	GaN HEMT (power)									
Was	Gate length (nm)			150	100	100	70	70		
Is	Gate length (nm)			~~150~~	150	100	100	70		
Was	F_{max} (GHz)			100	100	150	200	200		
Is	F_{max} (GHz)			~~100~~	80	100	125	200		
Was	Breakdown (volts)			40	60	80	100	100		

	Year of Production	*2005*	*2006*	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*
	DRAM ½ Pitch (nm) (contacted)	*80*	*70*	*65*	*57*	*50*	*45*	*40*	*36*	*32*
Is	Breakdown (volts)			~~40~~	40	60	75	100		
Was	I_{max} (ma/mm)			1000	1000	1000	1500	1500		
Is	I_{max} (ma/mm)			~~1000~~	1000	1200	1500	1500		
Was	G_m (S/mm)			0.3	0.4	0.5	0.5	0.5		
Is	G_m (S/mm)			~~0.3~~	0.4	0.5	0.5	0.6		
Was	P_{out} at 26 GHz and peak efficiency (mW/mm)			5000	6000	7000	8000	10000		
Is	P_{out} at 26 GHz and peak efficiency (mW/mm)			~~5000~~	5000	6000	7500	10000		
Was	Peak efficiency at 26 GHz (%)			35	40	50	60	60		
Is	Peak efficiency at 26 GHz (%)			~~35~~	35	40	50	60		
Was	Gain at 26 GHz, at P_{1dB} (dB)***			10	12	12	13	14		
Is	Gain at 26 GHz, at P_{1dB} (dB)***			~~10~~	10	12	13	14		
Was	P_{out} at 44 GHz and peak efficiency (mW/mm)			2000	2000	2000	2500	2500		
Is	P_{out} at 44 GHz and peak efficiency (mW/mm)			~~2000~~	2000	2500	3000	3500		
Was	Peak efficiency at 44 GHz (%)			35	35	35	40	40		
Is	Peak efficiency at 44 GHz (%)			~~35~~	35	40	50	50		
Was	Gain at 44 GHz, at P_{1dB} (dB)***			8	8	8	9	9		
Is	Gain at 44 GHz, at P_{1dB} (dB)***			~~8~~	6	8	9	10		
	*Device Technology—HBT **									
	InP HBT									
	Emitter width (nm)	350	350	250	250	150	150	150		
Was	*Emitter Area (square microns)*	1	0.75	0.75	0.5	0.5	0.4	0.4		
Is	*Emitter Area (square microns)*	1	0.75	0.75	0.5	0.5	0.4	0.4		
Was	F_t (GHz)	300	300	350	350	400	400	400		
Is	F_t (GHz)	300	300	350	350	400	400	400		
Was	F_{max} (GHz)	300	300	400	400	450	450	450		
Is	F_{max} (GHz)	300	300	400	400	450	450	450		
	Breakdown (BV_{CEO}) (volts)	4	4	4	4	3	3	3		
	$I_{max}/\mu m^2$ ($mA/\mu m^2$)	4	5	5	5	7	7	7		
	Beta	50	50	50	50	50	50	50		
	3 sigma V_{BE} (mV)	40	30	30	25	25	20	20		
	Interconnect metal layers	4	4	5	5	5				
	Interconnect metal	Al, Au	Al, Au	Al, Au, Cu	Al, Au, Cu	Al, Au, Cu	Al, Au, Cu	Al, Au, Cu		
	Barrier	PVD	PVD	IMP	IMP	IMP	IMP	IMP		
	Wafer diameter (mm)	100	100	150	150	150	150	150		
	SiGe HBT									
	Emitter Width (nm)	150	140	130	120	100	100	100		
	Peak F_t (GHz) B_{bc}=1V	200	230	265	300	350	370	385		
	Peak Fmax (GHz)	240	260	300	330	390	410	425		
	Breakdown (BV_{CBO}) (volts)	5.3	5	5	4.5	4.5	4.3	4.3		
	Breakdown (BV_{CEO}) (volts)	2	1.9	1.8	1.7	1.7	1.7	1.7		
	$I_{max}/\mu m^2$ ($mA/\mu m^2$)	10	11	12	13	14	15	16		
	Beta	200	200	250	250	300	325	350		
	Nf_{min} at 77 GHz (dB)	5.5	5.1	4.6	4.3	3.9	3.8	3.7		

Manufacturable solutions exist, and are being optimized	⬜
Manufacturable solutions are known	🟨
Interim solutions are known	◆
Manufacturable solutions are NOT known	🟥

** Lithography dimensions are drawn dimensions.*

*** Output power at peak efficiency is generally at 2 to 3 dB into compression; P_{out} is normalized to total gate periphery.*

**** P_{1dB} (dB) is the point at which the device gain is 1 dB less than the linear gain, i.e., the gain is compressed by 1 dB.*

REFERENCES

X. Huo, M. Zhang, P. C. H. Chan, Q. Liangf, and Z. K. Tang, *"High Frequency S Parameters Characterization of Back-Gate Carbon Nanotube Field-Effect Transistors,"* in Technical Digest of the 2004 International Electron Devices Meeting, ISBN: 0-7803-8684-1, San Francisco, CA, December 13–15, 2004, pp. 691–694.