

INTERNATIONAL  
TECHNOLOGY ROADMAP  
FOR  
SEMICONDUCTORS  
2006 UPDATE  
FINAL DRAFT

SYSTEM DRIVERS

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# SYSTEM DRIVERS

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## SUMMARY

The 2006 update of the System Drivers Chapter is a step in the direction of market-driven drivers that reflect the demands of a 21st-century roadmap. Driving towards the 2007 version of the roadmap, the set of main drivers is moving towards becoming a market-driven set, including driver segments such as office, consumer mobile drivers. This year one more driver is added, the consumer stationary driver, that represents a high-performance version of the increasingly important consumer electronics market. Other existing drivers have been reviewed to ensure the direction is appropriate. A complete set of market-driven drivers is expected for the 2007 version of the System Drivers roadmap, for which the plan is on track.

## 2 System Drivers

Table 8 Major Product Market Segments and Impact on System Drivers

Market Drivers	SOC	Analog/MS	MPU
<i>I. Portable/consumer</i>			
1. Size/weight ratio: peak in 2004 2. Battery life: peak in 2004 3. Function: 2×/2 years 4. Time-to-market: ASAP	Low power paramount  Need SOC integration (DSP, MPU, I/O cores, etc.)	Migrating on-chip for voice processing, A/D sampling, and even for some RF transceiver function	Specialized cores to optimize processing per microwatt
<i>II. Medical</i>			
1. Cost: slight downward pressure (~1/2 every 5 years) 2. Time-to-market: >12 mos 3. Function: new on-chip functions 4. Form factor often not important 5. Durability/safety 6. Conservation/ ecology	High-end products only. Reprogrammability possible. Mainly ASSP, especially for patient data storage and telemedicine; more SOC for high-end digital with cores for imaging, real-time diagnostics, etc.	Absolutely necessary for physical measurement and response but may not be integrated on chip	Often used for programmability especially when real-time performance is not important.  Recent advances in multi-core processors have made programmability and real-time performance possible
<i>III. Networking and communications</i>			
1. Bandwidth: 4×/3–4 yrs. 2. Reliability 3. Time-to-market: ASAP 4. Power: W/m <sup>3</sup> of system	Large gate counts High reliability More reprogrammability to accommodate custom functions	Migrating on-chip for MUX/DEMUX circuitry  MEMS for optical switching.	MPU cores, FPGA cores and some specialized functions
<i>IV. Defense</i>			
1. Cost: not prime concern 2. Time-to-market: >12 mos 3. Function: mostly on SW to ride technology curve 4. Form factor may be important 5. High durability/safety	Most case leverage existing processors but some requirements may drive towards single-chip designs with programmability	Absolutely necessary for physical measurement and response but may not be integrated on chip	Often used for programmability especially when real-time performance is not important  Recent advances in multi-core processors have made programmability and real-time performance possible
<i>V. Office</i>			
1. Speed: 2×/2 years 2. Memory density: 2×/2 years 3. Power: flat to decreasing, driven by cost and W/m <sup>3</sup> 4. Form factor: shrinking size 5. Reliability	Large gate counts  High speed  Drives demand for digital functionality  Primarily SOC integration of custom off-the-shelf MPU and I/O cores	Minimal on-chip analog  Simple A/D and D/A  Video i/f for automated camera monitoring, video conferencing  Integrated high-speed A/D, D/A for monitoring, instrumentation, and range-speed-pos resolution	MPU cores and some specialized functions  Increased industry partnerships on common designs to reduce development costs (requires data sharing and reuse across multiple design systems)
<i>VI. Automotive</i>			
1. Functionality 2. Ruggedness (external environment, noise) 3. Reliability and safety 4. Cost	Mainly entertainment systems.  Mainly ASSP, but increasing SOC for high end using standard HW platforms with RTOS kernel, embedded software.	Cost-driven on-chip A/D and D/A for sensor and actuators  Signal processing shifting to DSP for voice, visual  Physical measurement (“communicating sensors” for proximity, motion, positioning). MEMS for sensors	

A/D—*analog to digital* ASSP—*application-specific standard product* D/A—*digital to analog* DEMUX—*demultiplexer*  
 DSP—*digital signal processing* FPGA—*field programmable gate array* i/f—*intermediate frequency* I/O—*input/output* HW—*hardware*  
 MEMS—*microelectromechanical systems* MUX—*multiplex* RTOS—*real-time operating system*

## SYSTEM ON CHIP DRIVER

Table 9 SOC-PE Design Productivity Trends

	2005	2006	2007	2008	2009	2010	2011	2012	2013	2014	2015	2016	2017	2018	2019	2020
Trend: SOC total logic size (normalized to 2005)	1.00	1.27	1.62	2.15	2.81	3.42	4.27	5.50	6.58	8.54	10.69	13.77	16.69	20.62	26.12	34.15
Requirement % of reused design	30%	34%	38%	42%	46%	50%	54%	58%	62%	66%	70%	74%	78%	82%	86%	90%
Requirement productivity for new designs (normalized to 2005)	1.00	1.24	1.54	2.00	2.54	3.02	3.67	4.59	5.34	6.73	8.18	10.2	12.0	14.3	17.5	22.1
Requirement productivity for reused designs (normalized to productivity for new designs at 2005)	2.00	2.48	3.08	4.00	5.09	6.04	7.33	9.19	10.7	13.5	16.4	20.4	24.0	28.6	35.0	44.2

### NEW —SOC CONSUMER STATIONARY DRIVER (SOC-CS)

The SOC-CS( Consumer Stationary ) is a driver represents SOC designs—it includes wide variety of applications in the area of digital consumer electronic equipments such as high-end game machine, and those are assumed to be typically used in not mobile environment. Key aspects of the model are as follows:

- Processing performance is most important differentiator. As shown in Figure 17, required processing performance in year 2020 will be more than 70 TFLOPS.
- As Functions will be implemented and realized mainly by software, high processing power is required, and hence this SOC has to have many data processing engine( DPE ).
- Comparing with the SOC Consumer Portable, not so good as in terms of performance per power consumption, but better than in terms of functional flexibility in case of adding or modifying functions.
- The life cycle of those SOC-CS is relatively long, because it is easy to add or modify functions, and as a result the application area is wide.

Figure 16 shows a typical architecture template for SOC-CS. The SOC will feature a highly parallel architecture, and consist of a number of main processors, a number of DPEs( Data Processing Engine ), and IO for Memory Interface and Chip-to-Chip Interface.

A DPE is a processor dedicated for executing data processing achieving high speed processing by reducing the general purpose features. A Main Processor is general purpose processor, which allocates and does scheduling jobs to DPEs. Pair of a Main Processor and a number of DPEs structures basic architecture, here, number of DPEs will be determined by required performance and chip size. Possible largest number of DPEs will be on this SOC in order to achieve required performance.

## 4 System Drivers

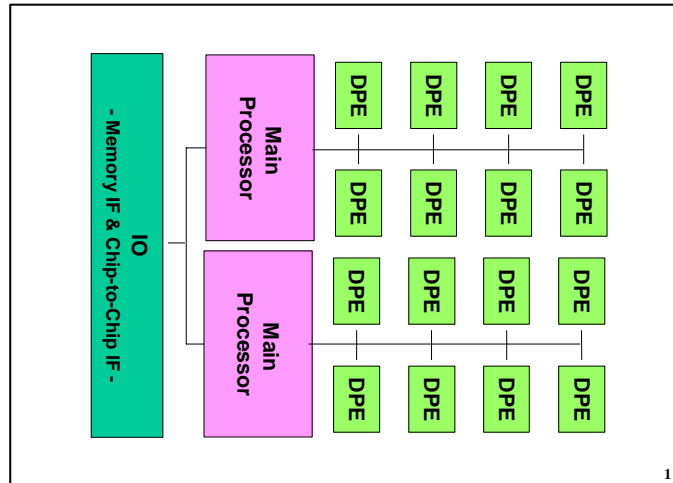
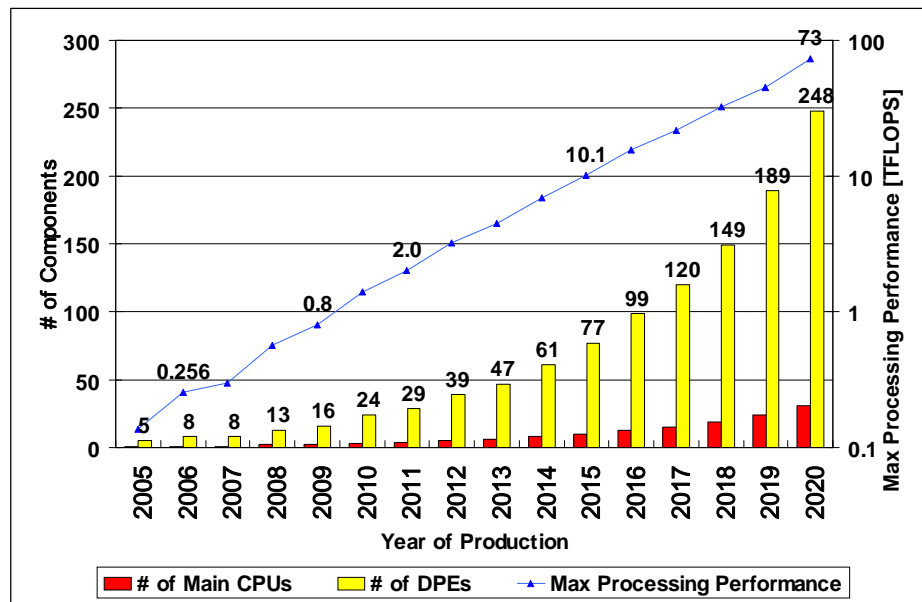


Figure 16 SOC Consumer Stationary Architecture Template *NEW*

### **SOC-CS POWER CONSUMPTION TRENDS**

Based on the architecture template, design-quantified design complexity trends for the SOC-CS driver are shown in Figure 17. The most interesting factor is the number of DPEs, which will rapidly grow. The followings are basic assumptions made for these design complexity trends.

- The SOC die size stays constant around 220mm<sup>2</sup> this is come from published information on the state-of-the-art gaming processor.
- Pair of a Main Processor and a number of DPEs structures basic architecture, here, number of DPEs will be determined by required performance and chip size.
- Possible largest number of DPEs will be on this SOC in order to achieve required performance.
- Circuit size of both Main Processor and DPE stays constant, and then area size will go down in proportion to the square of metal 1 pitch.
- A Main Processor is assumed to able to control up to 8 DPEs.



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Figure 17 SOC Consumer Stationary Design Complexity Trends *NEW*

### SOC-CS PERFORMANCE TRENDS

Figure 18 shows SOC-CS processing performance trends. As a basic assumption, processing performance will be improved in proportion to the device performance itself times the increase in the number of DPEs. The requirement for the processing performance will very rapidly grow more than 200 times in the next fifteen years. Important solutions to achieve the required performance include various design technologies to maximize the device performance. Automated design methodologies such as high-level synthesis are of course important, while very considerate design technologies particularly in Logic-Circuit-Physical design stage is highly desirable.

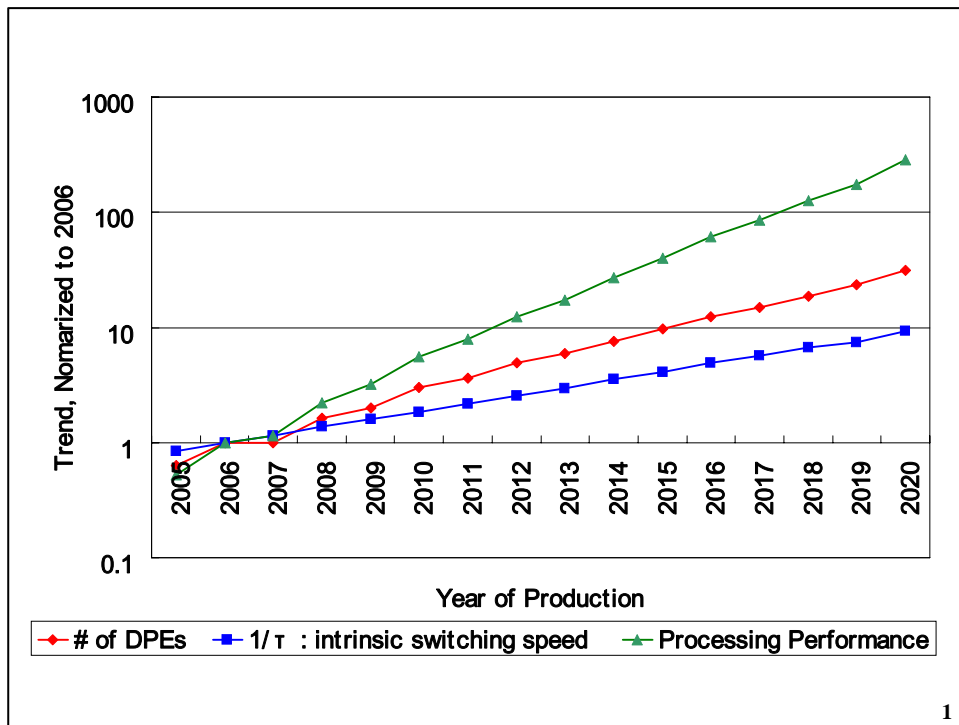


Figure 18 SOC Consumer Stationary Performance Trends *NEW*

### SOC-CS POWER CONSUMPTION TRENDS

Power consumption explosion is a critical factor for the design of SOC-CS chips. Figure 19 shows the trend for total chip power decomposing switching and leakage, also logic portion and memory portion respectively, using the transistor performance parameters from the PIDS requirement table, interconnect performance parameters from the Interconnect requirement table, and the SOC-CS design complexity trends assumed in this section. Initial power consumption value as of 2005 comes from gaming processor published data.

To better understand the trends shown in the figure, we note the following:

- Different from the SOC Consumer Mobile, the SOC-CS is generally free from the battery life issue, however rapid power consumption growth has a critical impact on chip packaging issue and cooling issue.
- Leakage power will be much more than the calculated value shown in Figure 19 because of variability and temperature effects.
- Power consumption per a DPE itself will be reduced because the decreasing factor such as V<sub>dd</sub> and insulator dielectric constant become dominant.

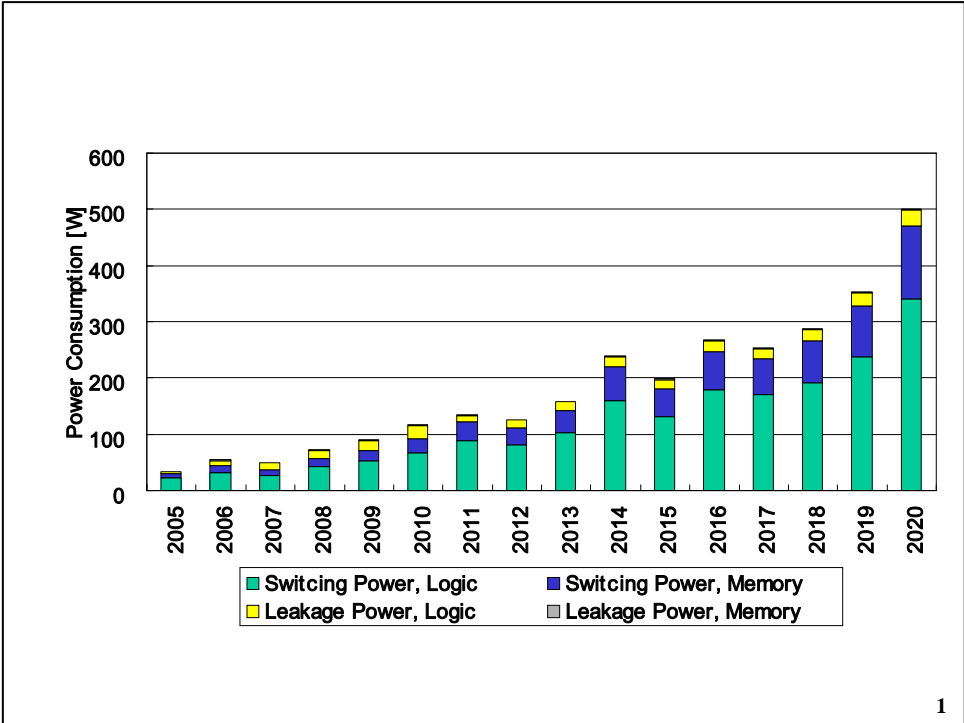


Figure 19 SOC Consumer Stationary Power Consumption Trends NEW

## MIXED-SIGNAL DRIVER

Table 10 Projected Mixed-Signal Figures of Merit for Four Circuit Types.

Year of Production	2005	2008	2011	2014	2017	2020	Driver
RF-CMOS $\frac{1}{2}$ Pitch	90	65	45	32	22	18	
$FoM_{LNA}$ [GHz]	80	160	200–300	300–400	400–600	500–700	Refer to the RF and AMS Technologies for Wireless chapter
$FoM_{VCO}$ [1/J] $10^{22}$	0.9	1.1	1.5	2	2.4	3	
$FoM_{PA}$ [ $W \times GHz^2$ ] $10^4$	10	20	40	60–80	90–100	110–130	
$FoM_{ADC}$ [GHz/W] $10^3$	1.2	2	3–4	4–10	6–20	8–40	

## EMBEDDED MEMORY DRIVER

Table 11a Embedded Memory Requirements—Near-term

Year of Production	2005	2006	2007	2008	2009	2010
DRAM $\frac{1}{2}$ Pitch (nm)	80	70	65	55	50	45
CMOS SRAM High-performance, low standby power (HP/LSTP) DRAM $\frac{1}{2}$ pitch (nm), Feature Size – F	90	90	65	65	65	45
6T bit cell size ( $F^2$ ) [1]	140F <sup>2</sup>	140F <sup>2</sup>	140F <sup>2</sup>	140F <sup>2</sup>	140F <sup>2</sup>	140F <sup>2</sup>
Array efficiency [2]	0.7	0.7	0.7	0.7	0.7	0.7
Process overhead versus standard CMOS – number of added mask layers [3]	1	2	2	2	2	2
Operating voltage – $V_{dd}$ (V) [4]	1.1/1.2	1.1/1.2	1.1	1/1.1	1/1.1	1
Static power dissipation (mW/Cell) [5]	1.5E-4/6E-7	1.5E-4/6E-7	3E-4/1E-6	3E-4/1E-6	3E-4/1E-6	5E-4/1.2E-6
Dynamic power consumption per cell – (mW/MHz) [6]	7E-7/8.5E-7	6E-7/8E-7	4.5E-7/7E-7	4E-7/6.5E-7	4E-7/6E-7	3E-7/5E-7
Read cycle time (ns) [7]	0.4/2	0.4/2	0.3/1.5	0.3/1.5	0.3/1.5	0.2/1.2
Write cycle time (ns) [7]	0.4/2	0.4/2	0.3/1.5	0.3/1.5	0.3/1.5	0.2/1.2
Percentage of MBU on total SER	8%	8%	16%	16%	16%	32%
Soft error rate (FIT/Mb) [8]	1100	1100	1150	1150	1150	1200
Embedded Non-Volatile Memory (code/data), DRAM $\frac{1}{2}$ pitch (nm)	130	130	90	90	90	65
Cell size ( $F^2$ ) – NOR FLOTOX /NAND FLOTOX [9]	10F <sup>2</sup> /5F <sup>2</sup>	10F <sup>2</sup> /5F <sup>2</sup>	10F <sup>2</sup> /5F <sup>2</sup>	10F <sup>2</sup> /5F <sup>2</sup>	10F <sup>2</sup> /5F <sup>2</sup>	10F <sup>2</sup> /5F <sup>2</sup>
Array efficiency – NOR FLOTOX/NAND FLOTOX [10]	0.6/0.8	0.6/0.8	0.6/0.8	0.6/0.8	0.6/0.8	0.6/0.8
Process overhead versus standard CMOS – number of added mask layers [11]	6–8	6–8	6–8	6–8	6–8	6–8
Read operating voltage (V)	2.5V	2.5V	2V	2V	2V	1.8V
Write (program/erase) on chip maximum voltage (V) – NOR/NAND [12]	12V/15V	12V/15V	12V/15V	12V/15V	12V/15V	12V/15V
Static power dissipation (mW/Cell) [5]	1.E-06	1.E-06	1.E-06	1.E-06	1.E-06	1.E-06
Dynamic power consumption per cell – (mW/MHz) [6]	0.8E-08	0.8E-08	0.6E-08	0.6E-08	0.6E-08	0.6E-08
Read cycle time (ns) NOR FLOTOX /NAND FLOTOX [7]	14/70	14/70	10/50	10/50	10/50	7/35

Program time per cell ( $\mu$ s) NOR FLOTOX /NAND FLOTOX [13]	<b>1.0/1000.0</b>	<b>1.0/1000.0</b>	<b>1.0/1000.0</b>	<b>1.0/1000.0</b>	<b>1.0/1000.0</b>	<b>1.0/1000.0</b>
Erase time per cell (ms) NOR FLOTOX /NAND FLOTOX [13]	<b>10.0/0.1</b>	<b>10.0/0.1</b>	<b>10.0/0.1</b>	<b>10.0/0.1</b>	<b>10.0/0.1</b>	<b>10.0/0.1</b>
Data retention requirement (years) [13]	<b>10</b>	<b>10</b>	<b>10</b>	<b>10</b>	<b>10</b>	<b>10</b>
Endurance requirement [13]	<b>100000</b>	<b>100000</b>	<b>100000</b>	<b>100000</b>	<b>100000</b>	<b>100000</b>
<i>Embedded DRAM, 1/2 pitch (nm)</i>	<i>130</i>	<i>90</i>	<i>90</i>	<i>90</i>	<i>65</i>	<i>65</i>
1T1C bit cell size ( $F^2$ ) [14]	<b>12–30</b>	<b>12–30</b>	<b>12–30</b>	<b>12–30</b>	<b>12–30</b>	<b>12–30</b>
Array efficiency [2]	<b>0.6</b>	<b>0.6</b>	<b>0.6</b>	<b>0.6</b>	<b>0.6</b>	<b>0.6</b>
Process overhead versus standard CMOS – number of added mask layers [3]	<b>3–5</b>	<b>3–5</b>	<b>3–5</b>	<b>3–5</b>	<b>3–5</b>	<b>3–5</b>
Read operating voltage (V)	<b>2.5</b>	<b>2</b>	<b>2</b>	<b>2</b>	<b>1.8</b>	<b>1.7</b>
Static power dissipation (mW/Cell) [5]	<b>1E-11</b>	<b>1E-11</b>	<b>1E-11</b>	<b>1E-11</b>	<b>1E-11</b>	<b>1E-11</b>
Dynamic power consumption per cell – (mW/MHz) [6]	<b>1.E-07</b>	<b>1.E-07</b>	<b>1.E-07</b>	<b>1.E-07</b>	<b>1.E-07</b>	<b>1.5E-07</b>
DRAM retention time (ms) [13]	<b>64</b>	<b>64</b>	<b>64</b>	<b>64</b>	<b>64</b>	<b>64</b>
Read/Write cycle time (ns) [7]	<b>1</b>	<b>0.7</b>	<b>0.7</b>	<b>0.7</b>	<b>0.5</b>	<b>0.4</b>
Soft error rate (FIT/Mb) [8]	<b>60</b>	<b>60</b>	<b>60</b>	<b>60</b>	<b>60</b>	<b>60</b>

*FIT—failures in time FLOTOX—floating gate tunnel oxide MBU—multiple bit upsets NAND—not an “AND” logic operation  
NOR—not an “OR” logic operation*

Table 11b Embedded Memory Requirements—Long-term\*

<i>Year of Production</i>	2012	2015	2018
<i>DRAM ½ Pitch (nm)</i>	36	25	18
<i>CMOS SRAM High-performance, low standby power (HP/LSTP) DRAM 1/2 pitch (nm), Feature Size – F</i>	35	25	18
6T bit cell size (F <sup>2</sup> ) [1]	<b>140F<sup>2</sup></b>	<b>140F<sup>2</sup></b>	<b>140F<sup>2</sup></b>
Array efficiency [2]	<b>0.7</b>	<b>0.7</b>	<b>0.7</b>
Process overhead versus standard CMOS – number of mask adders [3]	<b>2</b>	<b>2</b>	<b>2</b>
Operating voltage – V <sub>dd</sub> (V)	<b>0.9/1</b>	<b>0.8/0.9</b>	<b>0.7/0.8</b>
Static power dissipation (mW/Cell) [5]	<b>1E-3/1.5E-6</b>	<b>2E-3/2E-6</b>	<b>3E-3/2.5E-6</b>
Dynamic power consumption per cell – (mW/MHz) [6]	<b>2.5E-7/4.5E-7</b>	<b>2E-7/4E-7</b>	<b>1.5E-7/3E-7</b>
Read cycle time (ns) [7]	<b>0.15/0.8</b>	<b>0.1/0.5</b>	<b>0.07/0.3</b>
Write cycle time (ns) [7]	<b>0.15/0.8</b>	<b>0.1/0.5</b>	<b>0.07/0.3</b>
Percentage of MBU on total SERs	<b>64%</b>	<b>100%</b>	<b>100%</b>
Soft error rate (FIT/Mb) [8]	<b>1250</b>	<b>1300</b>	<b>1350</b>
<i>Embedded Non-Volatile Memory (code/data), DRAM ½ pitch (nm)</i>	45	35	25
Cell size (F <sup>2</sup> ) – NOR FLOTOX/NAND FLOTOX [9]	<b>10F<sup>2</sup>/5F<sup>2</sup></b>	<b>10F<sup>2</sup>/5F<sup>2</sup></b>	<b>10F<sup>2</sup>/5F<sup>2</sup></b>
Array efficiency – NOR FLOTOX/NAND FLOTOX [10]	<b>0.6/0.8</b>	<b>0.6/0.8</b>	<b>0.6/0.8</b>
Process overhead versus standard CMOS – number of mask adders [3]	<b>6–8</b>	<b>6–8</b>	<b>6–8</b>
Read operating voltage (V) [4]	<b>1.5V</b>	<b>1.3V</b>	<b>1.2V</b>
WRITE (program/erase) on chip maximum voltage (V) – NOR/NAND [4]	<b>12V/15V</b>	<b>12V/15V</b>	<b>12V/15V</b>
Static power dissipation (mW/Cell) [5]	<b>1.E-06</b>	<b>1.E-06</b>	<b>1.E-06</b>
Dynamic power consumption per cell – (mW/MHz) [6]	<b>0.4E-8</b>	<b>0.35E-8</b>	<b>0.3E-8</b>
Read cycle time (ns)	<b>5/25</b>	<b>3.5/18</b>	<b>2.5/12</b>
Program time per cell (µs) [13]	<b>1.0/1000.0</b>	<b>1.0/1000.0</b>	<b>1.0/1000.0</b>
Erase time per cell (ms) [13]	<b>10.0/0.1</b>	<b>10.0/0.1</b>	<b>10.0/0.1</b>
Data retention requirement (years) [13]	<b>10</b>	<b>10</b>	<b>10</b>
Endurance requirement [13]	<b>100000</b>	<b>100000</b>	<b>100000</b>
<i>Embedded DRAM, ½ pitch (nm)</i>	45	35	25
1T1C bit cell size (F <sup>2</sup> ) [14]	<b>12–30</b>	<b>12–30</b>	<b>12–30</b>
Array efficiency [2]	<b>0.6</b>	<b>0.6</b>	<b>0.6</b>
Process overhead versus standard CMOS – number of mask adders [3]	<b>3–6</b>	<b>3–6</b>	<b>3–6</b>
Read operating voltage (V)	<b>1.6</b>	<b>1.5</b>	<b>1.5</b>
Static power dissipation (mW/Cell) [5]	<b>1E-11</b>	<b>1E-11</b>	<b>1E-11</b>
Dynamic power consumption per cell – (mW/MHz) [6]	<b>1.6E-07</b>	<b>1.7E-07</b>	<b>1.7E-07</b>
DRAM retention time (ms) [13]	<b>64</b>	<b>64</b>	<b>64</b>
Read/Write cycle time (ns) [7]	<b>0.3</b>	<b>0.25</b>	<b>0.2</b>
Soft error rate (FIT/Mb) [8]	<b>60</b>	<b>60</b>	<b>60</b>

\*Table 11b data will be annualized in 2006. For the 2005 ITRS, long-term years are 2014–2020.

*Definitions of Terms for Tables 11a and 11b:*

[1] Size of the standard 6T CMOS SRAM cell as a function of minimum feature size.

[2] Typical array efficiency defined as (core area/memory instance area).

[3] Typical number of extra masks is needed over standard CMOS logic process of equivalent technology. This is typically zero, however for some high-performance or highly reliable (noise immune) SRAMs special process options are sometimes applied like additional high- $V_{th}$  pMOS cell transistors and using higher  $V_{dd}$  for better noise margin or zero- $V_{th}$  access transistors for fast read-out.

[4] Nominal operating voltage refers to the HP and LSTP devices in the logic device requirements table in the PIDS chapter.

[5] Static power dissipation per cell in standby mode. This is measured at  $I_{standby} \times V_{dd}$ . (off-current and  $V_{dd}$  are taken from the HP and LSTP devices in the logic device requirements table in the PIDS Chapter.

[6] This parameter is a strong function of array architecture. However, a parameter for technology can be determined per cell level. Assume full  $V_{dd}$  swing on the Wordline (WL) and 0.8  $V_{dd}$  swing on the Bitline (BL). Determine the WL capacitance per cell (CWL) and BL capacitance per cell (CBL). Then: dyn. power cons. per MHz per cell =  $V_{dd} \times CWL$  (per cell)  $\times (V_{dd}) + V_{dd} \times CBL$  (per cell)  $\times (V_{dd}) \times 10^6$ .

[7] Read cycle time is the typical time it takes to complete a READ operation from an address. Depends on memory size and architecture. Write cycle time is the typical time it takes to complete a WRITE operation to an ADDR. Depends on memory size and architecture.

[8] A FIT is a failure in 1 billion hours. This data is presented as FIT per megabit.

[9] Size of the standard 1T FLOTOX cell/size of the standard 2T select gate (SG) cell/size of the standard NAND cell. Cell size is somewhat enhanced compared to stand-alone NVM due to integration issues.

[10] Array efficiency of the standard stacked gate NOR architecture/standard split gate NOR architecture/standard NAND architecture. Data refer to PIDS table the NVM device requirements table in the PIDS chapter.

[11] Extra process steps needed to realize the technology as compared to standard CMOS process.

[12] Maximum voltage required for operation, typically used in WRITE operation. Data refer to the NVM device requirements table in the PIDS chapter.

[13] Program time per cell is typically the time needed to program data to a cell. Erase time per cell is typically the time needed to erase a cell. Data retention requirement is the duration for which the data must remain non-volatile even under worst-case conditions. Endurance requirement specifies the number of times the cell can be programmed and erased.

[14] Size of the standard cell for embedded trench DRAM cell. Data refers to the DRAM requirements table in the PIDS chapter.