International Technology Roadmap for Semiconductors

Assembly and Packaging 2006

July 12, 2006

Assembly and Packaging Roadmap 2006 Participants

W. R.Bottoms - Chair				William Chen -Co-Chair
United States		**Japan**	**Europe**	**Singapore**
Abhay Maheshwari	Keith Newman	Eiji Yoshida	Bernd Appelt	Kripesh Vaidyanathan
Bob Pfahl	Kishor Desai	Henry Utsunomiya	Bernd Roemer	
Charles Reynolds	Lei Mercado	Hirofumi Nakajima	Coen Tak	
Chi-Shih Chang	Luu Nguyen	Hisao Kasuga	Gilles Poupon	**Korea**
Bob Chylak	Mario Bolanos	Kazuo Nishiyama	Klaus Pressel	Jason Cho
Debendra Mallik	Martin Bayes	Masanao Yano	Max Juergen Wolf	Choon Heung Lee
George Harman	Muhannad Bakir	Michitaka Kimura	Ralf Plieninger	Dongho Lee
Harold.Hosack	Ralph K. Cavin	Nobuo Futawatari	Jean-Pierre Moscicki	Kwang Yoo Byun
James Bird	Richard Arnold	Ryo Haruta		Sonjin Cho
James Wilcox	Stan Mihelcic	Shigeki Ueda	**Taiwan**	Yong-Bin Sun
Joseph Adam	Voya Markovich	Shigeru Utsumi	Carl Chen	
Zhiping Yang	Susan Vitkavage	Shoji Uegaki	Mike Hung	
		Shuya Haruguchi	Rongshen Lee	
		Takashi Takata	Clinton Chao	
			Sebastian Liau	

ITRS A&P Chapter Organization

- Scope
- Difficult Challenges
- Technical Requirements
- Infrastructure Challenges
- Potential Solutions
- Tables

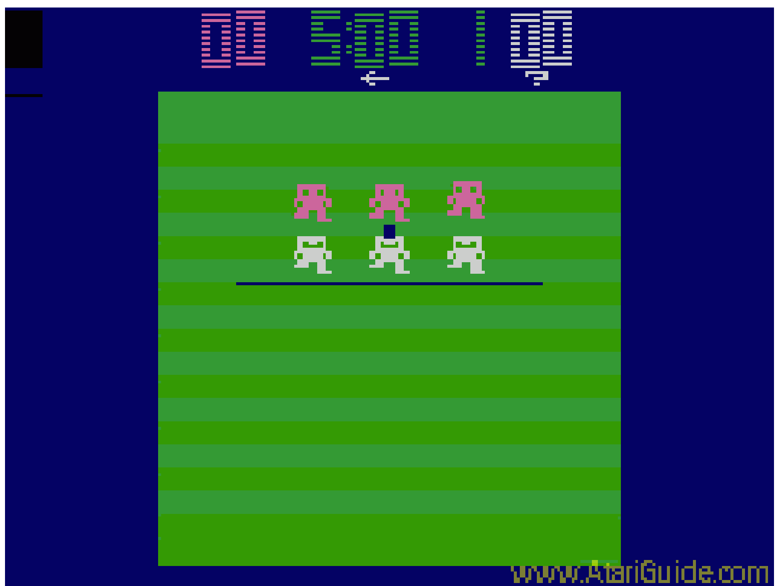
Assembly and Packaging Roadmap 2006

- Packaging has become the limiting element in system cost and performance
- The Assembly and packaging role is expanding to include system level integration functions.
- As traditional Moore's law scaling become more difficult innovation in assembly and packaging innovation can take up the slack.

Computing System performance increase continues

Example: Game Console

from this…



Mini Football video game
Circa: 1990s

to this…

Assembly and Packaging Emerging as Limiting Factor for Cost and Performance

- Consumers now drive more than half of integrated circuit revenue
- Assembly and Packaging technology is a primary differentiator for consumer electronics
- These factors are driving an unprecedented pace of innovation in:
  - New Materials
  - New Technologies
  - New Systems Integration

Assembly and Packaging

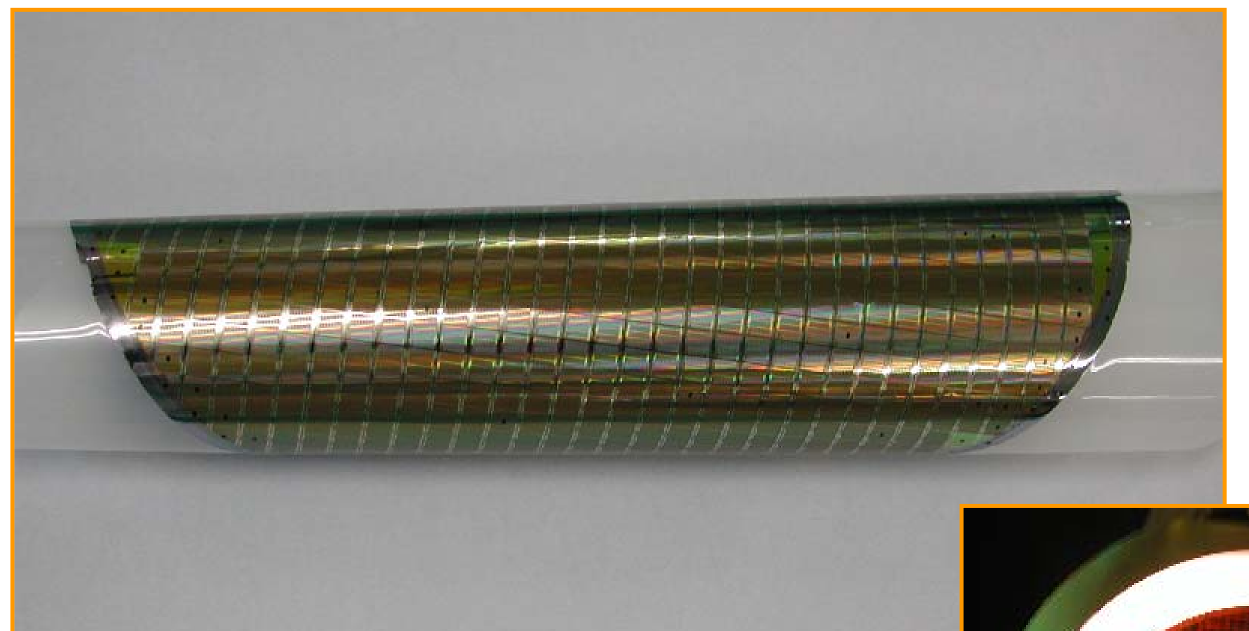
The pace of change in several areas is faster than anticipated

- System in a package (SiP) has become the structure of choice for many consumer products with new requirements for package design, materials, processing and test access
- Wafer thinning has progressed to a level requiring special handling and assembly processes
- Stacked die package layer count is increasing rapidly requiring new methods for bonding, testing, etc.

New Packaging Technologies

- Thinned wafers
- 3D systems integration
- Wafer level packaging
- Bio-chips
- Integrated optics
- Embedded/integrated active and passive devices
- MEMS
- Printable circuits
  - Semiconductors
  - Light emitters
  - RF
  - Interconnect
- Flexible (wearable) electronics

Thinned Wafers/Die



(a) Rolled Wafer

10μm Thickness Wafer

(b) Light
Transparency

Source: Shinko Electric Industry,

Systems Integration in the Cellular Phone

It is not only integrated circuits

Embedded Antenna
- Smaller・ Stability of signal
- Influence on the human body

Camera Circuit
- Smaller
- Lower power consumption
- One unit of lens and control circuit

LCD Circuit
- Larger display, Color display
- Lower power consumption
- Higher resolution

Memory Circuit
- Memory area for downloaded software
- Higher memory capacity

DSP・ CPU・ BB
- Dual CPU: Transmission /Application

Plug In Memory Card
- Smaller, thinner
- Higher memory capacity

Tx、Rx Circuit
- Smaller & lower power consumption of analog circuit
- Decrease of # of mounted components

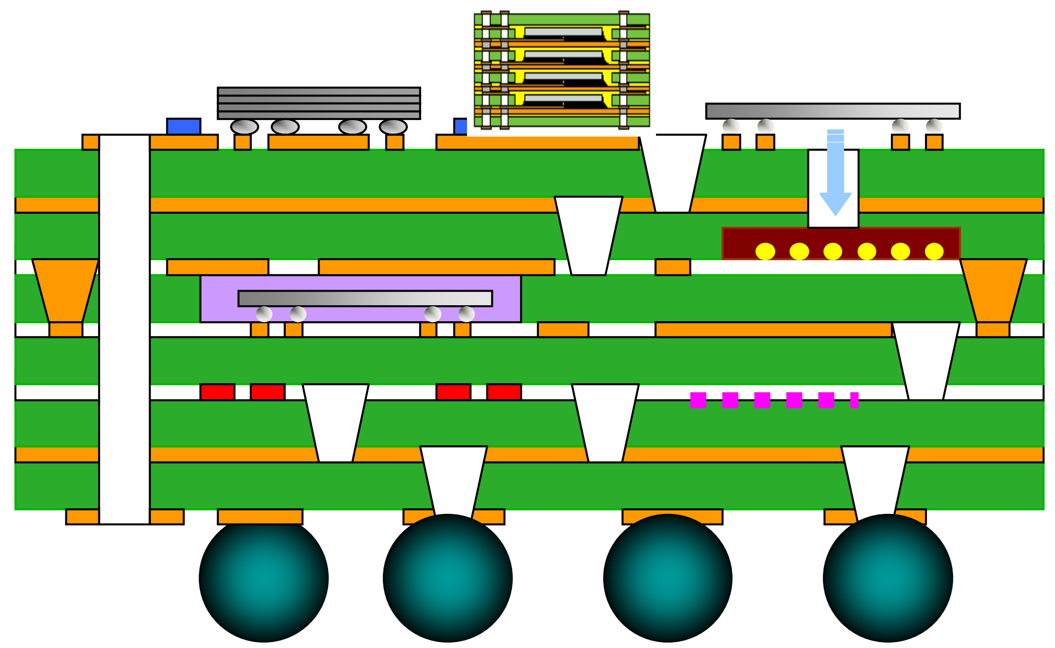
Outer Interface Circuit
- Bluetooth, USB interface
- MP3, GPS interface
- Memory Card interface

Power Supply Circuit
- Smaller Size

Source: H.Ueda JEITA

SiP: Multi-level System Integration

SiP may include SoC and other traditional packages



Packages may include:

- ➔Sub-system packages
- ➔Stacked thin packages containing passives and active chips
- ➔Mechanical, optical and other non electrical functions
- ➔Complete systems or sub-systems with embedded components
- ➔Bare die

ITRS

Source: Fraunhofer IZM

Categories of SiP

<table>
<tr><td colspan="2">Horizontal Placement</td><td>Wire Bonding Type
Flip Chip Type</td></tr>
<tr><td rowspan="2">Stacked Structure</td><td>Interposer Type</td><td>Wire Bonding Type
Wire Bonding + Flip Chip Type
Flip Chip Type</td></tr>
<tr><td>Interposer-less Type</td><td>Terminal Through Via Type</td></tr>
<tr><td colspan="2">Embedded Structure</td><td>Chip (WLP) Embedded + Chip on Surface Type
3D Chip Embedded Type
WLP Embedded + Chip on Surface Type</td></tr>
</table>

Source: 20030710 K. Nishi, Hitachi, JEITA, Revised by H. Utsunomiya

Assembly and Packaging

There are significant revisions to tables

- Difficult Challenges
  - Pb free transition presents cost, reliability and process compatibility problems that are not resolved
  - A new generation of DFM and DFT will be required for complex SiP and SoC packaging
  - Stress induced changes in electrical properties for very thin die
  - Reliability for through wafer vias and die layer bonding
  - Warpage control for stacked die
  - Interconnect for nano-scale structures
  - Self assembly for very small die

Significant Table Revisions
Continued

- Many new Materials are required for the emerging package requirements:
  - Improved thermal conductivity for dielectrics and materials interfaces
  - Molding compounds compatible with copper and other new materials
  - Improved resistance to electromigration as temperature and current density continue to rise
  - Dielectrics with improved fracture toughness and interfacial adhesion
  - Green materials that meet regulatory, cost and reliability requirements

New Materials

Most, if not all, packaging materials will change within this decade

- Cu interconnect
- Ultra Low k dielectrics
- High k dielectrics
- Organic semiconductors
- Green Materials
  - Pb free
  - Halogen free
  - other

Assembly and Packaging
Technical working Group 2006 Focus

We are giving special focus in 2006 to preparation of a white paper titled:

"The next step in Assembly and Packaging: Systems Level Integration"

Objectives of this white paper

- Catalyze additional SiP chapter for 2007 ITRS issue
- Identify needs and gaps
- Identify new technology trends for future SiP

“The next step in Assembly and Packaging: Systems Level Integration”

Introduction & Motivation

- The basic elements generic to all SiP System level integration applications will be defined.
- Examples will be used from various application areas to show how the basic elements are incorporated into these applications.

Critical updates to selected sections in preparation for 2007

- Expansion of the section on handling and packaging of extremely thin die
- Expanded treatment of sensors in cooperation with iNEMI

3D Packaging increases Performance Density and enables system level integration

Thank You