

2006 updates to the Lithography chapter of the ITRS

Lithography International Technology
Working Group
July 2006



Lithography ITWG chair persons and co-chair persons for 2006

Region	Chair person	Co-Chair person
Taiwan	Burn J. Lin	G. C. Hung
Japan	Isamu Hanyu	Iwao Higashikawa
Korea	Han-Ku Cho	
Europe	Mauro Vasconi	Jan-Willem Gemmink
USA	Scott Hector	Maureen Hanratty
USA (2006)	Mike Lercel	Gene Fuller



Summary of 2005 Lithography Chapter Updates

- CD control and linewidth roughness (LWR)
 - Increased CD tolerance to $\pm 12\%$ for MPU gates
 - CD control for MPU gates is still red (red starts at $< 4 \text{ nm } 3\sigma$)
 - Increased printed CD in resist to $\sim 1.7 \times$ physical gate length
 - Updated definition of and values for LWR
- Significantly tightened overlay tolerances from 35% to 20% of flash/DRAM $\frac{1}{2}$ pitch
- Updated potential solutions
- Added table describing imprint template requirements
- Requirements for exposure tool fluids and environment added to Yield chapter
- Increased detail on difficult challenges with immersion and EUV
- Added table showing progression of low k_1 methods and lithography friendly design
- DFM description to complement content in Design chapter
- Automatic process control (APC) detail
- Cost of ownership factors and throughput factors described in text



2005 ITRS lithography requirements

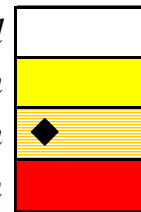
<i>Year of Production</i>	2005	2007	2010	2013	2016	2019
DRAM ½ Pitch (nm) (contacted)	80	65	45	32	22	16
Flash ½ Pitch (nm) (Un-contacted Poly)	76	64	57	51	45	40
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	90	68	45	32	23	16
→ MPU gate length in resist (nm)	54	42	30	21	15	11
MPU Physical Gate Length (nm)	32	25	18	13	9	7
Contact diameter in resist (nm)	111	84	56	39	28	20
Contact diameter after etch (nm)	101	77	51	36	25	18
→ Gate CD control (3 sigma) (nm)	3.3	2.6	1.9	1.3	0.9	0.7
→ Overlay [Å]	15	11	8.0	5.7	4.0	2.8
Mask CD uniformity (nm, 3 sigma) isolated lines (MPU gates), binary mask [H]	3.8	2.6	1.3	1.0	0.7	0.5
→ Line Width Roughness (nm, 3 sigma) <8% of CD *****	3.6	2.8	2	1.4	1	0.8

Manufacturable solutions exist, and are being optimized

Manufacturable solutions are known

Interim solutions are known

Manufacturable solutions are NOT known

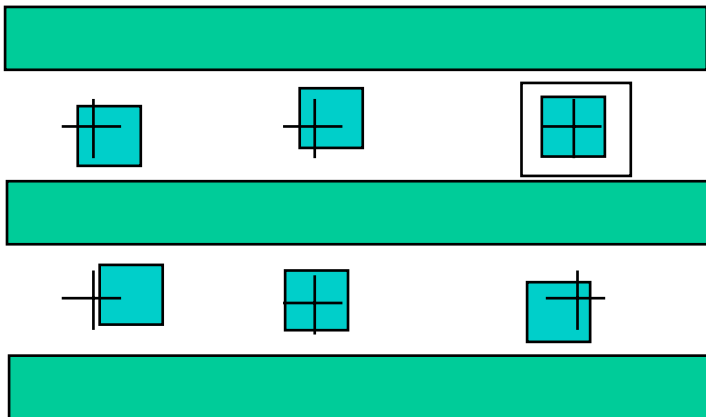


Proposal only; Not for publication



Overlay

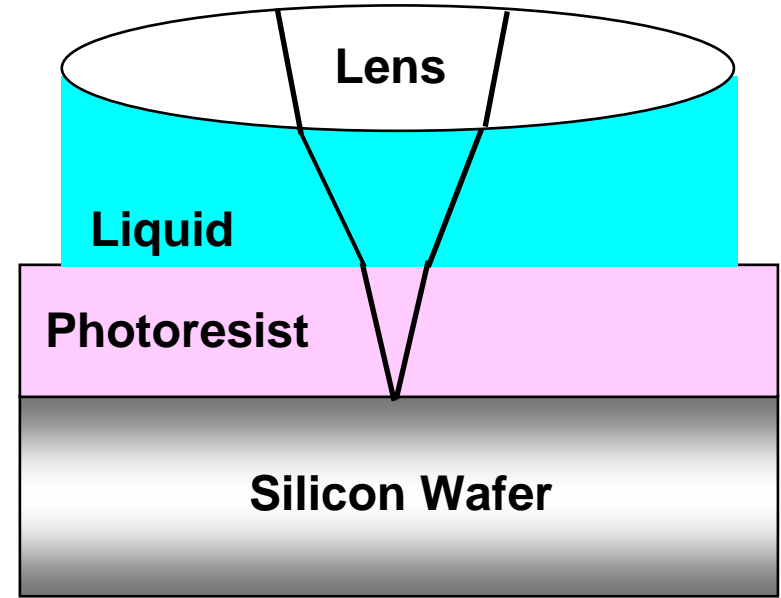
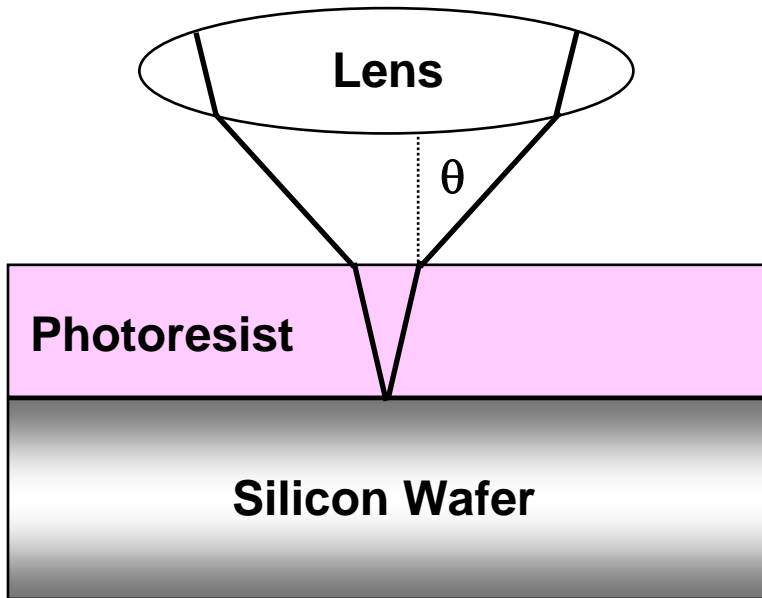
- Change from 35% to 20% of DRAM half-pitch
 - Reflects increasing emphasis placed on overlay to achieve device scaling in both Flash/DRAM and logic
- Overlay now red in 2008 (10nm)
 - Mask image placement also red in 2008 (6.1nm)



Resolution improvement by immersion

$$\begin{aligned}
 HP_{MIN,DRY} &= \frac{1}{4} \frac{\lambda_{RESIST}}{\sin \alpha_{RESIST}} \\
 &= \frac{1}{4} \frac{\lambda_{AIR} / n_{RESIST}}{\sin \theta / n_{RESIST}} \\
 &= \frac{1}{4} \frac{\lambda_{AIR}}{\sin \theta}
 \end{aligned}$$

$$\begin{aligned}
 HP_{MIN,WET} &= \frac{1}{4} \frac{\lambda_{RESIST}}{\sin \beta_{RESIST}} \\
 &= \frac{1}{4} \frac{\lambda_{AIR} / n_{RESIST}}{n_{LIQUID} \sin \theta / n_{RESIST}} \\
 &= \frac{1}{4} \frac{\lambda_{AIR}}{\sin \theta} / n_{LIQUID}
 \end{aligned}$$



$$n_{water} = 1.44$$



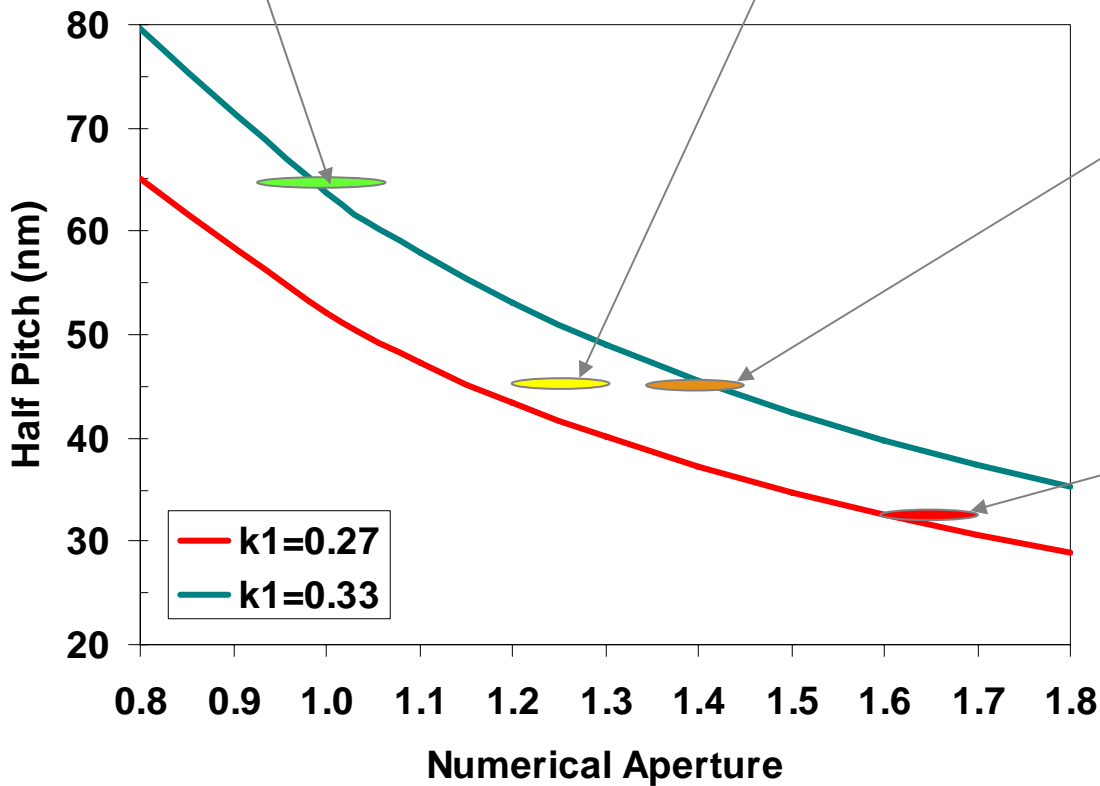
Immersion Generations

Generation 1: 65nm hp
0.93 ~ 1.07 NA, water

Generation 2a: 45nm hp
1.2 ~ 1.3 NA, water

Generation 2b: 45nm hp
1.35 ~ 1.45 NA,
Generation 2 fluid

Generation 3
32nm hp, 1.6 ~ 1.7 NA,
Generation 3 fluid,
High index lens material,
High index resist

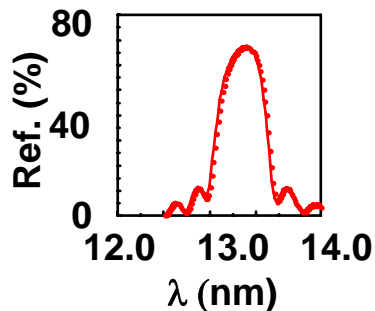


Extreme Ultraviolet Lithography (EUV)

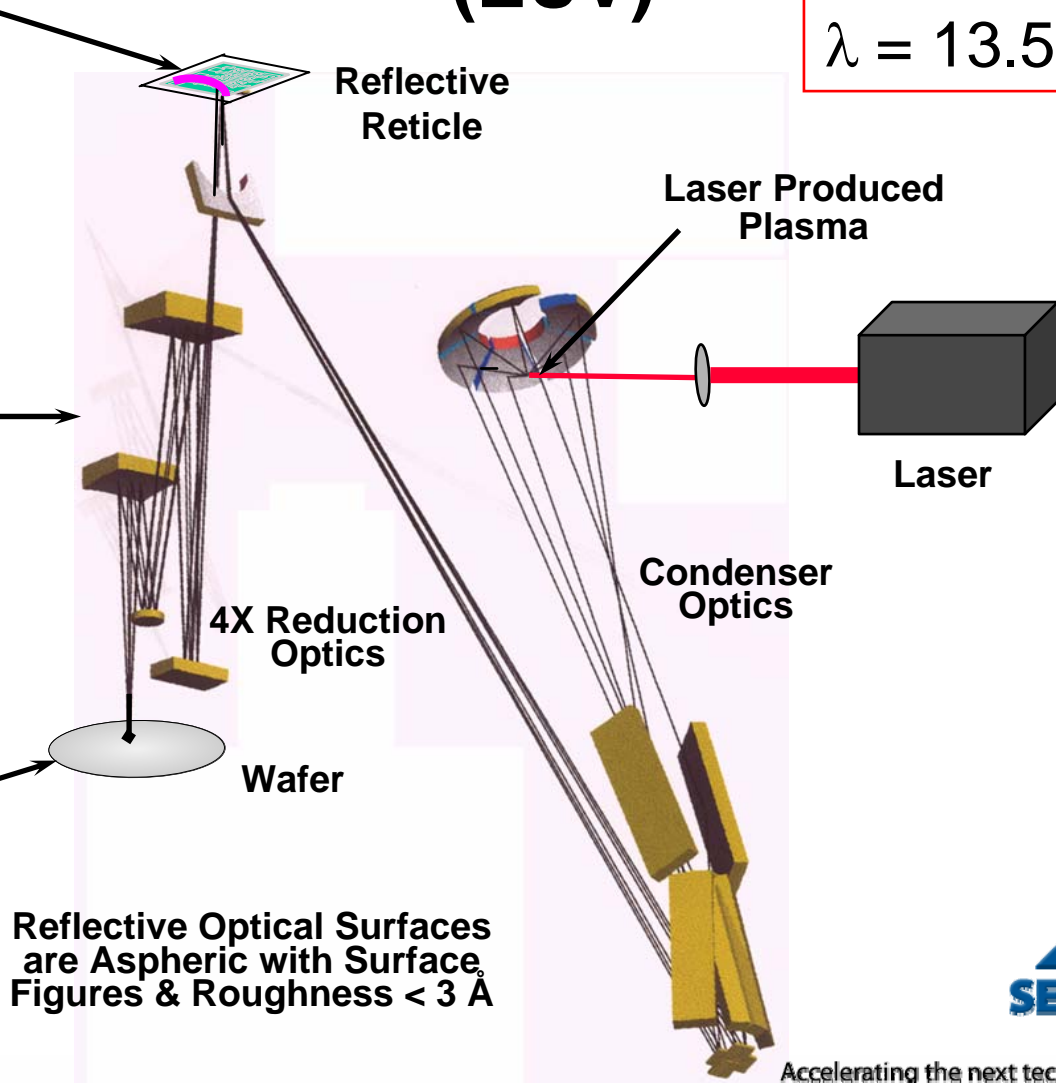
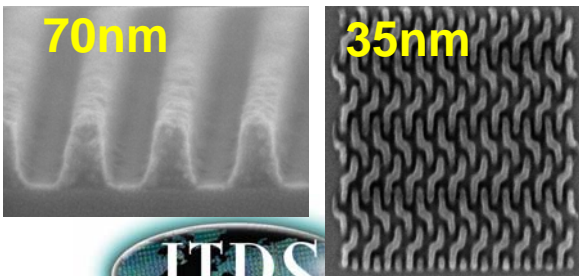
$\lambda = 13.5 \text{ nm}$

Ring Field Illumination
Scanning mask and wafer stages
Flat, square mask with multilayers

All optics surfaces coated with multilayer reflectors (40 - 80 layer pairs, each layer approx $\lambda/4$ thick, Control $\sim 0.1 \text{ \AA}$)



EUV imaging with ultrathin resist (UTR)



Reflective Optical Surfaces are Aspheric with Surface Figures & Roughness $< 3 \text{ \AA}$



Accelerating the next technology revolution.



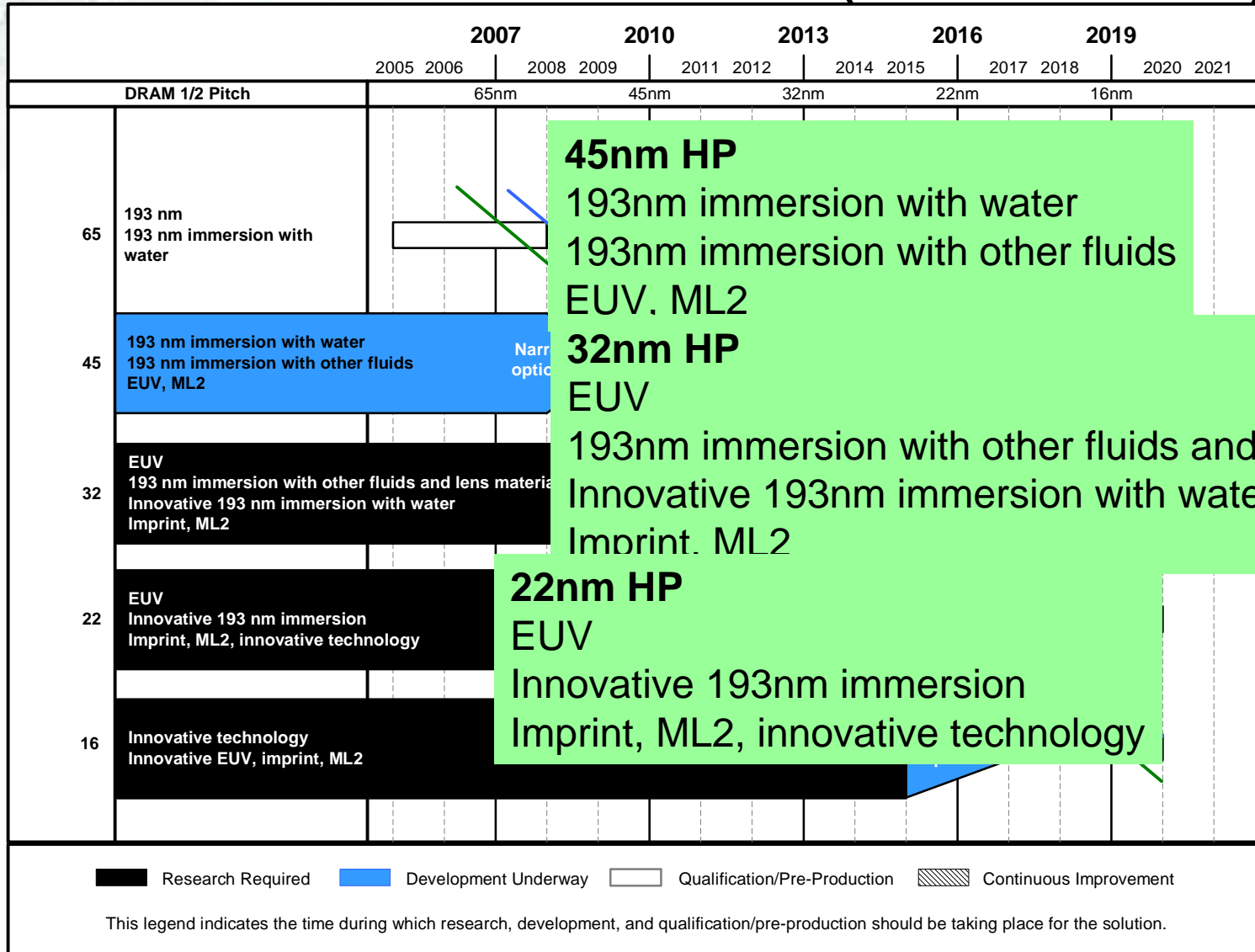
Significant changes to potential solutions in 2005

- 193nm immersion with water and other fluids expected to be primary technology through 45nm and perhaps 32nm $\frac{1}{2}$ pitch with new lens materials
- 157nm no longer seen as potential solution
- EUV remains most likely next generation lithography (NGL) with possible use starting at 45nm $\frac{1}{2}$ pitch and primary solution for 32nm and 22nm $\frac{1}{2}$ pitch
- Electron projection and proximity electron not as probable as in 2004
- Maskless lithography remains as potential solution starting at 45nm $\frac{1}{2}$ pitch
- Imprint extended to cover 32nm through 16nm $\frac{1}{2}$ pitch

Proposal only; Not for publication



Potential Solutions (2005 ITRS)



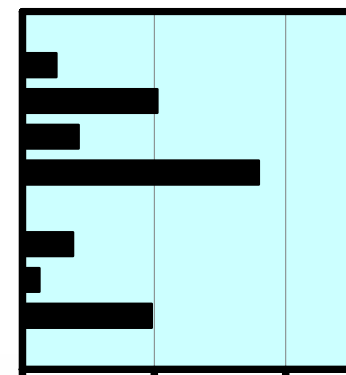
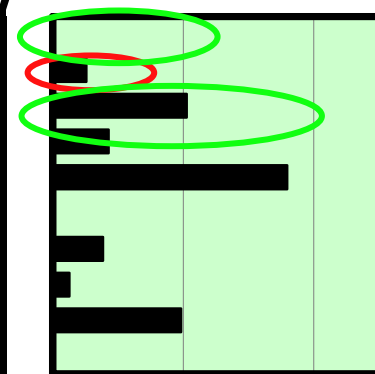
2012 Lithography Preferences

2006 SEMATECH Litho Forum survey results



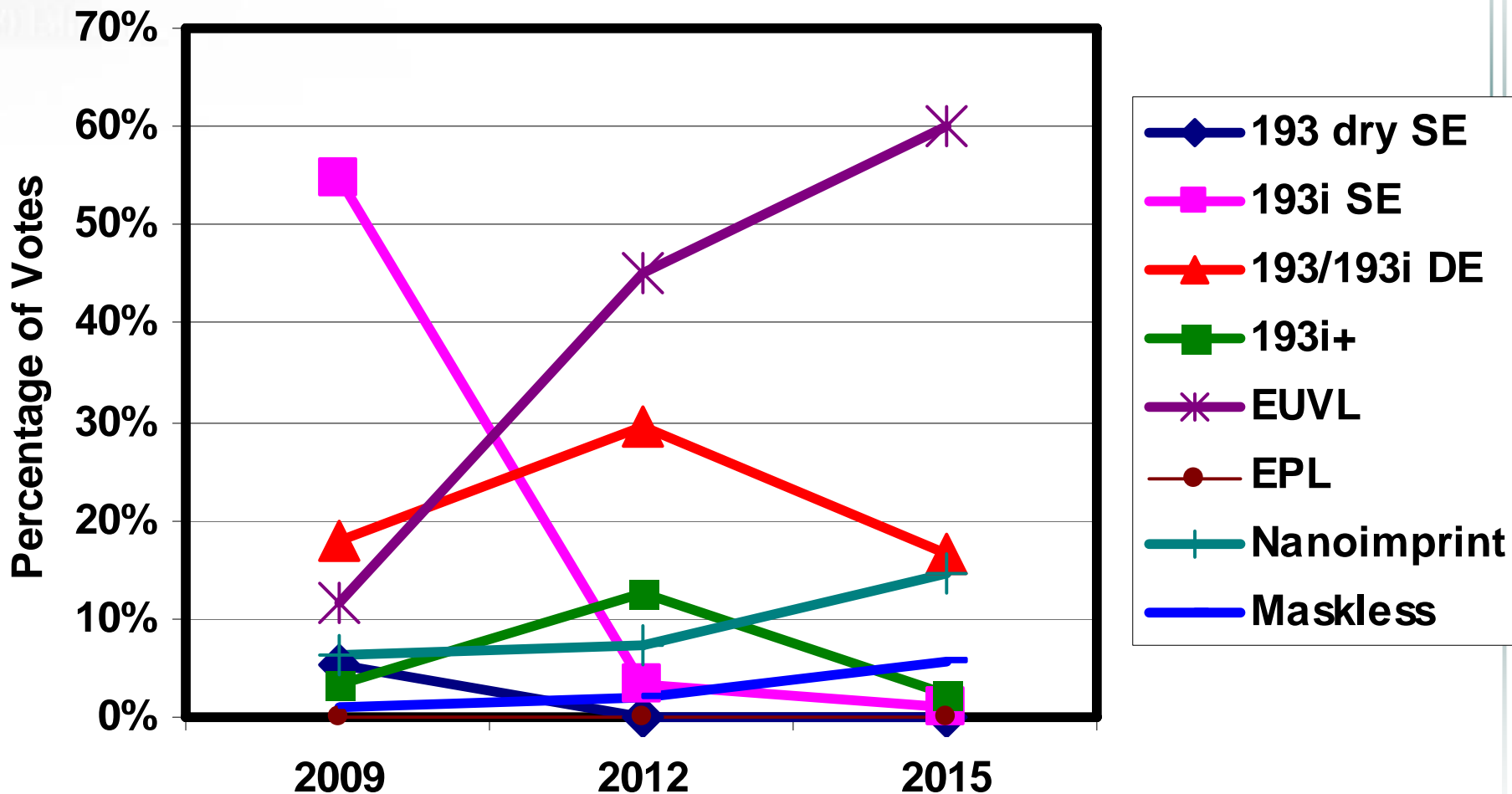
Primary lithography technology employed or supported for leading-edge mfg. in 2012

		ASIC + Mix + Foundry	MPU	Memory	Exp Tool	Mask Design + Fab	Resist / Process	Consortia	Research + Academia	Other
Gate	193 dry SE									
	193i SE									
	193/193i DE	X	X							
	193i+					X	X			
	EUVL	X	X	X	X	X	X	X	X	X
	EPL									
	Nanoimprint									
	Maskless									
	N/A			X					X	X
	Other									
Contact	193 dry SE									
	193i SE			X						
	193/193i DE	X	X							
	193i+					X				
	EUVL	X	X	X	X	X	X	X	X	X
	EPL									
	Nanoimprint									
	Maskless									
	N/A			X					X	X
	Other									



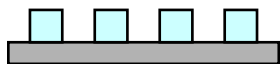
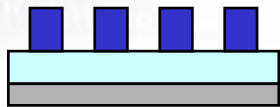
Preferred Technology by Year

2006 SEMATECH Litho Forum survey results

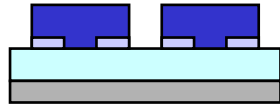
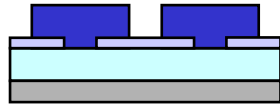
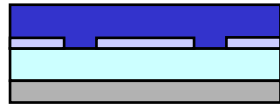
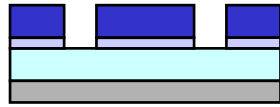





Double Patterning (DE/DE)

**Conventional
Single Expose**



**Double Exp/
Double Etch**



-  Resist
-  Hard Mask
-  Under Layer
-  Substrate

Expose #1

Hard Mask
Etch

Coat #2

Expose #2

Etch Hard Mask

Etch

Double Patterning Challenges

- Resist / Process
- Overlay
- DFM: DE split
CAD
- COO

Variety of application
dependent processes

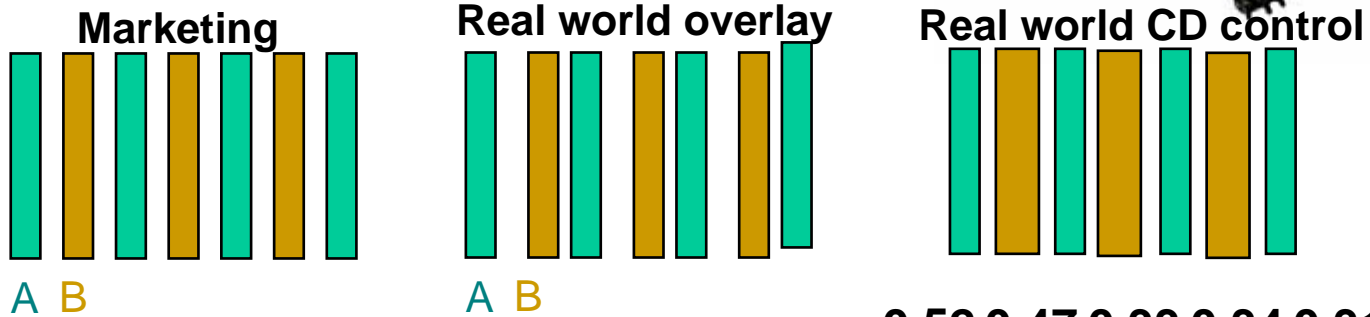
From Andrew Grenville.



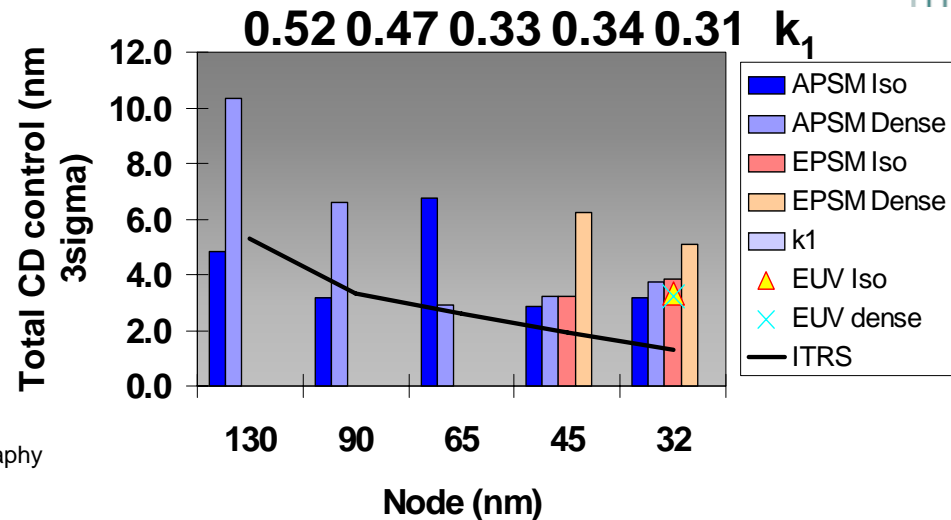
Proposed 2006 Updates



- Double patterning 193nm lithography as a potential solution
 - Add set of difficult challenges
 - New table entries for double patterning reflecting new challenges of overlay and CD control



- CD uniformity
 - Accurate definition matching with design and device groups
 - Update achievable CD uniformity (from 2003 study)



Scott D. Hector, Sergei Postnikov and Jonathan Cobb, Optical Microlithography XVII, SPIE Proceedings Volume 5377, 555-70, 2004.



Basic CoO Model - Lithography

$$C_{gwle} = \frac{(C_e + C_l + C_f + C_c)}{(T U Y_p)} + \frac{C_m}{N_{wm}}$$

C_{gwle} = cost per good wafer level exposed

C_e = yearly cost of expose, coat, and develop equipment including capital depreciation and maintenance

C_l = yearly cost of labor to operate equipment

C_f = yearly cost of cleanroom space

C_c = yearly cost of consumables including resist, BARC, developer, solvents

T = raw throughput (wafers/year)

U = overall operating utilization (% of total time)

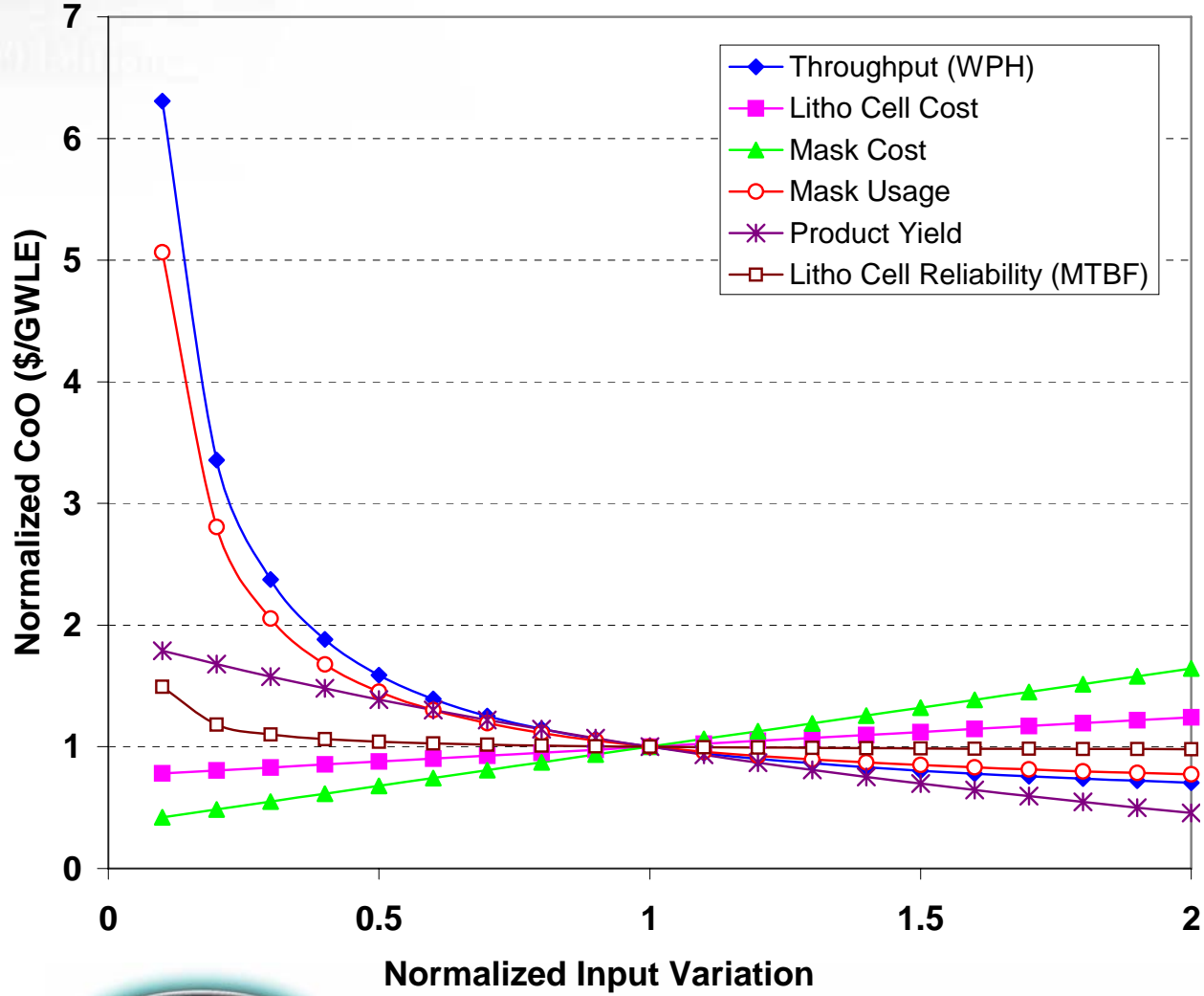
Y_p = process yield of step

C_m = cost of mask

N_{wm} = number of wafers exposed per mask

Cost-of-Ownership

CoO Sensitivity (Impact to \$/GWLE to input parameter)



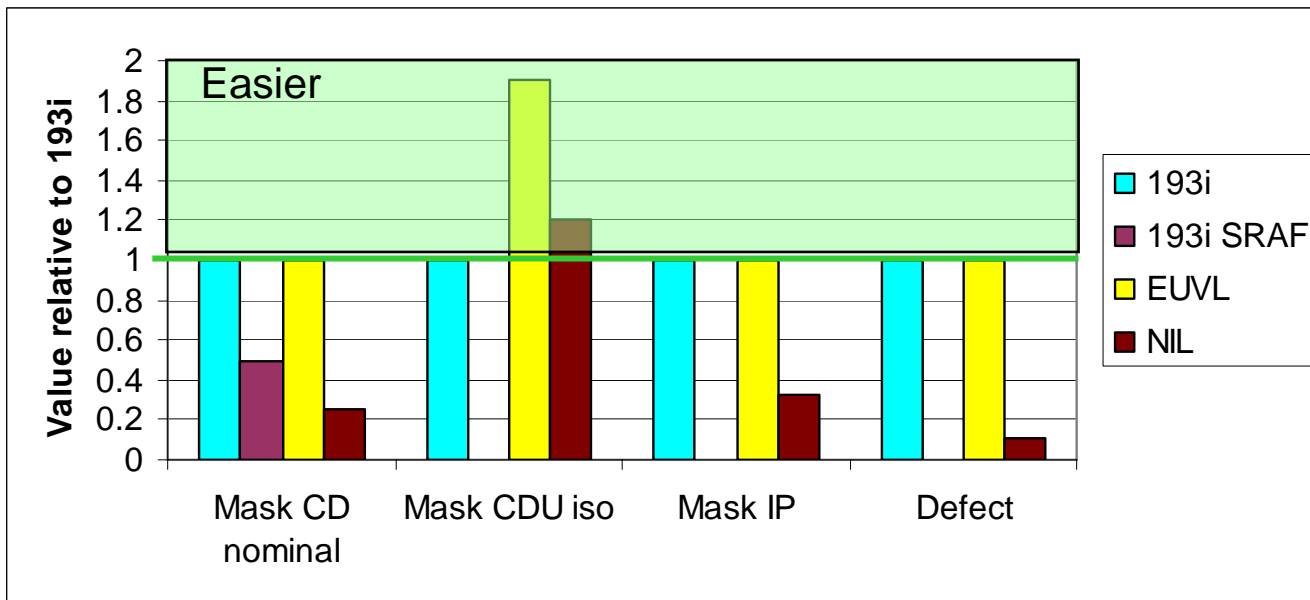
Litho CoO model provided in 2005 ITRS Litho chapter. Goal is to provide framework for individual companies to assess CoO issues

Significant CoO impacts with very low system throughput and low mask usage



Nanoimprint Template Requirements

- Added table to address template requirements
 - 1X patterning dimensions
 - Template specific requirements
 - Etch depth and uniformity
 - Rounding of top and bottom of features
 - Defect sizes affecting CD (x/y and z)
 - Surface roughness (bottom and sidewall)



Mask
parameters
relative to
193i



Summary

- 193nm immersion seen as the most promising candidate for 45nm half-pitch patterning
- EUVL remains the most promising candidate for 32nm half-pitch patterning with 193nm double exposure and 193nm high-index materials options as other candidates
 - Significant challenges remain in developing EUVL, but EUVL is seen as most extendible technology
 - Maskless lithography and nanoimprint are seen as possible technologies
- Increasing interest in double patterning techniques
 - Critical challenges remain in cost control and infrastructure readiness
- CD uniformity of $\pm 12\%$ adopted but still difficult to achieve
- Device scaling limitations drive more stringent overlay tolerances for most technologies



Scaling relations for Table 77 and 79

Item	Value (in nm) where becomes:	Yellow	Red
CD = Physical gate width = $0.4 \times \text{DRAM } \frac{1}{2} \text{ pitch}$		40	20
Overlay = $20\% \times \text{DRAM } \frac{1}{2} \text{ pitch}$		20	11
Minimum linewidth in resist = $1.6818 \times \text{physical gate}$		50	25
Contact size after etch = $1.125 \times \frac{1}{2} \text{ pitch}$		85	60
Contact in resist = $1.1 \times \text{contact after etch}$		75	50
CD control for DRAM = $13.5\% \times \text{sqrt}(0.75) \times \text{DRAM } \frac{1}{2} \text{ pitch}$		7	4
CD control for MPU/ASIC =		7	4
$12\% \times \text{sqrt}(0.75) \times \text{MPU/ASIC M1 contacted } \frac{1}{2} \text{ pitch}$			
Mask nominal image size = MAG \times resist linewidth		200	130
SRAF feature is $\frac{1}{2}$ of mask nominal image		130	100
Mask Min. Primary Feature Size =		200	130
$0.7 \times \text{Mask nominal image size}$			
Mask CD control = $\text{CD} \times \text{MAG} \times \text{sqrt}(0.75) \times 4\% / \text{MEEF}$		8	5
Placement = $\text{Overlay} \times \text{MAG} \times 15\%$		14	10
Defect size = $\text{DRAM } \frac{1}{2} \text{ Pitch} \times \text{MAG} / 5$		80	60
Linearity = $3.8\% \times \text{DRAM } \frac{1}{2} \text{ pitch} \times \text{MAG}$		15	10
CD mean-to-target = $2\% \times \text{DRAM } \frac{1}{2} \text{ pitch} \times \text{MAG}$		7	4
Absorber LER = $\text{Min. CD} \times \text{MAG} \times 3\%$		7	4
Blank flatness $\propto 1/\text{NA}^2$ (250nm in 2007)		250	150
Data volume = $2 \times \text{increase} / \text{node}$ (260 GB in 2004)		260	5000 GB

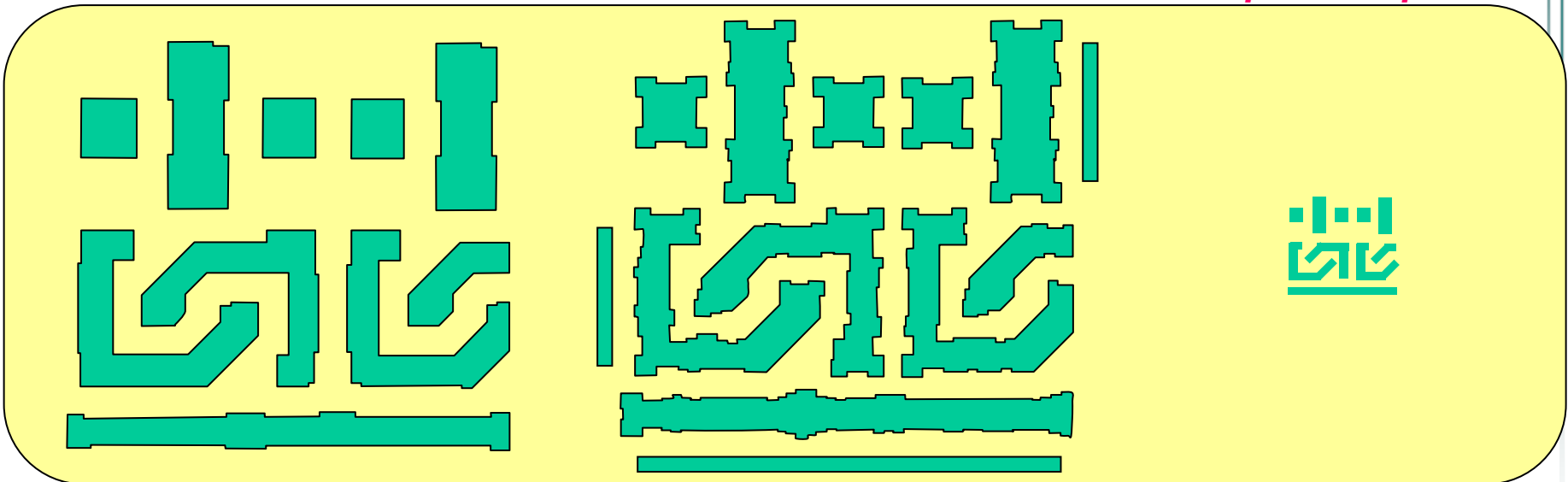
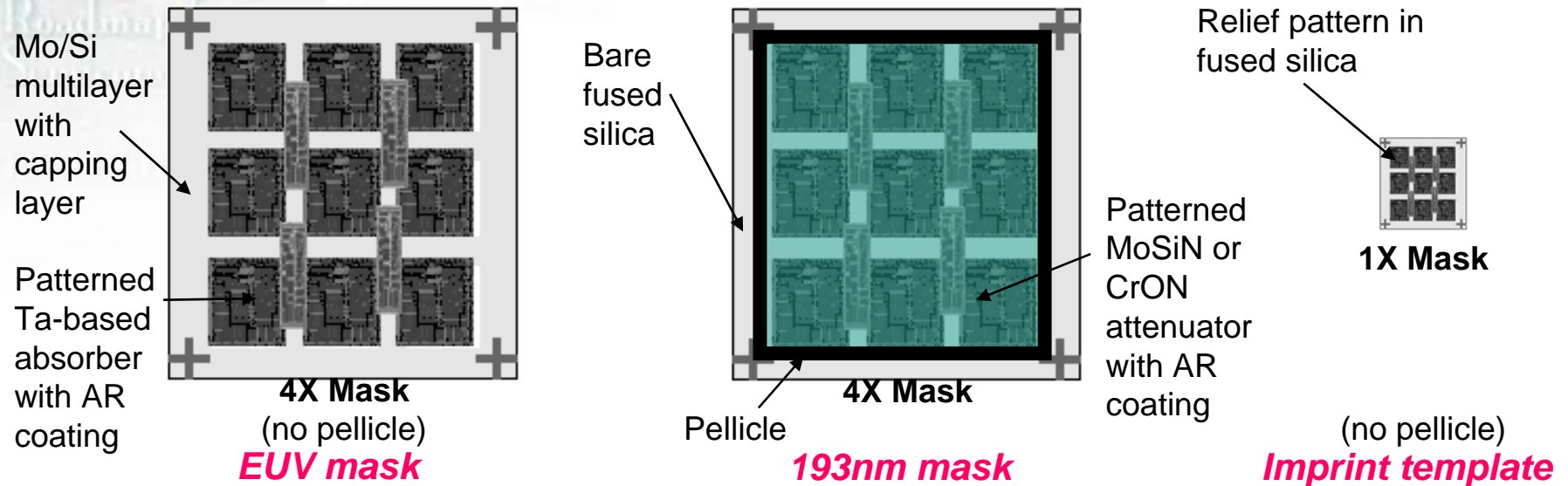


Criteria for potential solutions

- All infrastructure (masks, tools, resist,...) needs to be in place to meet the ramp for the specified node
- Technology must be planned to be used by IC makers in at least two geographical regions
 - For N+3 and later nodes with black coloring, the requirement to have more than one region support is not applicable
- Technology should be targeting leading edge critical layer needs
- Consideration (not a requirement): ≥ 100 tools worldwide over the life of that tool generation (not for each node)



Comparison of EUV, 193nm and imprint masks



2.7 nm 3σ

1.3 nm 3σ

1.7 nm 3σ