2006 ITRS Test TWG: Optimizing Test Cost

Mike Rodgers
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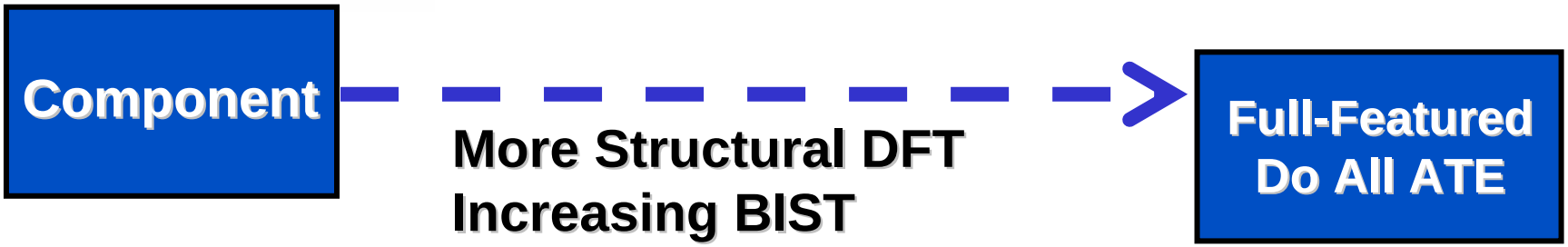
San Francisco, CA

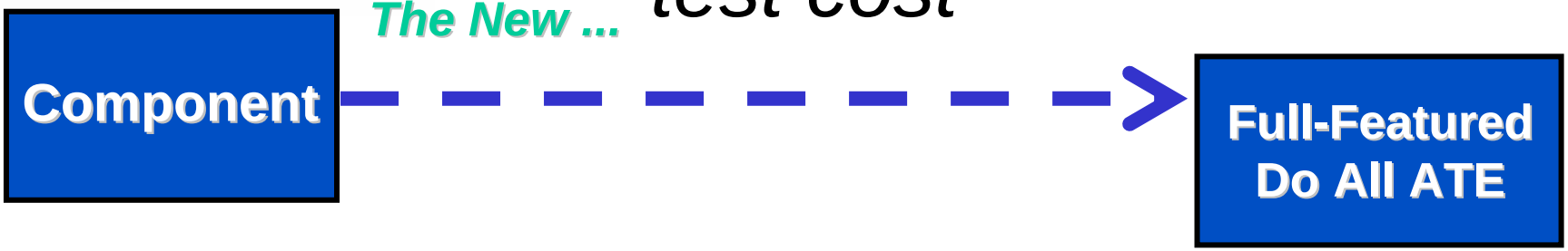
Looking Back:
The New Manufacturing Test paradigms:
Deliver Gbit+/s performance at commodity test cost



More Structural DFT
Increasing BIST
Advanced Fault Models
More ATPG, less manual test

Commodity cost
Gbit+/s I/O
Short product cycle
More feature integration

The New Manufacturing Test paradigms: *Deliver Gbit+/s performance at commodity test cost*



Continued use for silicon validation
Expanded use for mfg test verification
Reduced use for HVM mfg test

The New Manufacturing Test paradigms: *Deliver Gbit+/s performance at commodity test cost*

Fewer channels than device
Lower performance pin electronics
Re-use across technology generations
Standardized test software across vendors
Test tooling for power delivery

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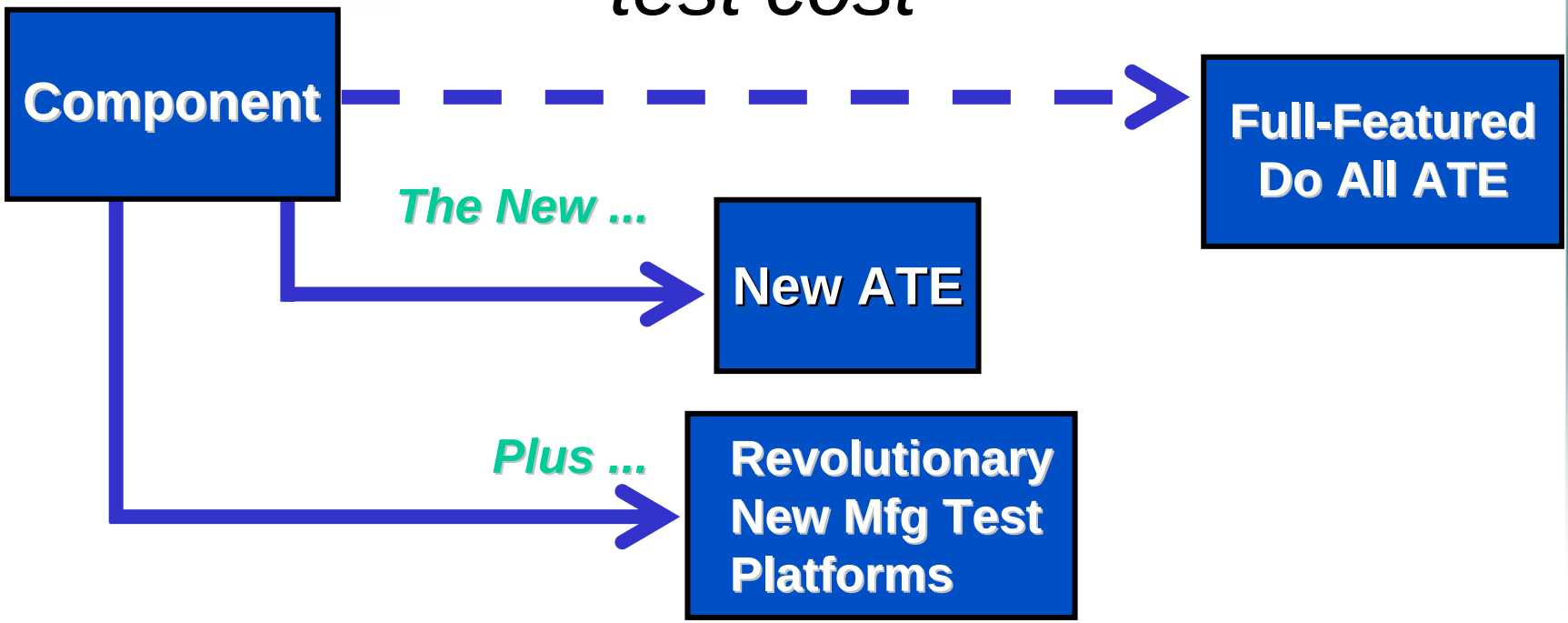


Application platform based testers (e.g., PC, appliance)
Test-During-Burn-in (substantial)
New test integration paradigms
- **Wafer Test-Burn-in combination**
- **Dedicated I/O testers**

2005 ITRS Test Chapter Revision

- Trends described in 2001 have held true
  - High speed serial I/O appeared across market segments
  - SOC and SIP occurring , 3D Pkg on the horizon
  - Low cost, flexible (open arch) platforms emerging
  - Increasing integration of analog/RF
- 2003 Test Chapter focused on key challenges
  - Less emphasis on evolutionary trending
  - Increased effort to identify, define, & discuss the key test challenges

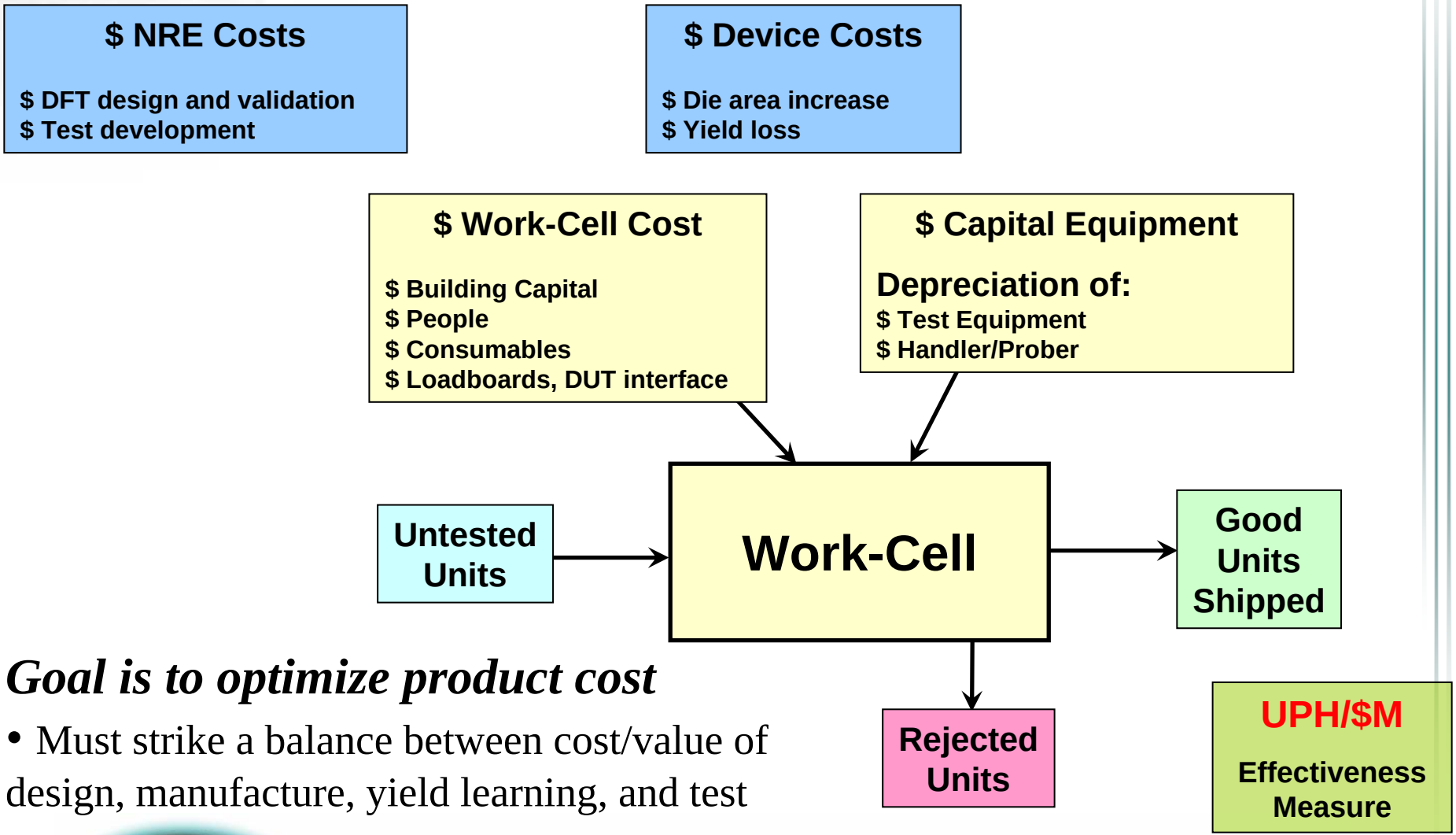
2005 Roadmap Update

- 2005 Revision
  - 1st major re-org of the Test Chapter in several years
    - Consolidation of logic ATE/product tables
    - Challenges split into Challenges & (new) Key Test Drivers
  - Reliability Screens update
  - Expanded the new “Cost of Test” section
  - Addition of test sockets and test interface boards
  - New section on RF pulled from AMS
  - 2006 revision will update values within current tables
  - 2006 TWG & WGs will plan ’07 structural changes

Key Test Drivers

- Device Trends
  - Device interface bandwidth (data rate & pin count, *to several Gb/s*)
  - Increasing integration (SOC, MCP, SIP, *3D pkg*)
  - Package form factor & electrical / mechanical characteristics
  - Device power complexity and management modes
- Integration of Emerging Technologies
  - RF, Analog, Optical, MEMs, in platforms such as displays, cellular, etc
- Increasing Test Process Complexity
  - To enable device customization, optimize test flow
  - To provide better and faster manufacturing feedback
- Bottom Line Constraint is Test Cost
  - Boundary conditions: Affordability and maximum allowable DPM

The Overall Cost of Test



Goal is to optimize product cost

- Must strike a balance between cost/value of design, manufacture, yield learning, and test

Key Test Challenges & Opportunities

- Test for Yield Learning
  - Critically essential, not a nice to have, driver: limits of physical FA
- Screening for reliability
  - Increasing challenges for effective burn-in, Iddq, Vstress
  - Rel concerns increasing at 45nm and beyond
- Increasing systemic defects
  - Testing for local non-uniformities not just *Hard Defects*
    - Symptoms of line width control, dopant variation, other systemics
- Containing and optimizing total product test cost
  - Improving/ maintaining test efficiency
    - Keeping up with complexity: Multi-core, 3D,
    - Managing test data volume: ATPG compression, parallelism
    - Barriers on increasing parallelism for memory test not as bad as predicted

Yield Learning, FA, and Diagnosis

- Physical FA hitting the wall:
  - Significant tpt, technology, cost, & results barriers

- Enhanced automated software diagnostic capabilities to improve physical failure analysis ROI
  - Characterization capabilities must ID, locate, and distinguish defect types
  - Increased accuracy and throughput (days to hours)
  - Failure analysis methods for analog devices must be developed

- DFT is essential to localize failures
  - Improve efficiency, reduce design complexities associated with test

- Defect types and behavior will continue to evolve with advances in fabrication process technology
  - Research in existing and novel fault models to address emerging defects required

Reliability Screens Run Out of Gas

- Critical: new techniques for t>0 defects
  - Burn-in methods limited by thermal runaway
  - Lowered use voltages limits voltage stress opportunity
  - Iddq signal to noise degrading rapidly
- New materials and devices
  - Integration increasing rel risks
  - Rate of introduction increasing: Cu, low k, high k,
    - Critical interactions of new materials increasing
    - More integration of silicon systems (MEMs, optical, etc)
    - More device permutations even in vanilla CMOS
  - Increasing mechanical and thermal sensitivities
- Rel concerns at 45nm and beyond increasing
  - When does “correction” become mainstream?

Test Cost vs Capability Treadmill

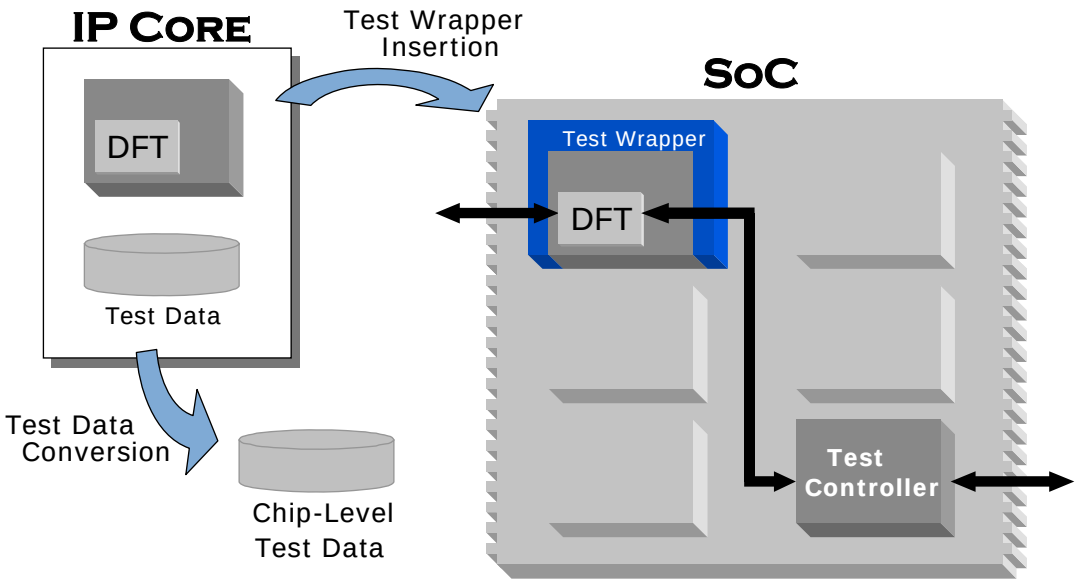
- Some critical questions:
  - Flattening of test parallelism further increases
  - How slow can a tester go?
- DFT and test methods development is effectively constraining logic test requirements
- Capability driven investment into equipment for testing Analog, RF, and SerDes circuits
- MCP, SiP, and SoC drive convergence of leading edge, high density logic with flash, DRAM, SRAM, analog, RF, and SerDes
- The move toward open architecture is intended to make it easier (and cheaper) to implement incremental capability while enabling reuse

SOC, MCP, and SIP

- Customer requirements for form factor and power consumption are driving a significant increase in design integration levels
  - Test complexity will increase dramatically with the combination of different classes of circuits on single die or within a single package
  - Disciplined, structured DFT is a requirement to reduce test complexity
  - Increased focus on KGD & sub-assembly test driven by cost for SIP
  - Test thermal issues in 3D stacked dice products
  - Mems, opticals, and other emerging or newly integrated to SIP and silicon systems and devices
- SIP/MCP physical FA is much more difficult,
  - Test diagnostics will be more critical moving forward

Automated DFT Insertion

- Automation of test control integration and test scheduling
  - Insert test wrapper and test control circuits
  - Needs to extend to pkg integration increases (3D)



Configuration of Chip-Level Test Controller and Test Access Mechanism

Analog and RF

- Analog and RF circuits pervasive in digital world
  - Mobile/wireless as % of semis increasing
  - Circuit performance envelope increasing
- Test method innovation required
  - Primary test solutions continue to be based on expensive functional and parametric methods
  - Relatively little DFT has been deployed, and what does exist lacks industry momentum