Interconnect Working Group

2006 Update - Draft
12 July 2006
San Francisco

Christopher Case

ITWG Regional Chairs

Japan
- Tomoji Nakamura
- Hideki Shibata

US
- Christopher Case
- Robert Geffken

Taiwan
- Douglas CH Yu

Europe
- Hans-Joachim Barth
- Alexis Farcy

Korea
- Hyeon-Deok Lee
- Sibum Kim

Partial List of Contributors

- Robert Geffken
- Hans-Joachim Barth
- Alexis Farcy
- Harold Hosack
- Paul Feeney
- Ken Monnig
- Rick Reidy
- Mauro Kobrinsky
- Hideki Shibata
- Kazuyoshi Ueno
- Michele Stucchi
- Susan Vitkavage
- Eiichi Nishimura
- Mandeep Bamal
- Osamu Yamazaki
- Lucile Arnaud
- JD Luttmer
- Manfred Engelhardt
- Dirk Gravesteijn
- NS Nagaraj
- Mike Mills
- Skip Berry
- Gunther Schindler
- Chung-Liang Chang
- Tomoji Nakamura
- Greg Smith
- Detlef Weber
- Christopher Case

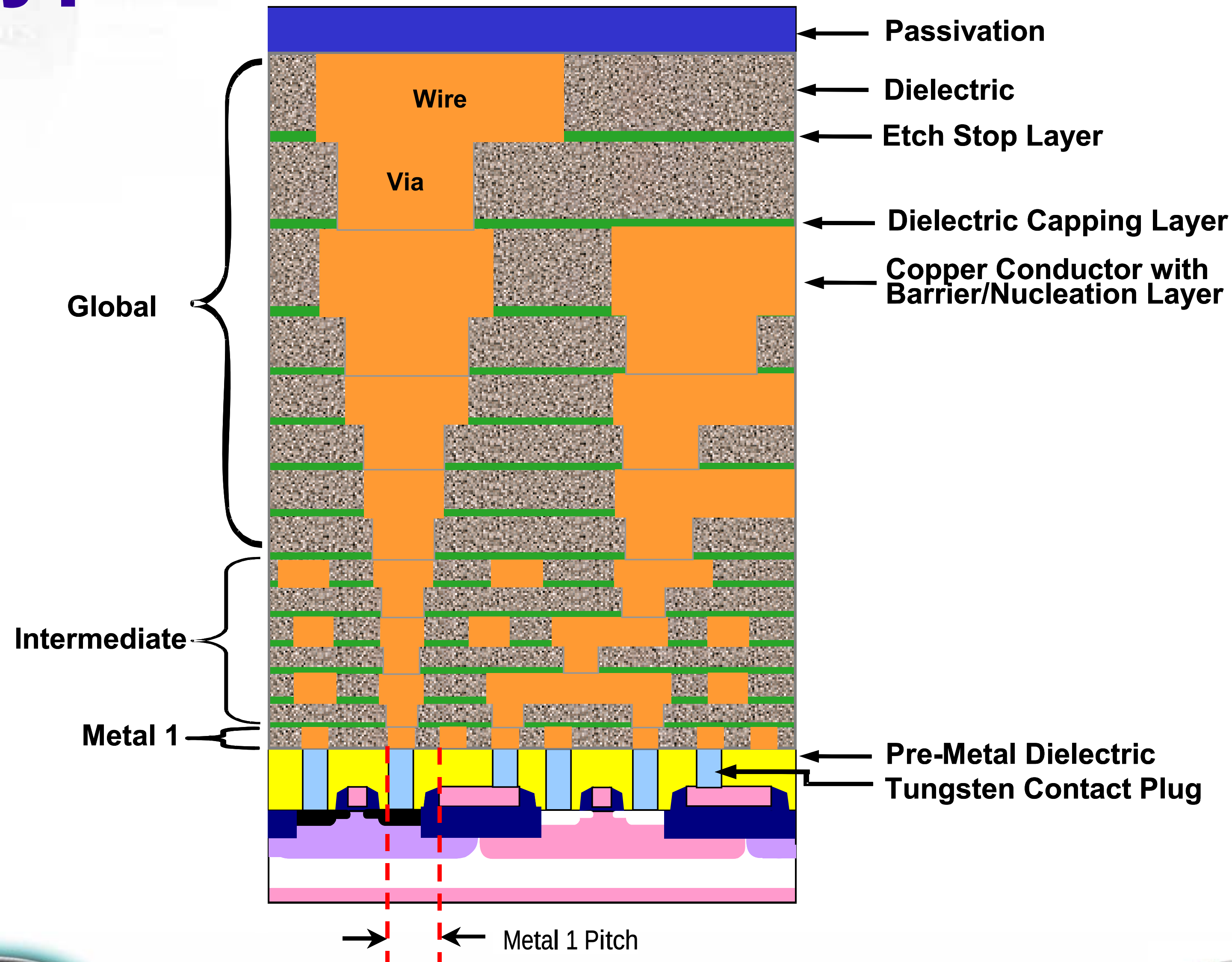
Agenda

- Scope and structure
- Technology requirements
- Difficult challenges
- Cu resistivity effects
- Energy and performance
- Low κ roadmap
- DRAM update
- Emerging interconnect
- Last words

Interconnect scope

- Conductors and dielectrics
  - Starts at conductor etch
  - Metal 1 through global levels
  - Includes the pre-metal dielectric (PMD)
- Associated planarization
- Necessary etch, strip and cleans
- Embedded passives
- Reliability and system and performance issues
- Ends at the top wiring bond pads
- Predominantly “needs” based, with some important exceptions (k and resistivity)

Typical MPU cross section



Technology Requirements

- Tables for HP MPU and ASIC plus DRAM
- Wiring levels including “optional levels”
- Reliability metrics
- Minimum wiring/via pitches by level
- Performance figure of merit and capacitance (NEW)
- Planarization requirements
- Conductor resistivity with and without scattering
- Barrier thickness
- Dielectric metrics including effective k (UPDATED)
- Crosstalk metric
- Metal 1 variability due to CD and scattering
- Power Index (NEW)

Difficult challenges

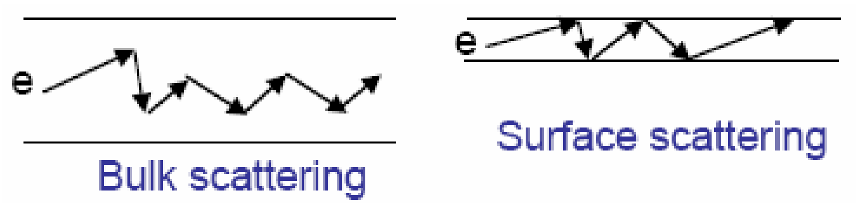
- *Identify solutions which address wiring scaling issues*
- Introduction of new materials to meet conductivity requirements and reduce the dielectric permittivity
- Engineering manufacturable interconnect structures compatible with new materials and processes

Whose linewidth is it anyway? The pitch for M1

- M1 and intermediate wire pitch for MPU is scaling rate at a rate faster than the 2004 ITRS
  - Continue to track and reference staggered contacted M1 half pitch as the driver for high performance MPU and ASIC products
  - 90 nm contacted M1 logic half pitch in 2005
  - 78 nm contacted M1 logic half pitch in 2006
  - scaling at x 0.75 / 2 years from 2005 to 2009
  - reverting to 3 years cycle in 2010 and beyond
  - DRAM on a 3 year cycle
- Metal 1 pitches converging between DRAM and logic

Size matters

- 2003 – the impending impact of Cu resistivity increases at reduced feature sizes (due to scattering) - first noted
- 2004 – metrics introduced to highlight the impact of width dependent scattering on the effective resistivity and impact on RC delay
  - Models have been refined to more accurately predict the resistivity due to changes in aspect ratio, shape and metal thickness
- 2006 - Metrics have been updated
- Adapt the same methodology for DRAM when Cu is introduced (2007)



Size matters

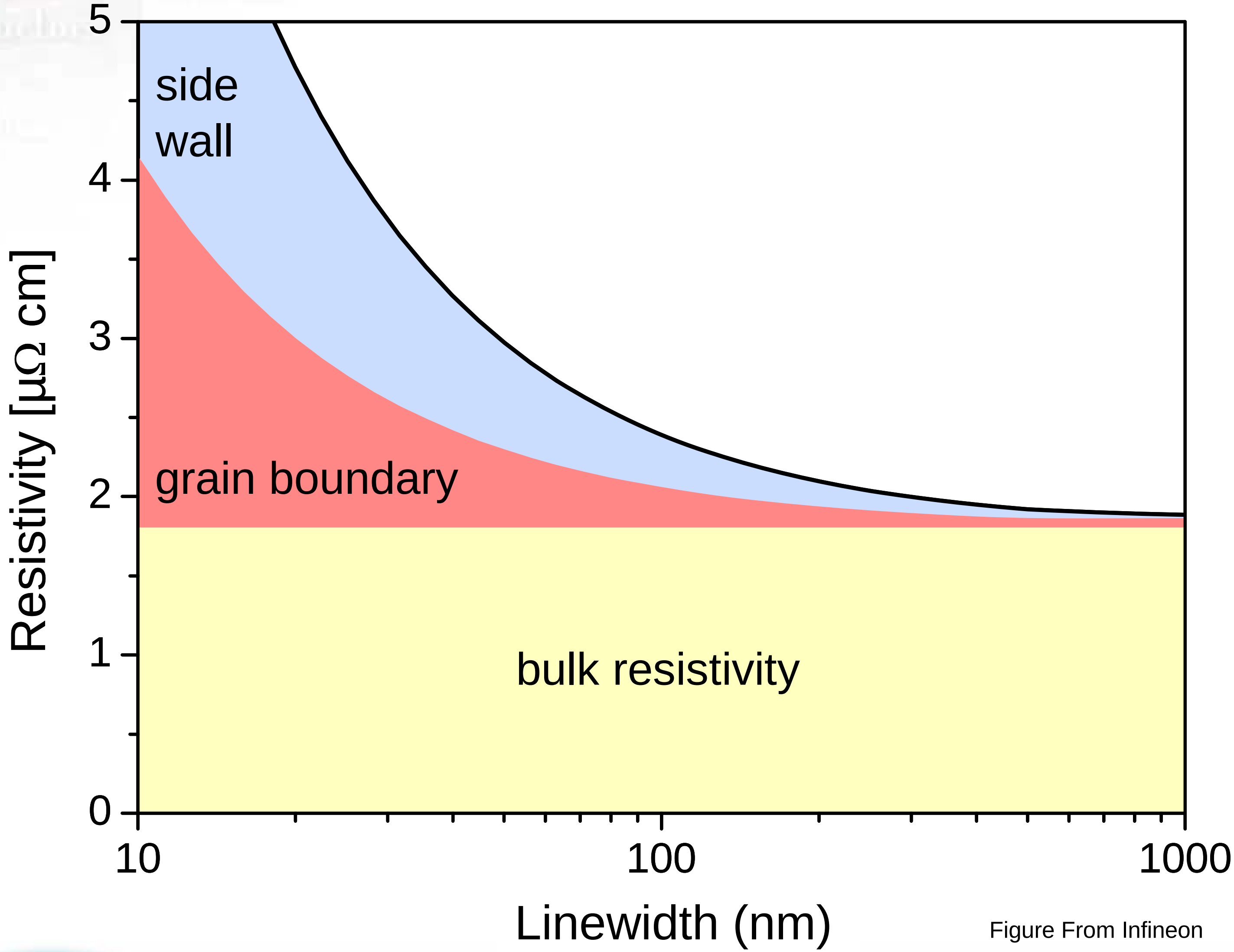


Figure From Infineon

Relative Delay

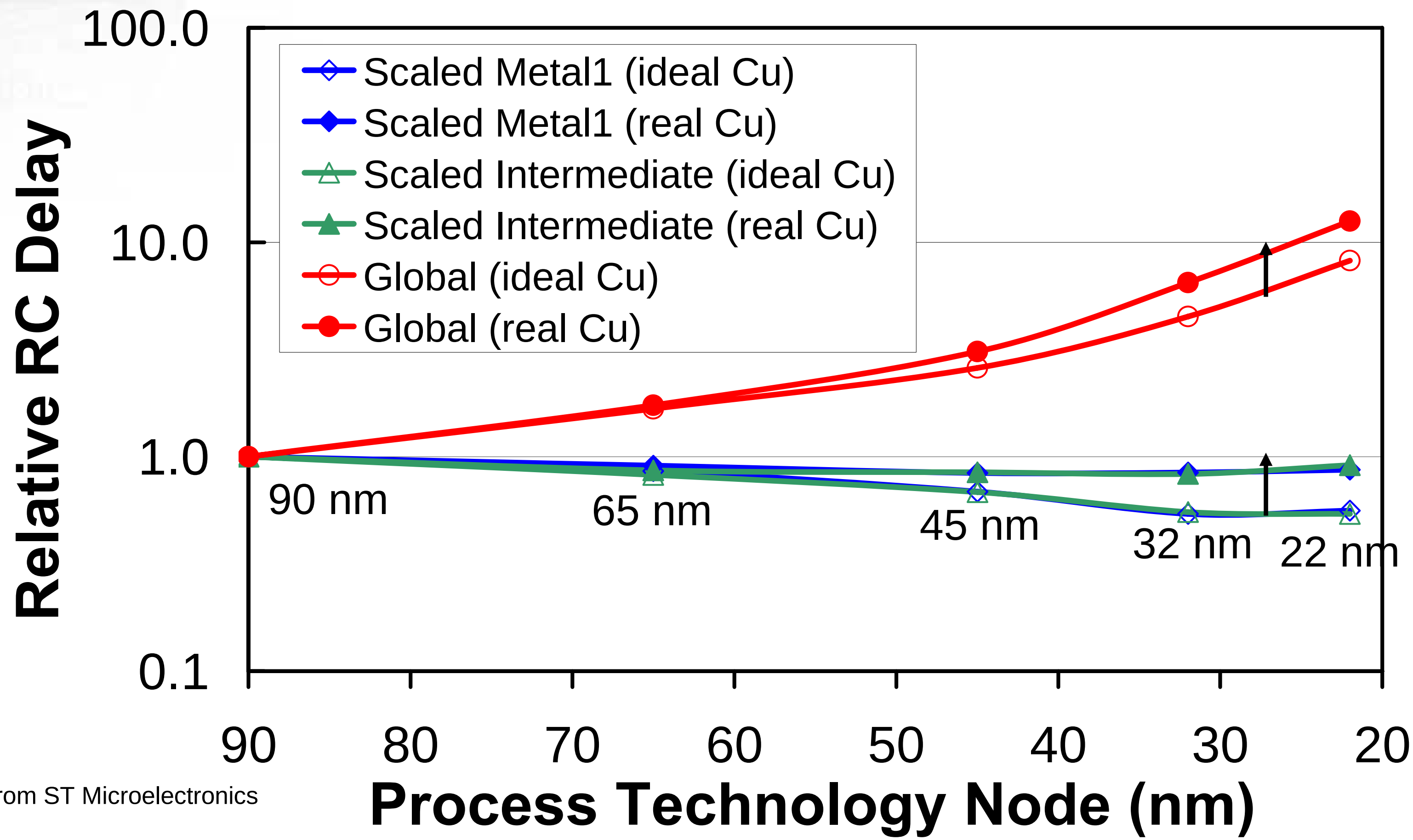


Figure From ST Microelectronics

- Minimum global and intermediate wires are impacted soon

Dynamic Power

- Increasing concern about rising dynamic power in the interconnect stack
  - Interconnects make a significant contribution to total dynamic power
- Impacts effective k roadmap
  - Drives reduction in parasitic capacitance
- Dynamic power is a key constraint for high performance MPUs
- Alternative interconnect technologies (optical, CNT, RF, etc.) should be performance competitive in terms of delay and power

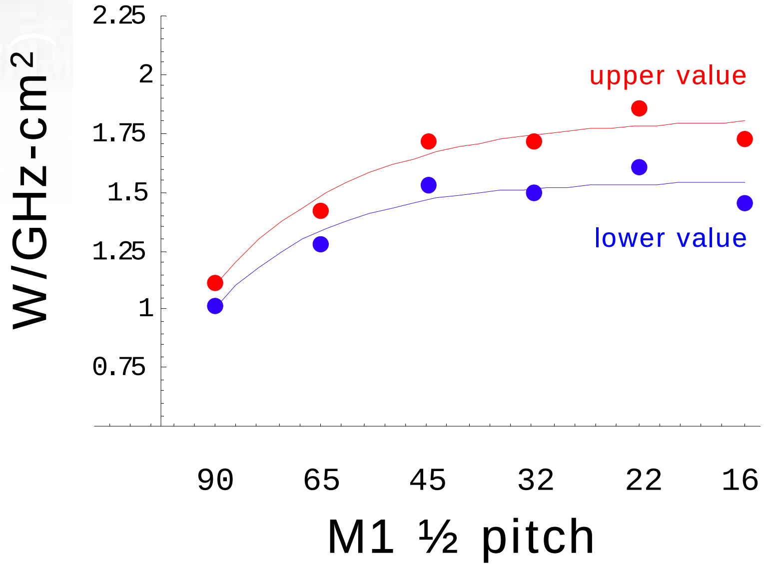
- Influence of number of functions (N), activity (A) and frequency (F) - P = (NAF)CV2

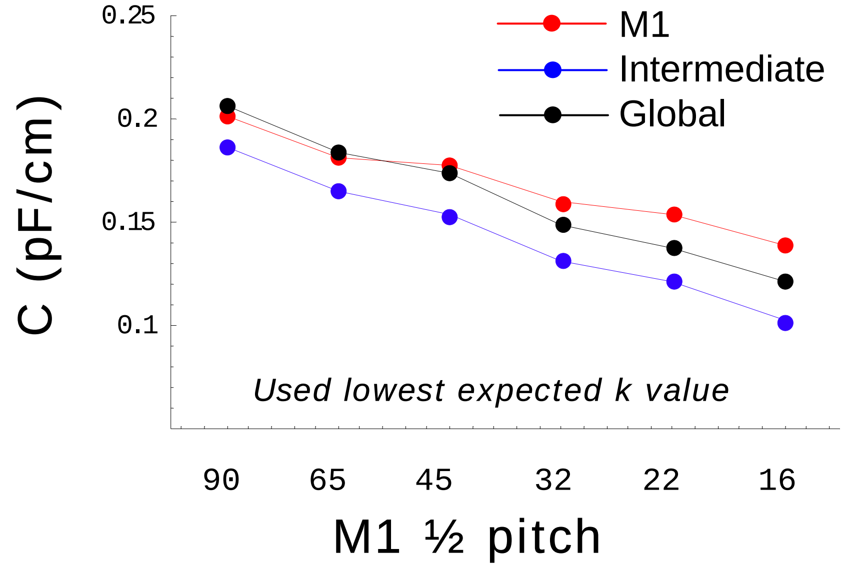
$$P_{layer}\left[\frac{W}{GHz-cm^2}\right] = C \cdot V^2 \cdot a \cdot (1\ GHz) \cdot \left(e_w \cdot \frac{1\ cm^2}{\mathrm{p}}\right) = \text{Power per GHz per cm}^2 \text{ of metal layer.}$$

C = capacitance per unit length.

$V = V_{dd}$, p = pitch, e_w = wiring efficiency, a = average activity factor of interconnects.

Capacitance and Power Index





- Capacitance per unit length decreases due to decreases of the dielectric constant.
- However, the dynamic power per metallization layer is expected to increase despite the efforts to decrease the dielectric constant and supply voltage.

Row to be added to table 80a ("***MPU and ASIC Interconnect Technology Requirements—Near-term Years***") shown in red

M1_half_pitch	90	78	68	59	52	45	40	35	32
Power index (W/GHz-cm^2) [x]	1-1.1	1.2-1.3	1.3-1.4	1.3-1.4	1.4-1.5	1.5-1.7	1.7-1.9	1.4-1.6	1.5-1.7

Row to be added to table 80b ("***MPU and ASIC Interconnect Technology Requirements—Long-term Years***") shown in red

M1_half_pitch	28	25	22	20	18	16	14
Power index (W/GHz-cm^2) [x]	1.7-2.0	1.4-1.6	1.6-1.9	1.3-1.6	1.3-1.5	1.5-1.7	1.7-2.0

FOOTNOTE TO BE ADDED AT THE BOTTOM OF TABLES 80 (a and b)

[x] Power index = C V_{dd}^2 a (1 GHz) e_w (1 cm^2)/p; p = pitch; V_{dd} = supply voltage; e_w = wiring efficiency = 1/3; a = activity factor = 0.03. The calculated values are an approximation for the "power per GHz per cm^2 of metallization layer". This index scales with the critical parameters that determine the interconnect dynamic power. NOTES: the values provided are an average for M1, Intermediate and Global interconnects. The range of values results from the maximum and minimum effective dielectric constants.

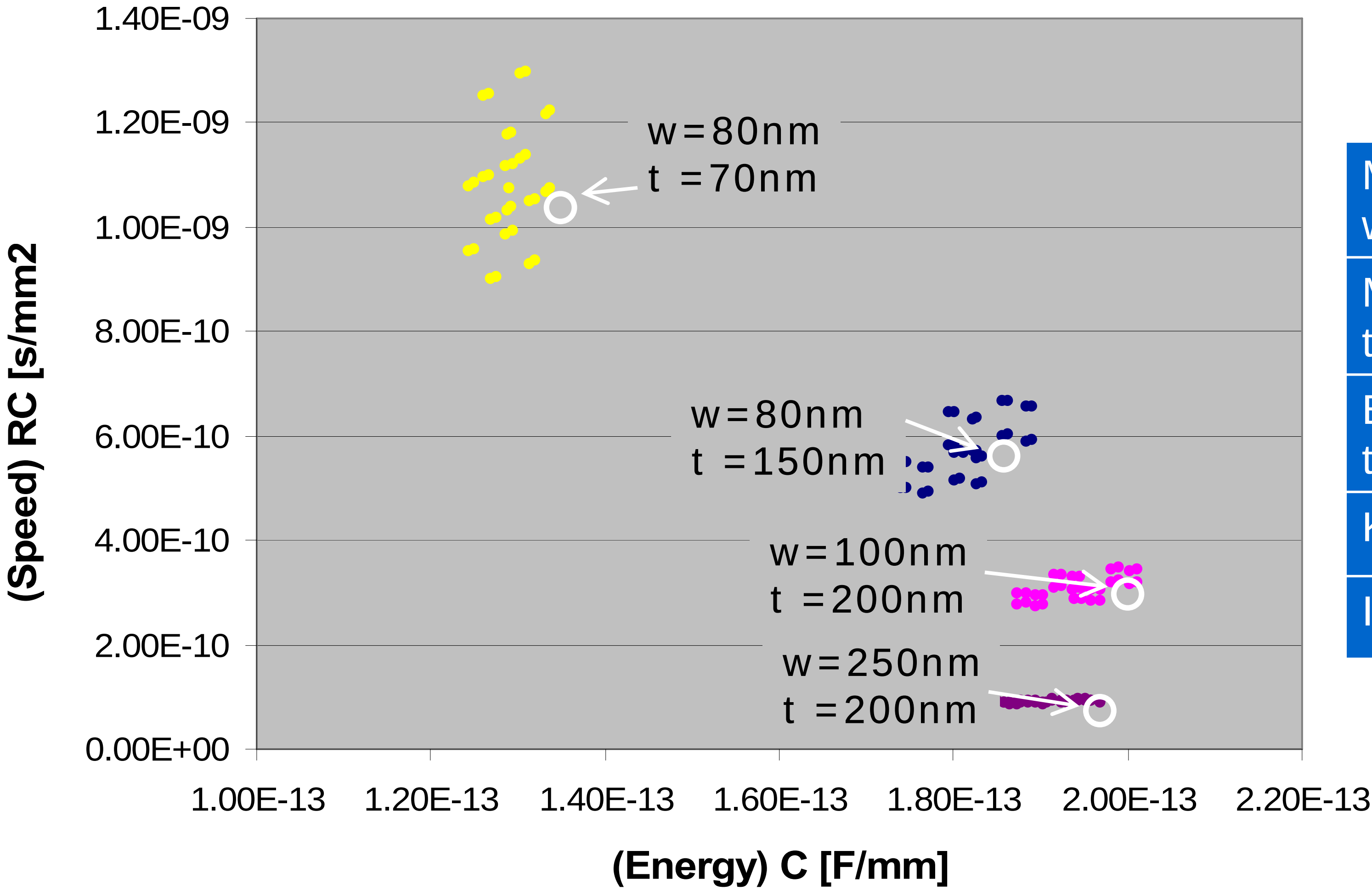
Row to be added to table 80a ("***MPU and ASIC Interconnect Technology Requirements—Near-term Years***") shown in red

M1_half_pitch	90	78	68	59	52	45	40	35	32
Capacitance per unit length for M1 wires (pF/cm) [y]	2.0-2.2	2.0-2.2	1.8-2.0	1.9-2.1	1.8-2.0	1.8-2.0	1.8-2.0	1.6-1.8	1.6-1.8
Capacitance per unit length for intermediate wires (pF/cm) [y]	1.9-2.0	1.9-2.0	1.7-1.8	1.7-1.8	1.5-1.7	1.5-1.7	1.5-1.7	1.3-1.5	1.3-1.5
Capacitance per unit length for global wires (pF/cm) [y]	2.1-2.3	2.1-2.3	1.8-2.0	1.8-2.0	1.7-1.9	1.7-1.9	1.7-1.9	1.5-1.7	1.5-1.7

Row to be added to table 80b ("***MPU and ASIC Interconnect Technology Requirements—Long-term Years***") shown in red

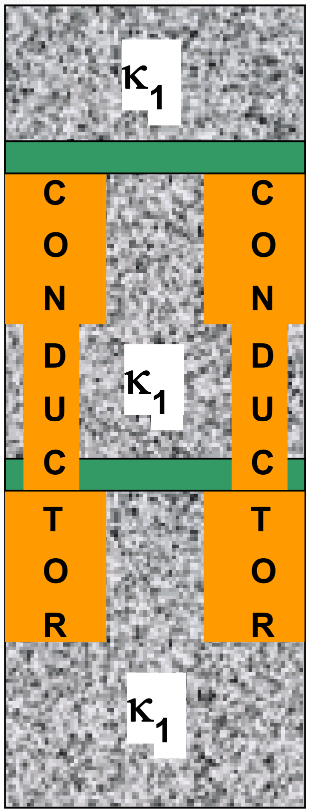
M1_half_pitch	28	25	22	20	18	16	14
Capacitance per unit length for M1 wires (pF/cm) [y]	1.6-1.8	1.5-1.7	1.5-1.8	1.5-1.8	1.4-1.6	1.4-1.6	1.4-1.7
Capacitance per unit length for intermediate wires (pF/cm) [y]	1.3-1.5	1.2-1.4	1.2-1.4	1.2-1.4	1.0-1.2	1.0-1.2	1.0-1.2
Capacitance per unit length for global wires (pF/cm) [y]	1.5-1.7	1.4-1.6	1.4-1.6	1.4-1.6	1.2-1.4	1.2-1.4	1.2-1.4

R and C variability

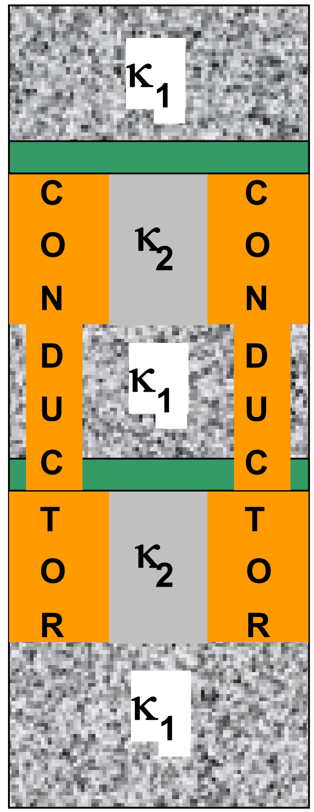


Metal width	± 6nm
Metal thk	± 4nm
Barrier thk	± 2nm
Keff	± 0.1
ILD thk	± 4nm

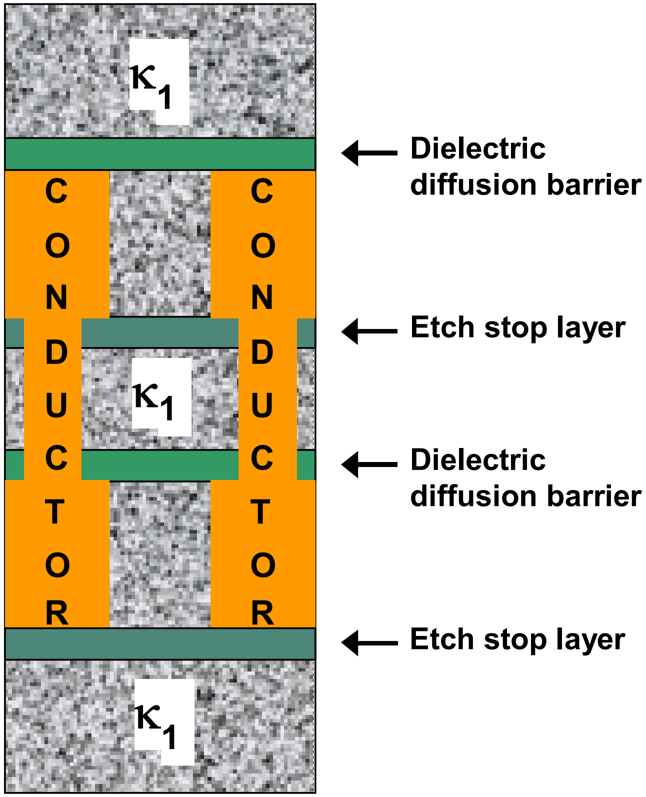
Integration Schemes



Homogeneous ILD without trench etch stop

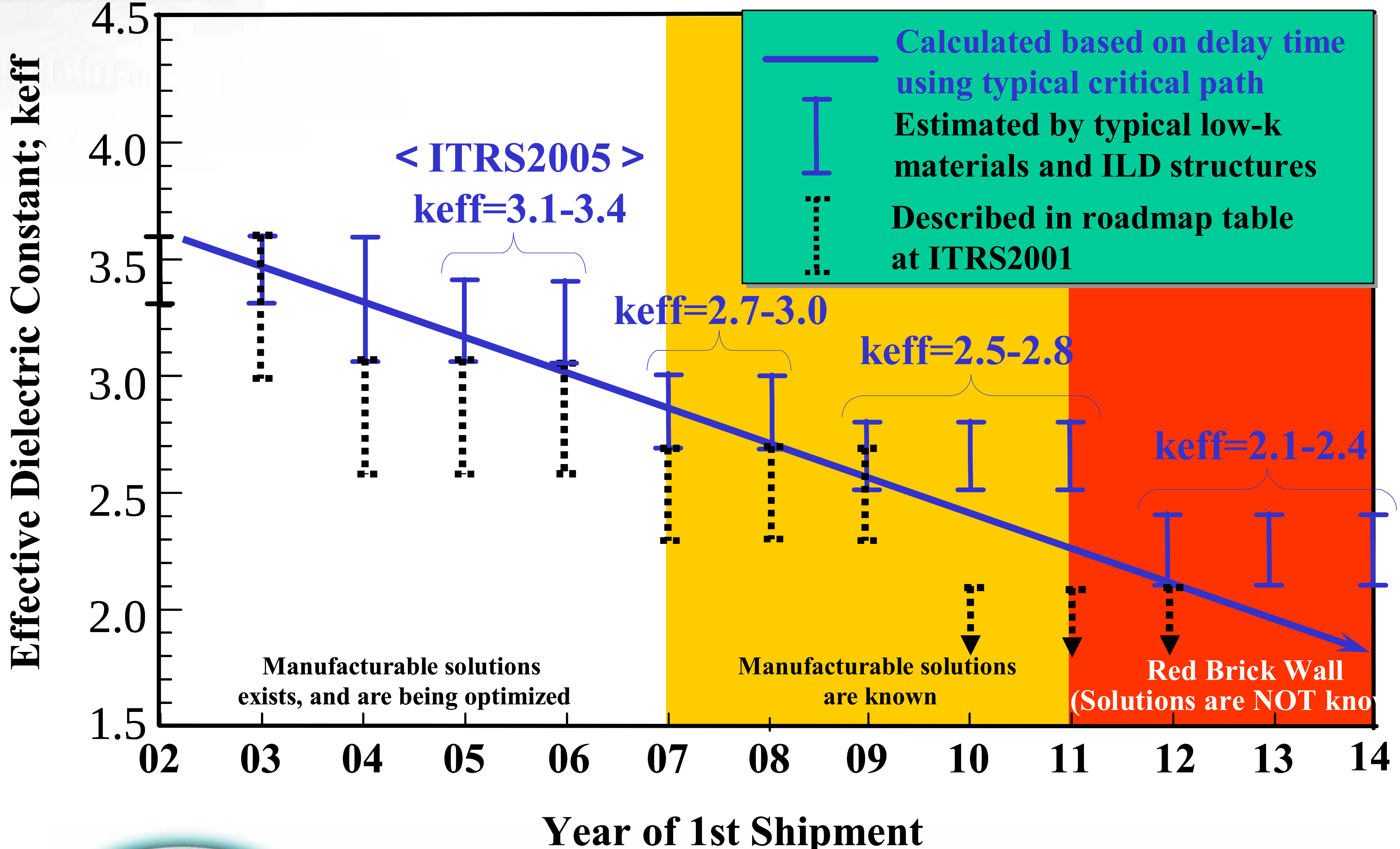


Embedded low κ ILD ($\kappa_1 > \kappa_2$)



Homogeneous ILD with trench etch stop

Dielectric models



Low κ again! HP MPU and ASIC

	Year of Production	2005	2006	2007	2008	2009	2010	2011	2012	2013
	DRAM ½ Pitch (nm) (contacted)	80	70	65	57	50	45	40	36	32
	MPU/ASIC Metal 1 ½ Pitch (nm)(contacted)	90	78	68	59	52	45	40	36	32
	MPU Physical Gate Length (nm)	32	28	25	22	20	18	16	14	13
Was	Interlevel metal insulator (minimum expected) – bulk dielectric constant (κ)	≤ 2.7	≤ 2.7	≤ 2.4	≤ 2.4	≤ 2.2	≤ 2.2	≤ 2.2	≤ 2.0	≤ 2.0
Is	Interlevel metal insulator – bulk dielectric constant (κ)	2.6-3.0	2.6-3.0	2.3-2.7	2.3-2.7	2.1-2.4	2.1-2.4	2.1-2.4	1.8-2.1	1.8-2.1

DRAM

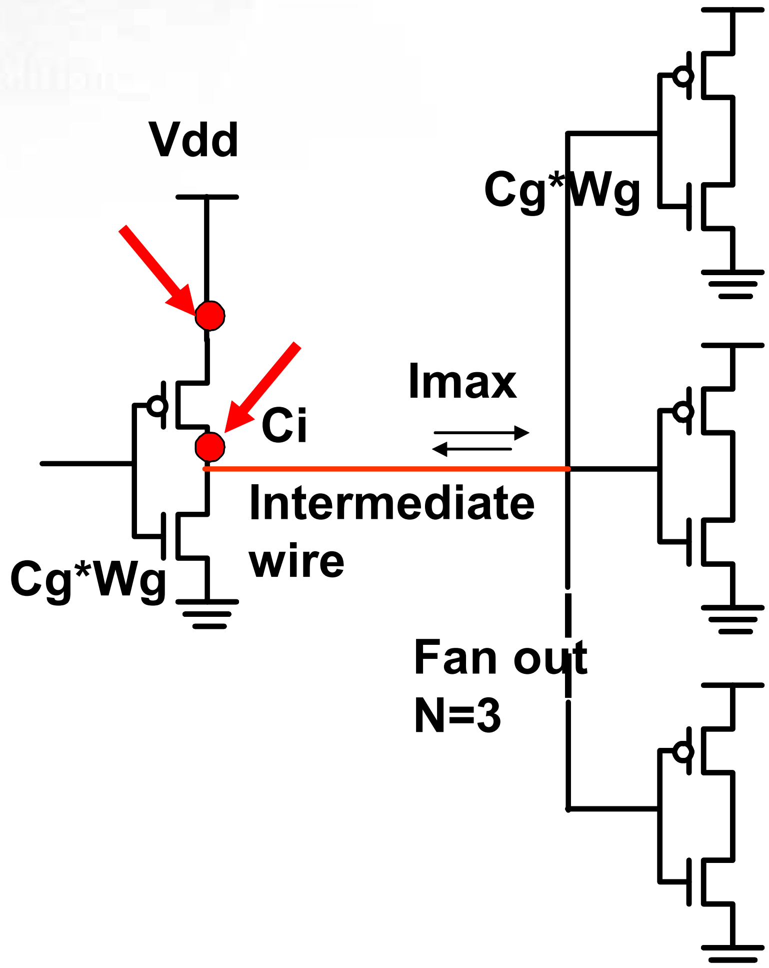
Small changes in specific via and contact resistivity

Contact A/R rises to >20 in 2020 - a red challenge - associated with the 16 nm DRAM half pitch

Low k in 2003 - Cu delayed to 2007

Plan to distinguish embedded, flash, and traditional DRAM in the future (2007)

Jmax 2006 – no changes



Inverter circuit (F.O=3)

-Minimum Tr width (Wmin.):

NMOS Gate width= (ASIC Half-pitch)x 4

PMOS Gate width=(NMOS Gate-width) x 2

-Tr-width (Wg):

Wg =Wmin.x 8

-Gate capacitance(Cg)

-Wiring length (Li): IM-Pitch x 200

-Wiring capacitance(Ci): Updated keff

Average current density of IM-interconnect (J_{max})

$$= f\,(Cg*Wg*N+Ci)*Vdd/(Wi*Ti)$$

Multi-core Impact on Interconnect

- Wiring lengths change
  - Critical path reduced (in core)
  - Mechanical integrity challenges will change
  - Jmax changes
  - Hierarchical structure may no longer be necessary
    - Converge to more fine pitch local/intermediate wires
    - Power and ground delivered through grid
  - Global delay challenge relaxed
  - 3D may include multi-core
- Need to consider splitting metrics into:
  - In-core (intra-tile) and Inter-core (inter-tile)
    - New bandwidth requirements

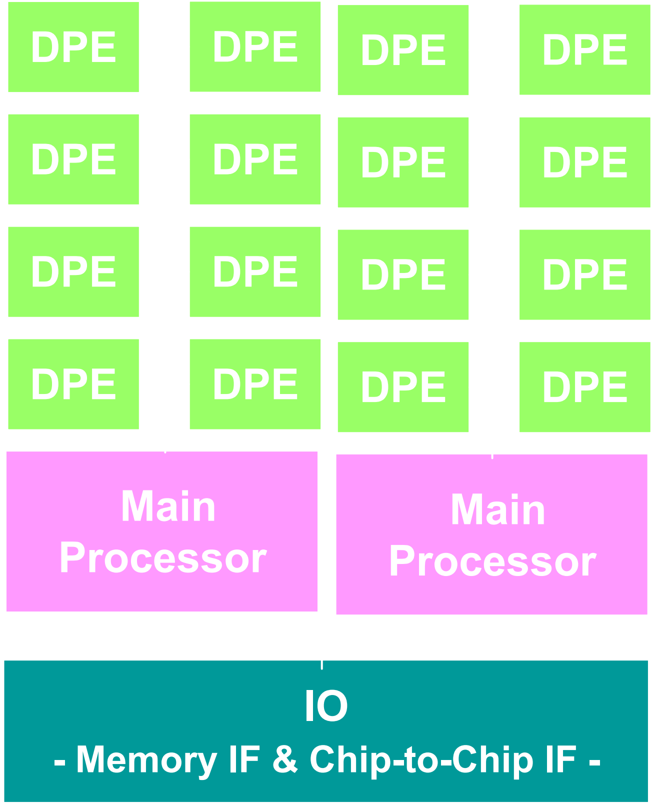


Figure From ITRS 2006 Design TWG

Emerging Interconnect

- Use geometry
  - 3D
  - Air gap
- Use different signaling methods
  - Signal design
  - Signal coding techniques
- Use innovative design and package options
  - Interconnect - centric design
  - Package intermediated interconnect
  - Chip-package co-design

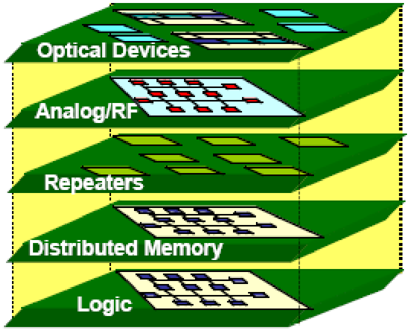


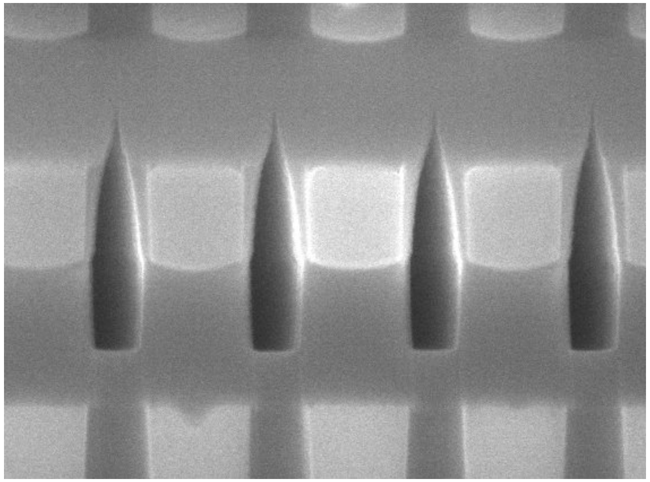
Figure From Stanford

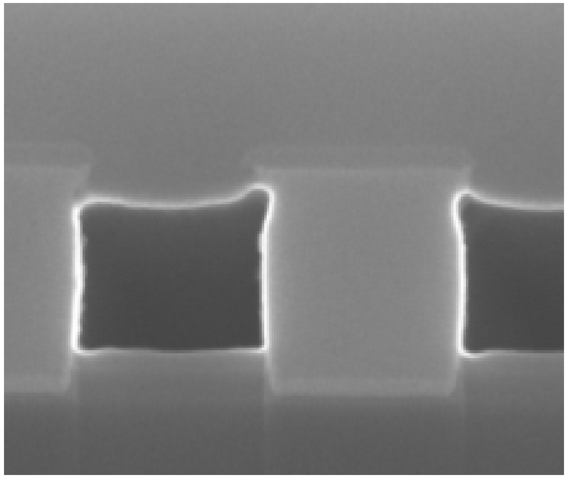
Emerging interconnect

- Use different physics
  - Optics (waveguides, emitters, detectors, free space, trans-impedance amps, modulators)
  - RF/microwaves (transmitters, receivers, free space, waveguides)
  - Terahertz photonics
- Radical solutions
  - Nanowires/nanotubes
  - Molecules
  - Spintronics
  - Quantum wave functions

From low κ to no κ - air gaps

- Introduction of air gap architectures
  - Creation of air gaps with non-conformal deposition
  - Removal of sacrificial materials after multi-level interconnects





⇒ Values of effective k-value down to 1.7 with low crosstalk levels

⇒ Localized air gaps to maintain good thermal and mechanical properties

Ultra-low κ and Air gap (κ<2.0) (CVD & Spin-on)

3D Integration – first thoughts

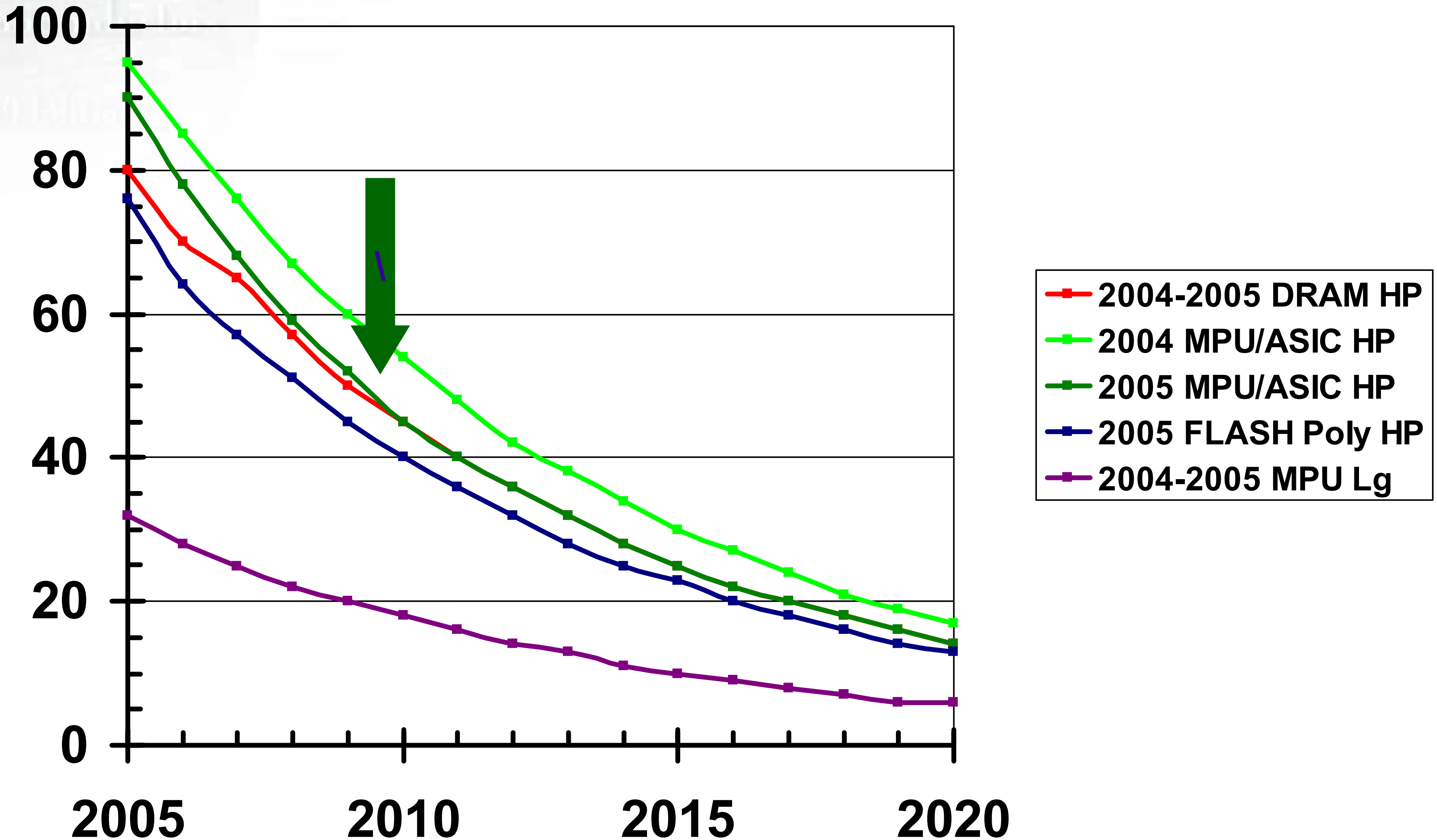
- Through silicon via (TSV)
  - Reliability
  - Physical metrics (pitch, diameter, density)
- Alignment tolerance
- Bond layer
  - Reliability
  - Interfacial defect density
  - Adhesion
- List of "Difficult Challenges", e.g. TSV processes, alignment, low k impact on TSV, etc.

2006 last words

- Metal 1 design rule concerns
  - Staggered pitch used for definitio
    - 78 nm half pitch for 2006
    - High performance MPU pitches scaling at ~0.75/2 years until 2009
    - Returning to 0.7/3 years 2010

- Working with Design, Assembly and Packaging and Test groups to identify directions for 3D ICs – may address global wiring problem

M1 Half Pitch Trends



Last words

- Must manage the power envelope
- Develop solutions for emerging devices
- Must manage 3DCD
- System level solutions must be accelerated to address the wire scaling grand challenge
  - Cu resistivity increase impact appears ~2006
  - materials solutions alone cannot deliver performance - end of traditional scaling
  - integrated system approach required