

# **ITRS Roadmap Design + System Drivers** *2006 Summer Meeting*

**San Francisco, July 10-12**

Worldwide Design TWG



# Key Thoughts

- 1. Last year we created a Design Technology Roadmap**
  - *System-level, logic/ckt/phy, DFT, Verification, DFM,*
  - *General dependency: PIDS, yield, interconnect, A&P,...*
- 2. This year we're creating a Systems Driver roadmap**
  - Consumer stationary, networking, auto
  - *Driver-specific dependency: PIDS, interconnect, A&P,...*
- 3. Added value = design technology + design innovation**
  - Design technology: general value add
  - Design innovation: driver-specific value add





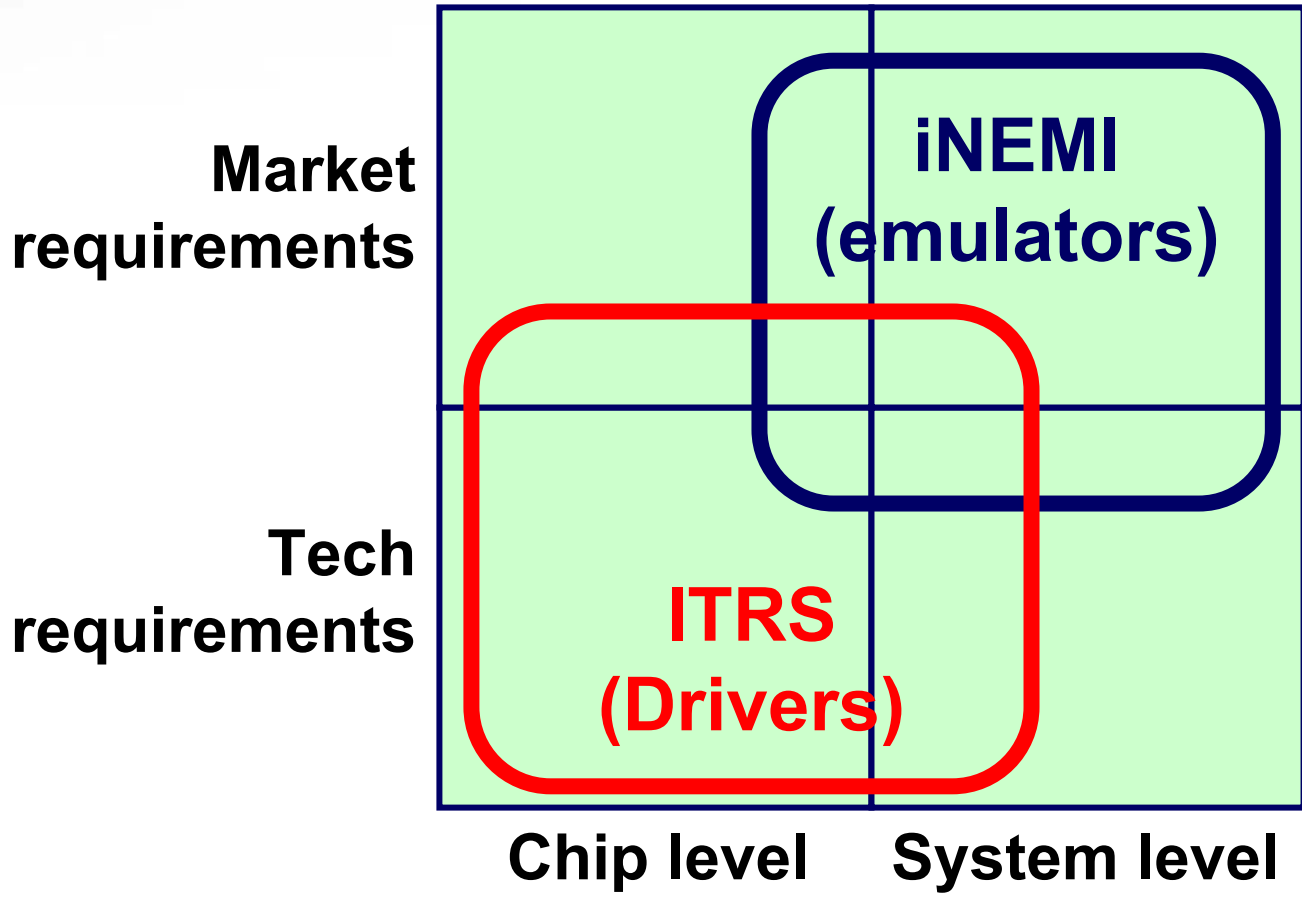
# Working Table For Design Chapter

Section	Action and status	Leader
<b>General</b>	<ol style="list-style-type: none"> <li>1. Share formula or approach for each value</li> <li>2. Requirements-solutions correspondence table</li> </ol>	<b>All</b>
<b>System Level</b>	<p>2006 → 1-2 new HD-SW metrics (virtual prototyping, parallel compiler)</p> <p>Text definition of TLM (Ecker)</p>	Rosenstiel <b>DONE</b>
<b>Logic/circuit/physical</b>	<p>See Jap. Comments on each metric.</p> <p>Adequacy for metrics and fluctuation.</p> <p>Thermal design (esp. AMS)</p>	Kravets <b>Pending</b>
<b>Design verification</b>	<p>See Jap. Comments on rows. Possible errors.</p> <p>New verification topics. Table relating reqs-sols</p>	Bertacco <b>Pending</b>
<b>Design Test</b>	<p>Reduce focus on analog/MS. Get more data from industry. Run cross-TWG interlock team.</p> <p>Add SIP-DFT to system-level design solutions (multi-fabric implementation planning)</p>	Soma <b>Pending</b>
<b>DFM</b>	<p>Explain red brick boundary (performance, power)</p> <p>Fix typo and recalculate. Explain metrics around Vth variability.</p>	Carballo / Kahng / Nassif

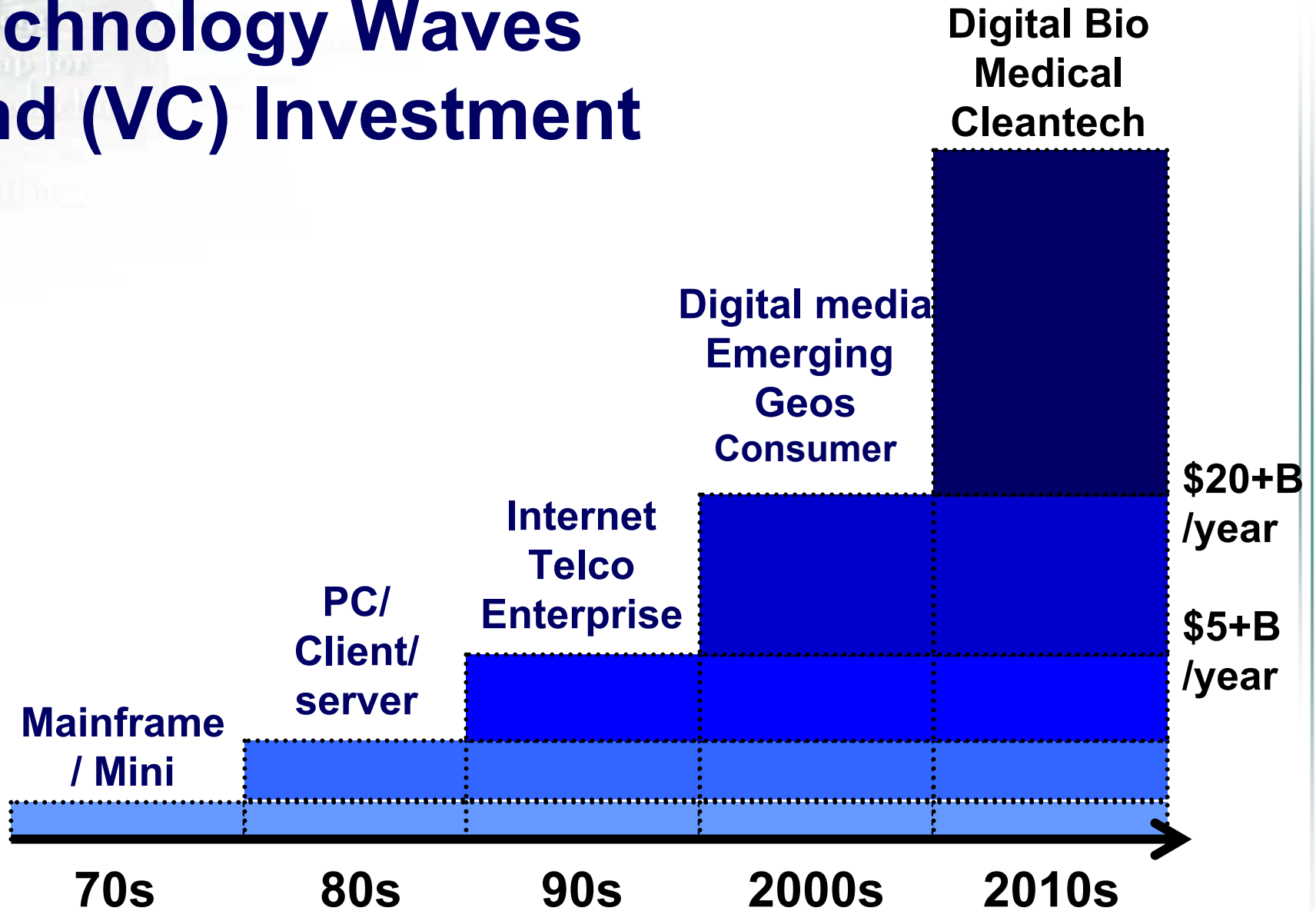
# System Drivers Chapter



# ITRS-iNEMI Domain Space



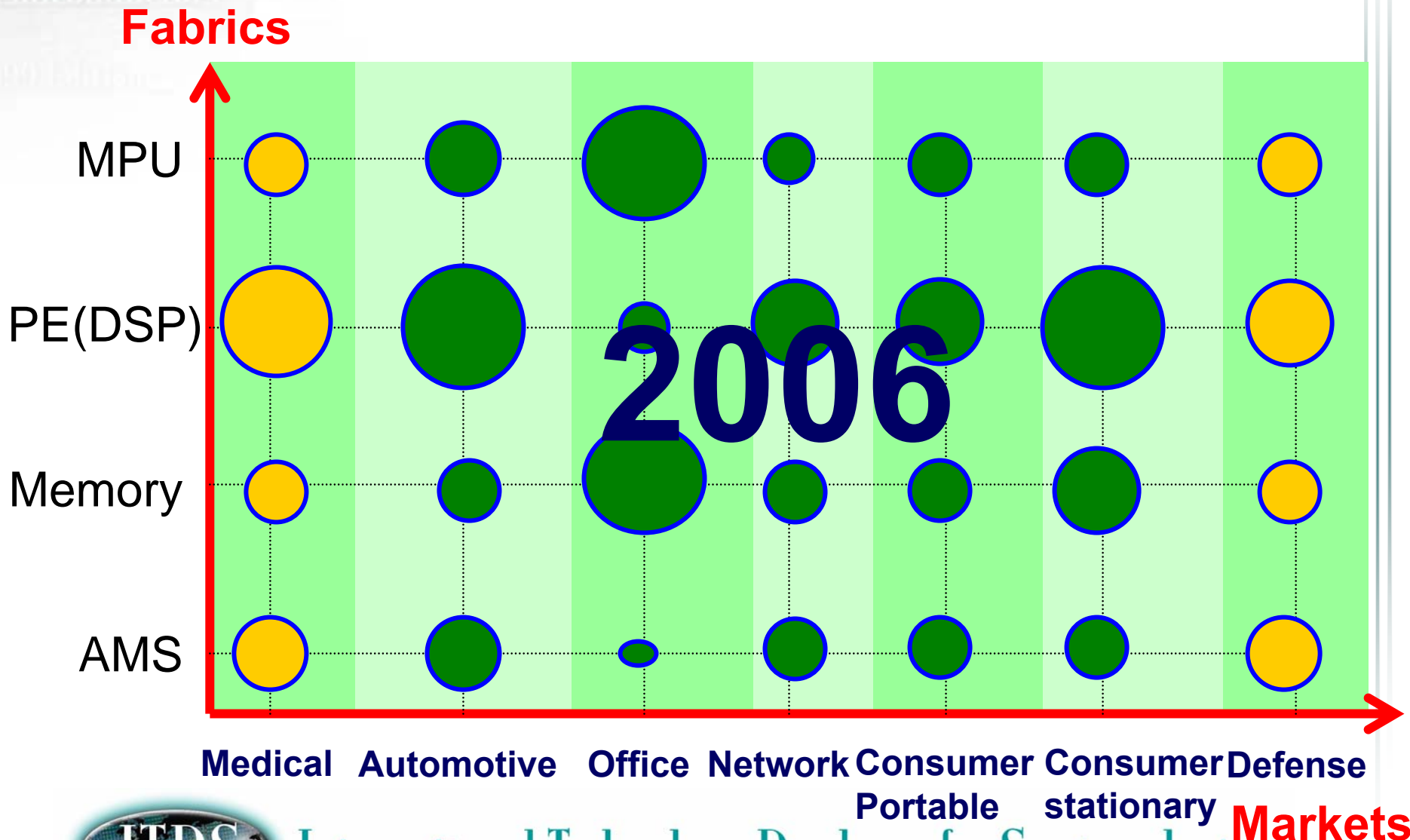
# Technology Waves And (VC) Investment



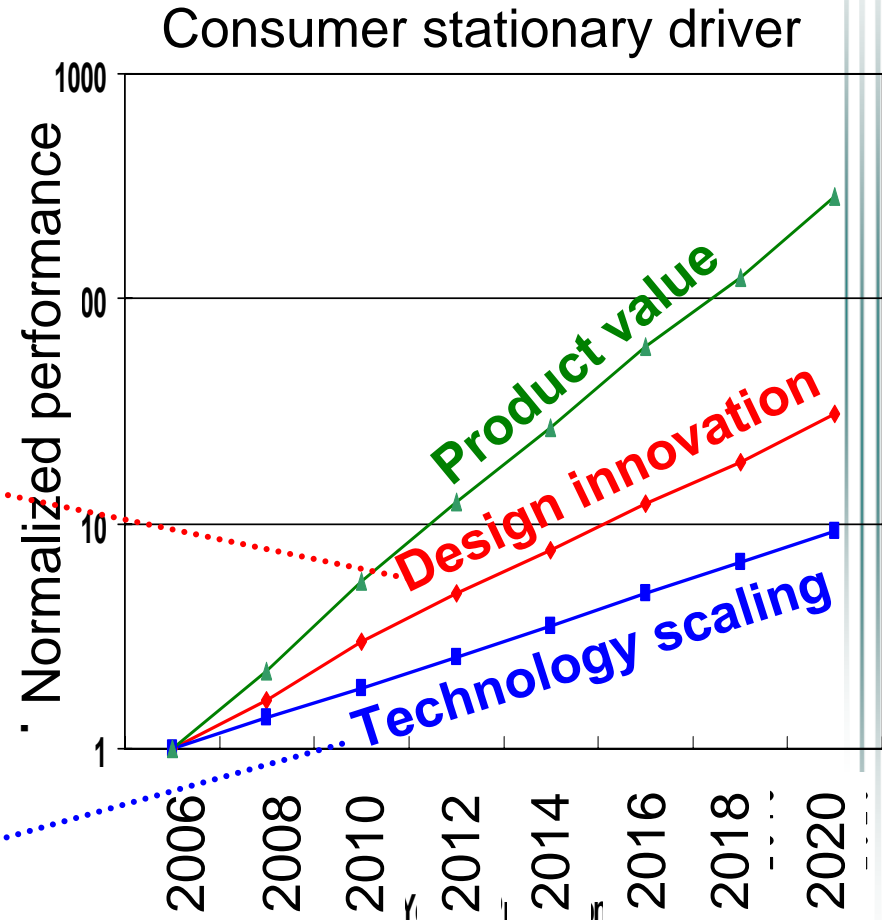
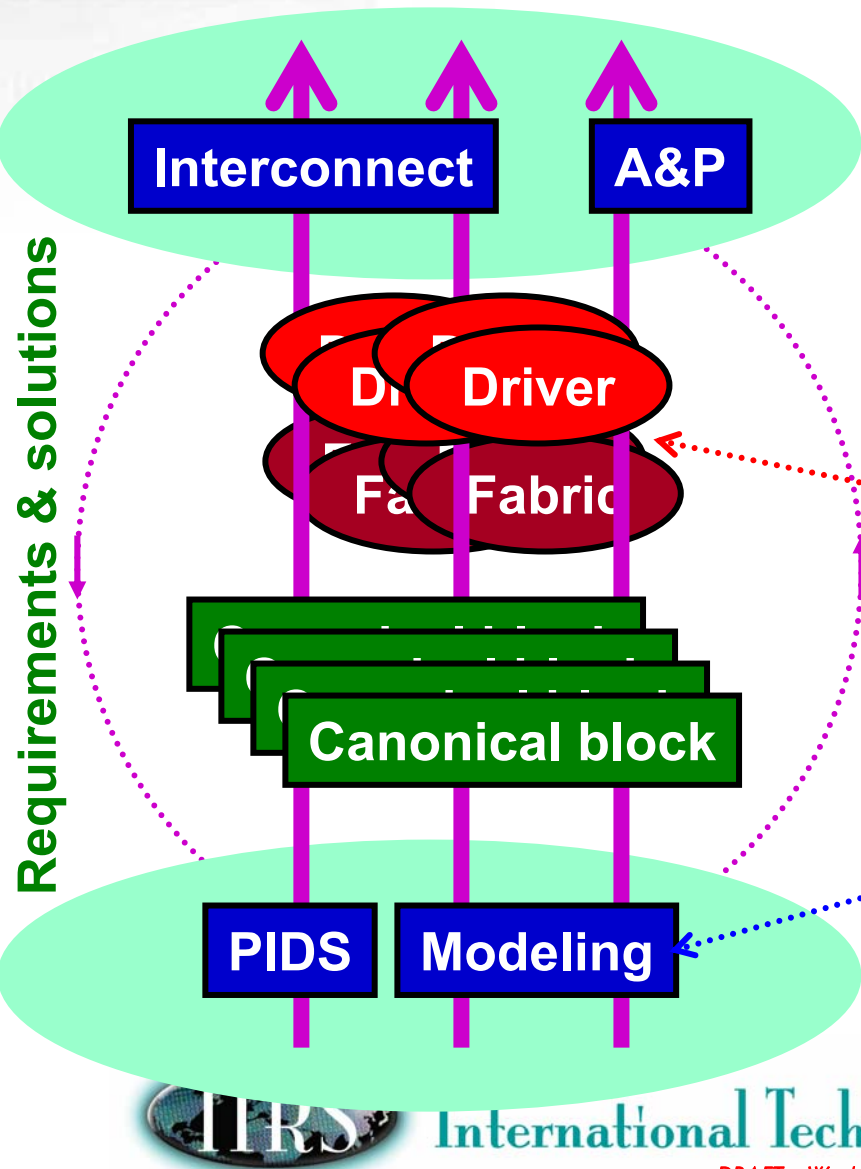
Source: insight from Top VCs including Walden  
International Technology Roadmap for Semiconductors

DRAFT - Work In Progress - NOT FOR PUBLICATION 12 July 2006

# Market Drivers Starting To Drive Roadmap



# Market Drivers As Value Adders



- #DPEs, other
- Intrinsic switching speed
- Performance

# Driver Template

Driver parameter	Example	Units
<b>Market requirements</b> (customers AND suppliers)	Cost, Performance Energy consumption / battery life Time to market Reliability, environmental?	\$ / unit Pages / sec Hours Months Years
<b>Critical design requirements</b>	Power, Area, Time per operation / clock speed Latency / throughput / bandwidth Design productivity Hours of operation, Environmental constrs.	Watts mm <sup>2</sup> GHz Nano-secs PY/ mm <sup>2</sup> Hours
<b>Critical design parameters</b>	Memory size / bandwidth # processing units, redundant units Size and clock speed/BW of each unit Number of pins	Bytes <None> Mm <sup>2</sup> <None>



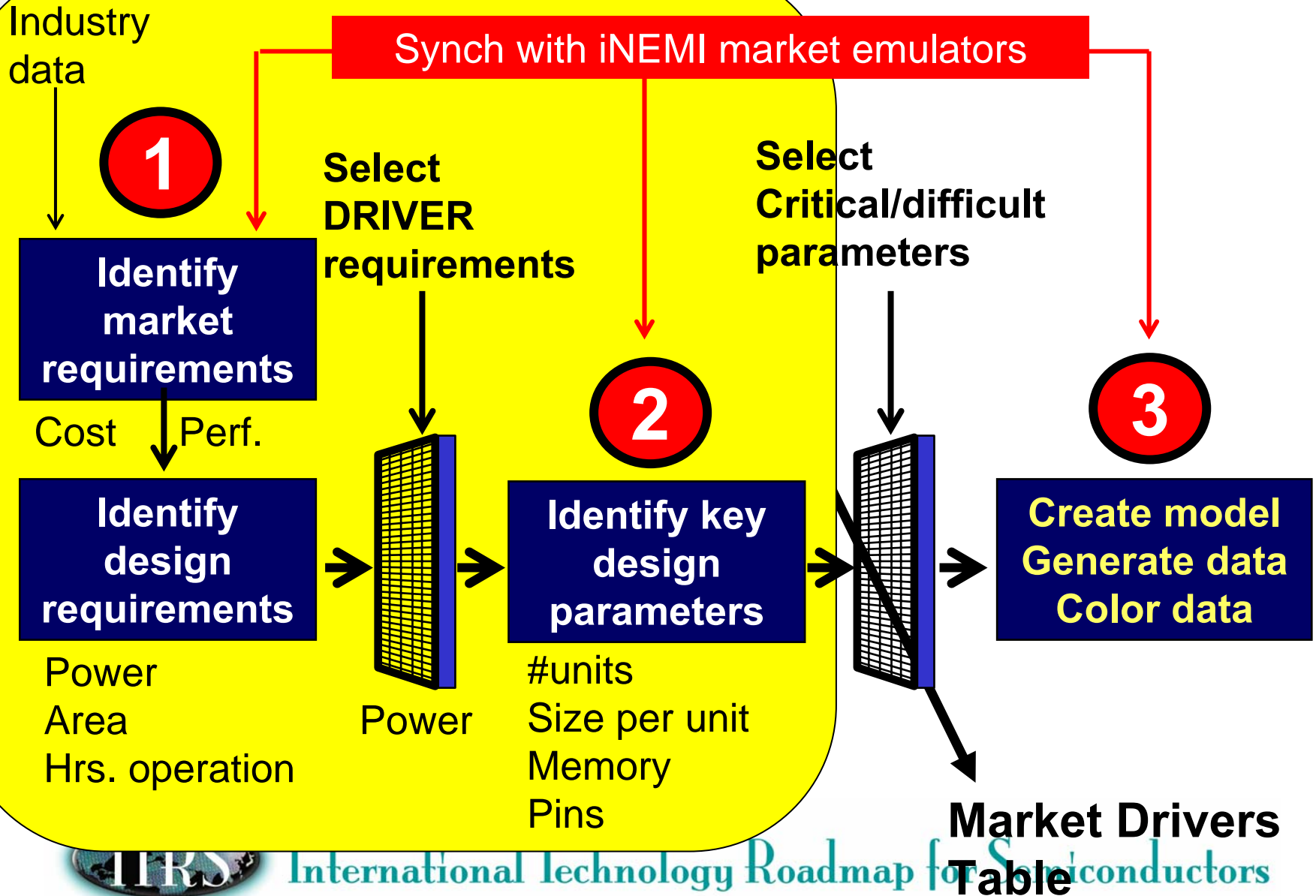
# System (Market) Drivers Working Table

Driver	Market ST/LT requirements	Design requirements	Design parameters	Leader
Office/PC (processor)	(General) Performance	Clock cycle MIPS, FLOPS	#of cores memory	US 2005
Consumer (portable)	Energy cost	W, hours of operation (energy)	# of cores, voltage, clock cycle, etc.	Asia 2005 (Japan)
Consumer (stationary)	(Media/emerg) performance	Frames/sec, FLOPS	# of SPUs, memory BW, etc., latency	Asia 2006 (Japan)
Network (comms.)	Bandwidth	G/Tbits/sec	# of I/Os, BW per I/O, etc.	US 2006
Automotive (industrial)	Reliability Accuracy	Years, max/min T, radiation, sensing accuracy	% redundancy	EU 2006
Medical	Heterogeneous Integration?	Analog, digital, chemical, bio, sensors, etc.	#of (bio, chem) sensors on-chip,	EU 2007
Defense	Reliability (extreme)	Years, max/min T, radiation,	Redundancy	USA 2007

# System (Market) Drivers Working Table

Driver	Market ST/LT requirements
<b>AMS</b>	<p>Software-defined radio as a trend (text)</p> <p>If they'll send info about ADC/PA requirements, we'll look at numbers again and see if we need to change them</p>
<b>Consumer stationary and mobile</b>	<p>Send power trends and number of transistors and proportion to PIDS</p>

# Process For Each System Driver



# System Drivers

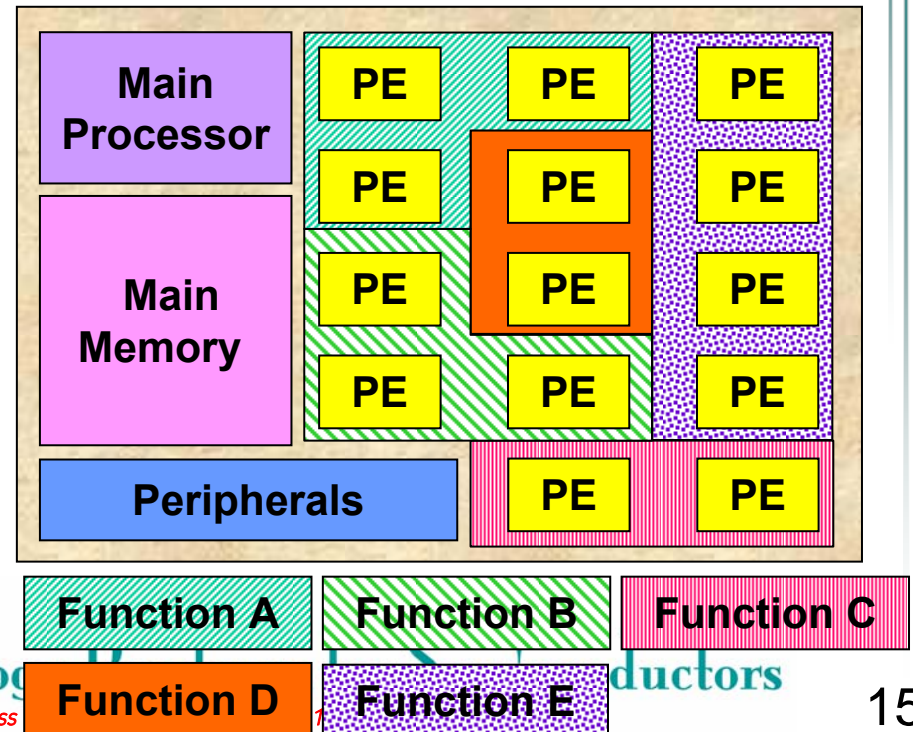
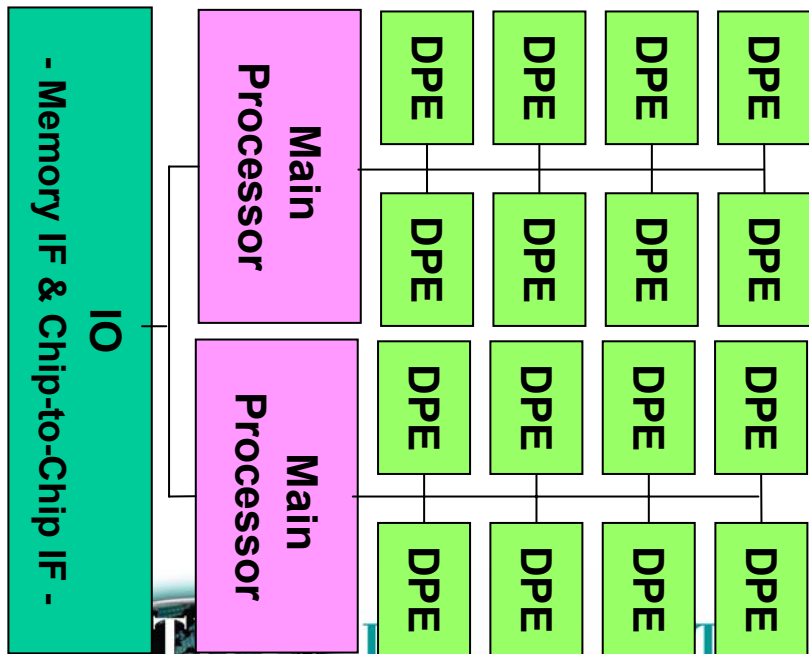
## Possible ITRS-iNEMI Engagement Model

Driver	ITRS	iNEMI
Office / large business	US TWG (A. Kahng UCSD)	Tom Pearson, Intel Erich Klink, IBM
Portable / Consumer	Japan TWG (Hiwatashi-san Toshiba)	Susan Noe, 3M
Automotive	EU TWG (J.P. Schoelkopf ST )	Jim Spall, Delphi
Networking / Communications	US TWG (Joe Abler, IBM)	Tom Pearson, Intel Erich Klink, IBM
Aerospace/ Defense	TBD 2007	William Murphy, Lockheed Martin
Medical Products	TBD 2007	Terry Dishongh, Intel

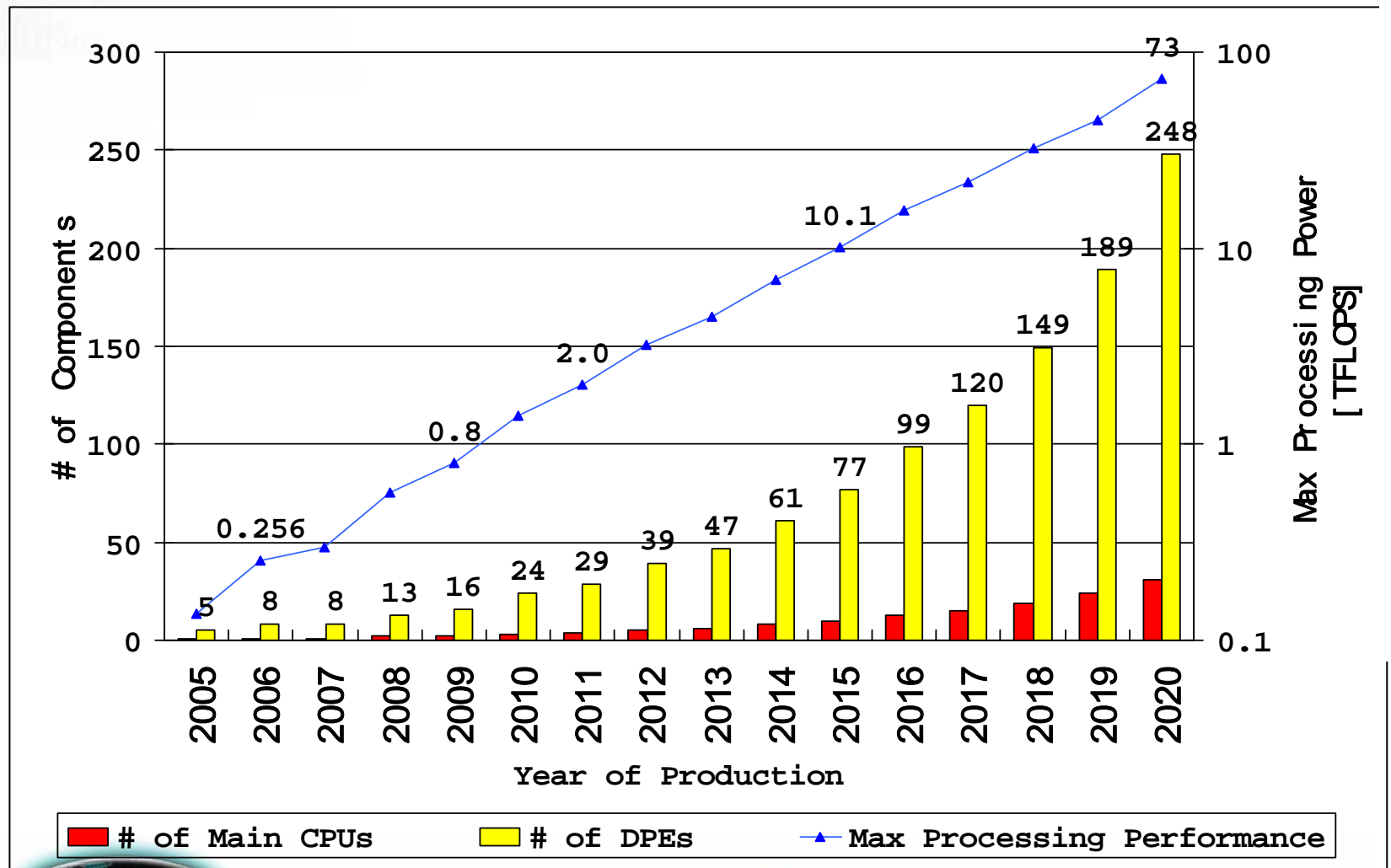


# Generic features of “SOC Consumer Stationary” Contrast with “SOC Consumer Portable”

SOC Consumer Stationary	SOC Consumer Portable ( SOC Power Efficient)
Core SOC of Consumer Electronics Applications	Core SOC of Personal Mobile Electronics Applications
Many Data Processing Engines (DPE) with high processing performance to cope with high level functions implemented by SW	Many Processing Engines (PE) dedicated for each function to achieve low power



# Design Trend: # of Processors & Processing Performance



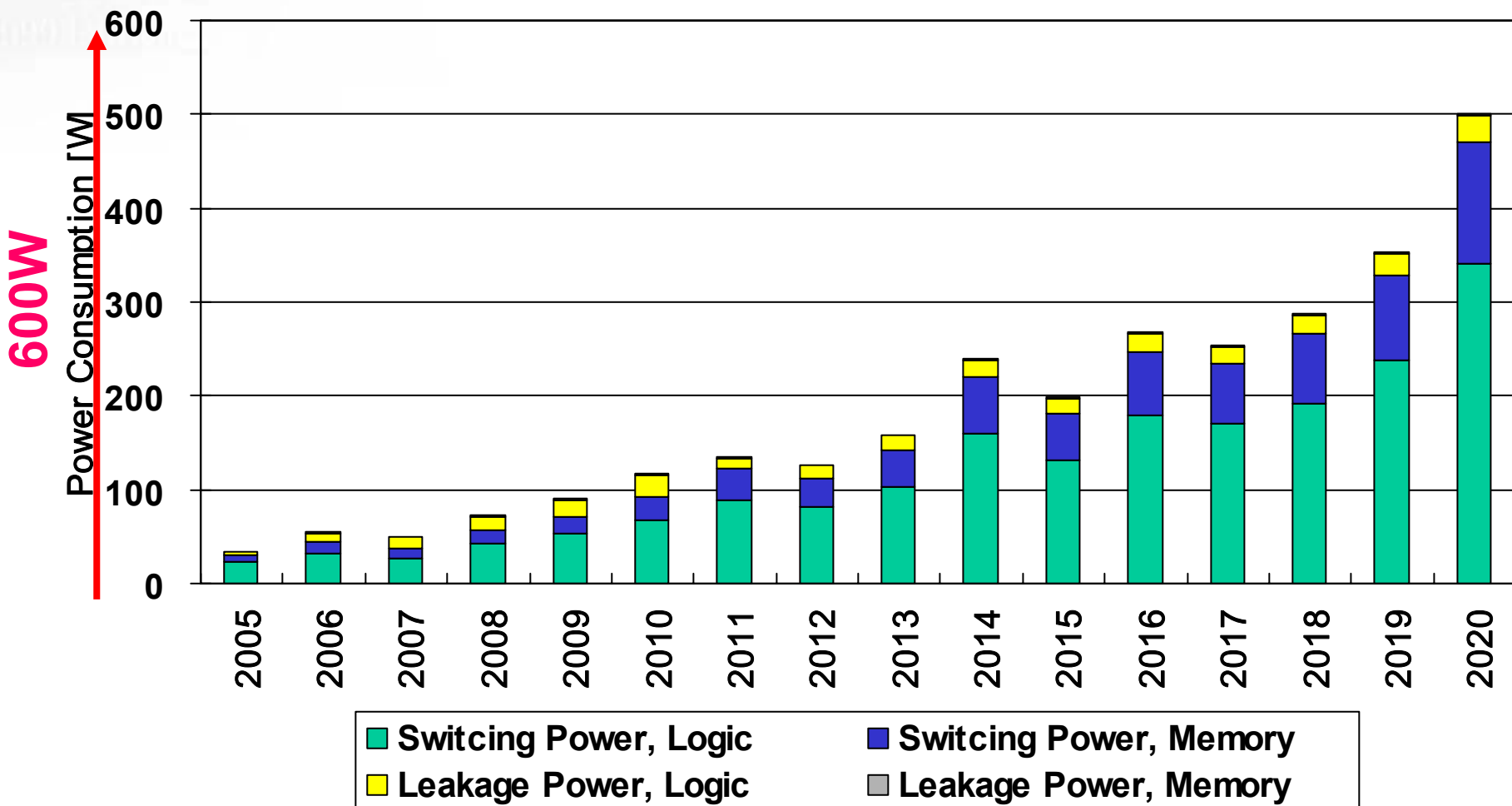
Max Processing Performance [TFLOPS]

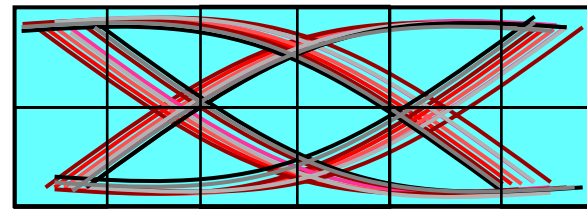
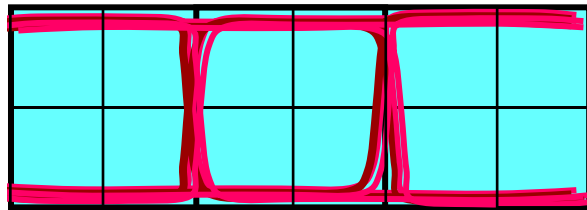


# Design Trend: Power Consumption

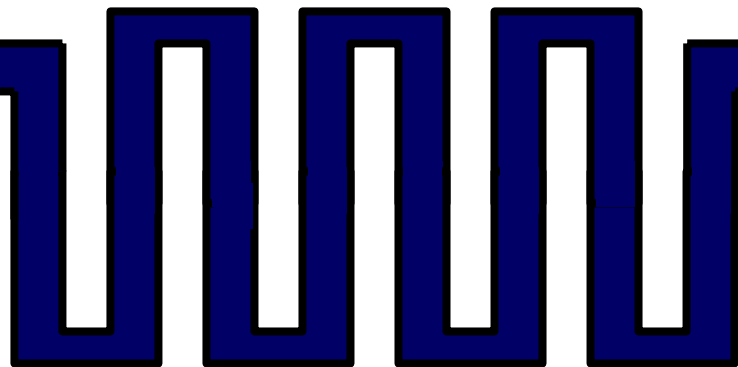
## – SOC Total

SOC total power consumption rapidly increases



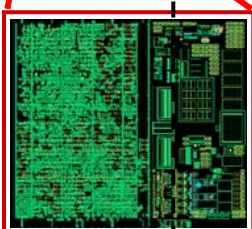


Channel

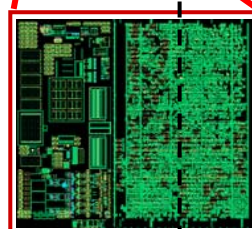


A Networking Driver

Transmitter core



Receiver core

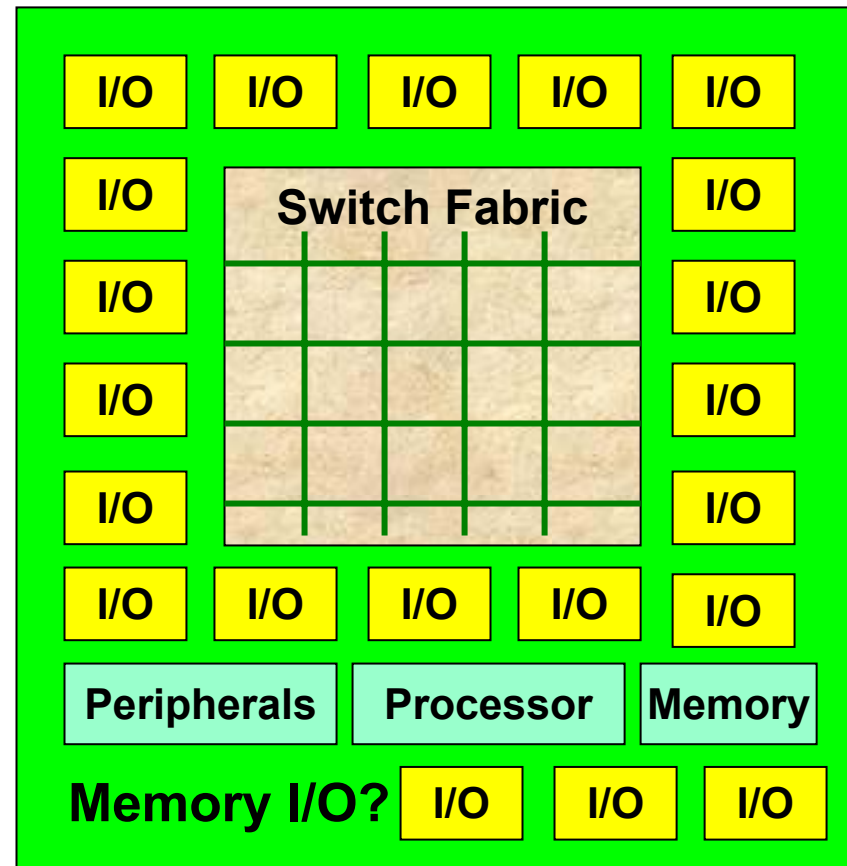


High-bandwidth host chip

High-bandwidth switch chip

# Chip Structure

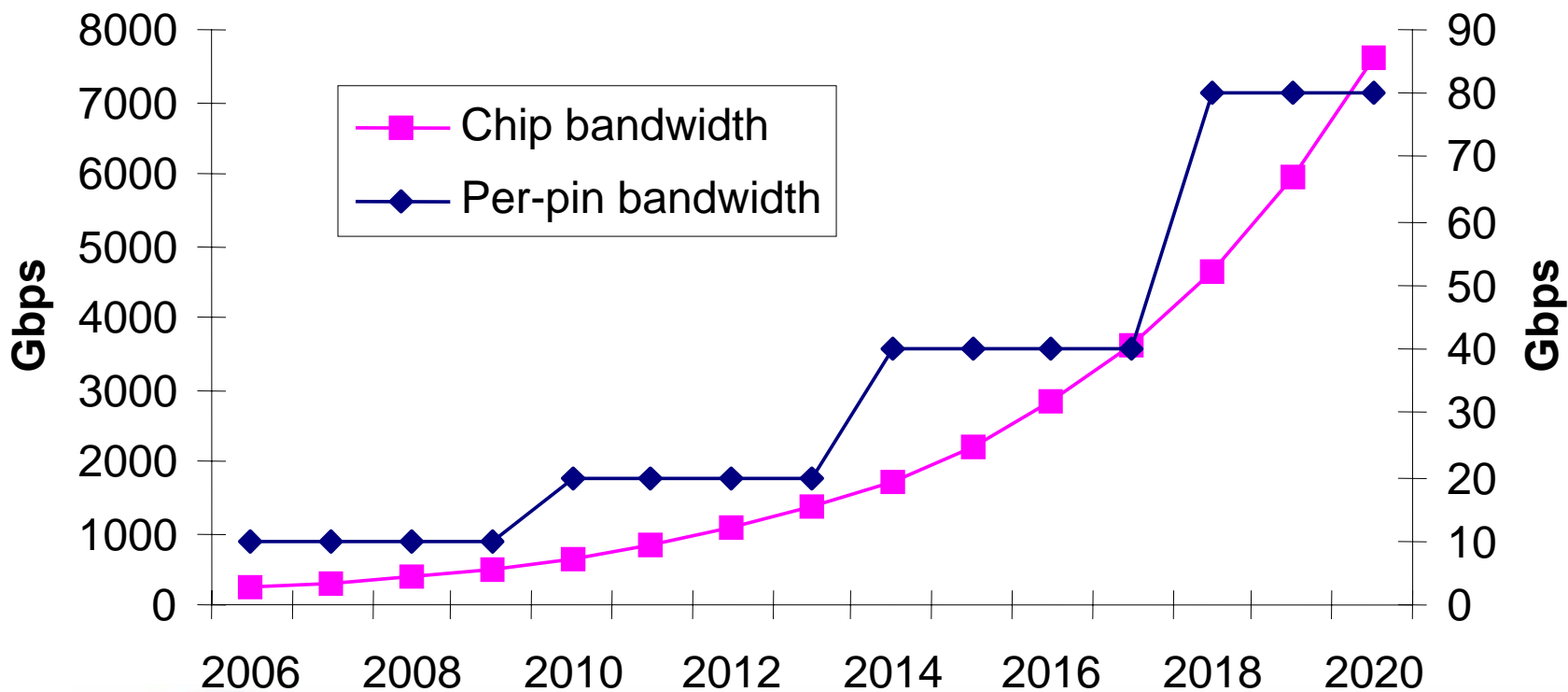
- **Very high bandwidth**
  - Key driver
- **Large size**
- **Many high-speed I/Os**
  - Mixed signal
  - Consume lots of power
- **Key components**
  - I/O
  - Switch fabric
  - Possible control processor and memory
  - CMOS technology



# Evolution of Key Parameters

## ■ Bandwidth driver

- Combination of technology scaling and bandwidth standards
- Assume I/Os dominate driver



# Summary

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## 3. Added value = design technology + design innovation

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