Yield Enhancement - International Technical Working Group

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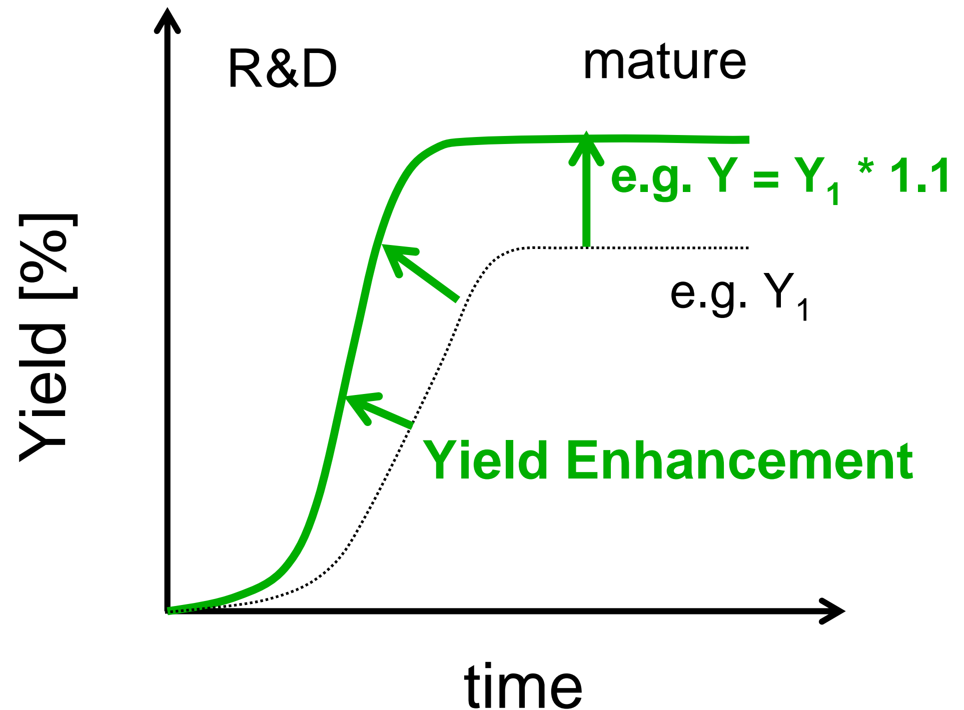
Outline

- Chapter Outline
- Organization of the Chapter
- 2005 Revision of Key Challenges
- 2005 Revision at a Glance
- Yield Enhancement International Technical Working Group contributors
- Subchapters
  - Defect Detection and Characterization
  - Wafer Environment Contamination Control
  - Yield Learning
  - Yield Model and Defect Budgets
- Defect Budget Survey
- Outlook

Chapter Outline

- Scope and topics
  - improvement from R&D yield level to mature yield
  - limited to front-end processing
  - defect detection
  - yield learning/fast ramp



Phase 1: R&D yield level → **YE** → **speed up yield detracting identification**
Phase 2: ramp-up yield level → **YE** → **Faster ramp up**
Phase 3: mature yield level → YE → **Higher yield levels!**

Organization of the Chapter

- **Chair:** Lothar Pfitzner (Fraunhofer IISB) **Co-Chair:** Dilip Patel (Intel assignee to SEMATECH)

- Difficult Challenges
    - Table 109
- Technology Requirements and Potential Solutions
  - Yield Model and Defect Budget (YMDB)
    - Chair: Sumio Kuwabara (NEC) - Japan
    - Table 111 a – Near-term, Table 111 b – Long-term (MPU)
    - Table 112 a – Near-term, Table 112 b – Long-term (DRAM)
  - Defect Detection and Characterization (DDC)
    - Chair: Ines Thurner (Qimonda) - Europe
    - Table 113 a – Near-term, Table 113 b – Long-term
  - Yield Learning (YL)
    - Chair: Tings Wang (Promos Tech) - Taiwan
    - Table 114 a – Near-term, Table 114 b – Long-term
  - Wafer Environment Contamination Control (WECC) – USA
    - Chair: Kevin Pate (Intel) - USA
    - Table 115 a – Near-term, Table 115 b – Long-term

2005 Revision of Key Challenges

- **The Yield Enhancement community is challenged by the following topics:**
  - ***Signal to Noise Ratio –*** it is a challenge to find small but yield relevant defects under a vast amount of nuisance, false defects.
  - ***High Throughput Logic Diagnosis Capability -*** identification and tackling of systematic yield loss mechanisms.
  - ***Detection of Multiple Killer Defect Types -*** and simultaneous differentiation at high capture rates, low cost of ownership and throughput.
  - ***High-Aspect-Ratio Inspection -*** need for high-speed and cost-effective high aspect ratio inspection tools remains as the work around using e-beam inspection does not at all meet requirement for throughput and low cost.
  - ***Process Stability vs. Absolute Contamination Level Including the Correlation to Yield -*** data, test structures, and methods are needed for correlating process fluid contamination types and levels to yield and determine required control limits.
  - ***In - line Defect Characterization and Analysis –*** as an alternative to EDX analysis systems [1]. The focus is on light elements, small amount of samples due to particle size and microanalysis
  - ***Wafer Edge and Bevel Control and Inspection -*** In order to find the root cause inspection of wafer edge, bevel and apex on front and backside is needed
  - ***Data Management and Test Structures for Rapid Yield Learning -*** to enable the rapid root-cause analysis of yield-limiting conditions
  - ***Development of Parametric Sensitive Yield Models -*** including new materials, (OPC) – optical proximity correction and considering the high complexity of integration.

NEW PROPOSAL:

- ***Variation of Critical Dimensions –*** how to monitor the variations of Critical Dimensions, how can we minimize the CD variations, how do we specify the tolerances and how can we get immunity/robustness for the variations.

2005 Revision at a Glance

- **Defect Detection and Characterization:**
  - Identification of bevel and edge inspection for yield impact
  - Extension of tables for specifications of bevel and edge inspection tools
- **Wafer Environment and Contamination Control:**
  - New approach: moving from the point of connection to the point of entry to the tool
  - New inputs from immersion lithography and new ALD and CVD precursors
  - Restructuring of the tables in a more process specific way
  - Emphasize the importance of process stability versus absolute contamination on yield
- **Yield Model and Defect Budget:**
  - Definition of new procedure for generation of tolerable defect budgets
  - Removal of defect target calculator

2005 YE ITWG Contributors

- Europe
  - **Ines Thurner (Qimonda)**
  - **Lothar Pfitzner (FhG-IISB)**
  - **Andreas Neuber (M+W Zander)**
  - **Andreas Nutsch (FhG-IISB)**
  - Eric Rouchouze (STM)
  - François Finck (STM)
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  - Dirk de-Vries (Crolles 2/ Philips)
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  - Mart Graef (Philips)
  - Dieter Rathei (D R Yield)
  - Christoph Hocke (Infineon)
  - Hubert Winzig (Infineon)
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  - CS Yang (Winbond)
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  - D.H. Cho (Samsung)
  - Sang Kyun Park (MagnaChip)

Thank you very much!

- United States
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  - Allyson Hartzell (Exponent)
  - Bart Tillotson (Fuji-Arch)
  - Billy Jones (Infineon)
  - Bob McDonald (Metara)
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  - Chris Muller (Purafil)
  - Dan Rodier (IBM)
  - Dan Wilcox (AMD)
  - David Roberts (Air Products)
  - Diane Dougherty (Chemtrace)
  - Ed Terrell (PMS)
  - Hank Walker (Texas A&M)
  - James McAndrew (Air Liquide)
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  - Jeff Chapman (IBM)
  - Jian Wei (Mykrolis)
  - John DeGenova (TI)
  - John Kurowski (IBM)
  - John Rydzewski (Intel)
  - Keith Kerwin (TI)
  - Ken Tobin (ORNL)
  - Kristen Cavicchi (BOCE)
  - Mansour Moinpour (Chemtrace)
  - Mark Camenzind (Air Liquide)
  - Mark Crockett (Applied Materials)
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  - Rob Henderson (Yield Service)
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  - Robert McDonald (Metara)
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  - Steven Hues (Freescale)
  - Tony Schleisman (Air Liquide)
  - Terry Stange (Ultra Analytics)
  - Tracey Boswell (Sematech)
  - Val Stradzs (Intel)
  - Victor Chia (KLA Tencor)
  - William Moore (IBM)

Defect Detection and Characterization

- 2005 revision highlights
  - Add new table for bevel inspection
  - Update of tool specification table
    - CoO definition
    - ADC lower requirements on number of classes but higher requirements on accuracy and purity
  - Alignment of edge exclusion defined by Factory Integration
  - Backside particle contamination

- future objectives
  - Add macro inspection table
  - Specifications for 90 % and 50 % capture rate
  - HARI specification: verify next year for application of DUV solutions

Defect Detection and Characterization

General definition of bevel inspection tools

- Definition of inspected area:
  - basically all the area the other inspection tools can not cover
  - top and bottom bevel, apex but also coverage of edge exclusion
- Review capability :
  - necessary: optical and/or SEM
  - Standardized Defect Data Set (SDDS): coordinate, angular information and image from tool

Wafer Environment Contamination Control

- 2005 revision highlights
  - Update litho requirements
  - Thin film precursor table
  - Work on particle metrology
  - Process area specific Airborne Molecular Contamination requirements
  - Increased focus on reticle areas
  - Updated critical ion lists
- Future objectives
  - General
    - Investigation of deposition models
    - Address point of use versus point of connection requirements
    - CVD/ALD Precursors and their impact on yield
    - Yield impact of SOI and strained silicon
  - Wafer environment control and airborne molecular contamination
    - Focus areas: litho, metal & contact (Al, Cu, CoSi2), gate, reticle handling & storage, organics, dopants, surface molecular contamination
    - Measuring methods

Wafer Environment Contamination Control

- Future objectives
  - Ultrapure water
    - Criticality of anions, ammonia and urea for the process
    - Specific requirements of immersion lithography
    - UPW contribution to water spotting
    - Dissolved oxygen specification relaxation
    - Specification of organic contamination contributors
  - Process chemicals:
    - Clarification of critical ions and other specifications by specific chemicals
    - Identification of newer precursors specification
    - Particle specification sensitivity
    - Requirements for slurry particles, CMP rinse chems particles & metals, and plating chems particles
  - Bulk and specialty gases
    - Identify process capabilities
    - Identify more detailed specialty gas requirements, e.g. dopant levels
    - Measuring methods for specific contaminants

Yield Learning

- 2005 revision highlights
  - Breakdown of YL phases into three phases
    - Development phase: 0% - 30%
    - Ramp-up phase: 30% - 70%
    - Mature yield (maintain and improve) in production: >70%
- future objectives
  - Extend YE scope to final test
  - Yield learning by wafer-out volume
  - Tools for yield analysis – EFA, PFA
  - Reticle defect inspection and prevention
  - In-line metrology to yield correlation
  - DFM and DFT methodology
  - Adapt tables to volume dependent yield learning (in contrast to time dependant yield learning cycles).

Yield Model and Defect Budget

- 2005 revision highlights
  - Simplification and improvement of defect budget survey
  - Modification of the subchapter outline (skip defect budget calculator)
  - New survey during 2005 → update of numbers for 2006
- future objectives
  - Evaluation of new defect budget survey.
  - Discussion on extended yield models adapted to mature yield with special focus on models for systematic yield loss.

Defect Budget Survey

Assumption: yield loss due to particulate contamination

Scope

- International survey of data for major product technology @ specific technology generation
- Defect budget of equipment = Control limits of particle per wafer pass (PWP) of equipment
- Status on defect budgets for current technology generation (e.g. DRAM; MPU; Logic)
- Interpolation of data for future technology generation with simple model

Defect Budget Survey

Benefit

- IC companies: present status / benchmarking
  - Comparison of own standard with industrial standard and benchmark
  - Generation of reliable and realistic values within ITRS industrial standard

- IC companies and tool vendors: definition of tool specifications

Defect Budget Survey

Comparison and Interpolation of Defect Densities

Defect Density [#/cm²]

10

1

0,1

0,01

1 10 100 1000

Defect Size [nm]

— 2004
— 2007
— 2010
— 2013

Data from survey of equipment particle control limits at control size and subsequent comparison of particle control sizes via scaling to common defect size using $1/x^2$
→ Current status

Interpolation towards future using reduction factor ½ for defect density for each technology generation
→ Prediction of tolerable defect budgets

$$D_{scaled} = D_{control}^{@x_{controlsize}} \cdot \left(\frac{x_{controlsize}}{x_{scale}} \right)^2$$

Outlook

- **Improvement of the Yield Enhancement chapter**
  - Highly active subchapters DDC and WECC → improve input to YL and DB&YM (acquisition of members in Asia)
  - Adjust outline and content of the chapter and make necessary changes to reflect current/future needs
  - Back to basics – ensure we have enough and necessary players and resources including academia/supplier participation
- **Yield Model for ITRS (start of new activity)**
  - Definition of defect distribution models
  - Match the defect budgets of subchapters
  - Propose a specific working group
    - For a definition phase
    - For appropriate YMs
    - Need for strong collaboration with Device Manufacturers