

# Metrology Roadmap 7-06

## Europe

**Bart Rijpers (ASML)**  
**Marco van der Haar (Panalytical)**  
**Thomas Hingst (Infineon)**  
**Dick Verkleij (FEI- Philips)**  
**Mauro Vasconi (ST)**

## Japan

**Eiichi Kawamura (Fujitsu)**  
**Yuichiro Yamazaki (Toshiba)**  
**Masahiko Ikeno (Hitachi High-Technologies)**

## Korea

**Soobok Chin (Samsung)**  
**Hyun Mo Cho (KRISS)**  
**Chul Hong Kim (Hynix)**  
**Jae Sam Kim (Nanometrics)**

## Taiwan

**Jia-Rui Hu (ProMOS)**  
**J.H. Sheih (TSMC)**

## US

<b>Steve Knight (NIST)</b>	<b>Andras Vladar (NIST)</b>
<b>Alain Diebold (SEMATECH)</b>	<b>John Allgair (ISMI)</b>
<b>Ingrid Peterson (Applied Materials)</b>	<b>George Orji (NIST)</b>
<b>Susie Yang (Applied Materials)</b>	<b>Ben Bunday (IMSI)</b>
<b>Andy Hegedus (Exponent)</b>	<b>Meredith Beebe (Technos)</b>
<b>Dick Hockett (Evans Analytical Group)</b>	



# Metrology Roadmap

## 4-06

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# AGENDA

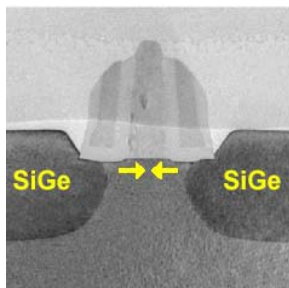
- 2006 Changes
- Litho Metrology
- FEP Metrology
- Interconnect Metrology
- ERD/ERM
- Conclusions



# Transistor Evolution

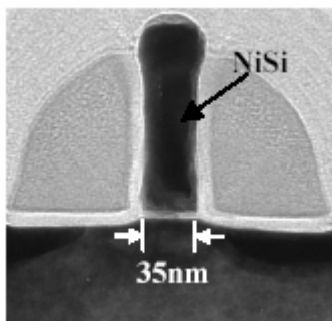
Future  
15 years  
Non-classical CMOS

Today  
65 nm Node

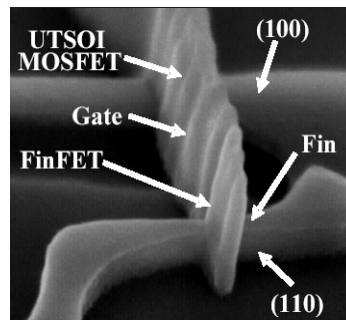


Strain  
Enhanced Mobility

Tomorrow

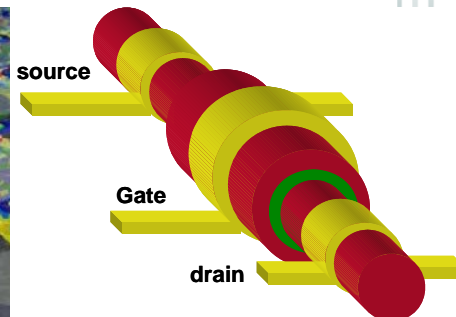
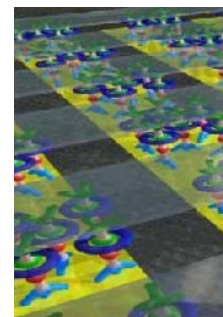


New Materials



CMOS  
pMOS FINFET

Beyond CMOS



Molecular Switches ?  
Nanowire Transistor ?

# 2006 New Areas

## FACTORY Issues

- As Clean Rooms move to FOUPs and relax particle class do we need to spec humidity and temperature control ranges across fab for metrology?? Can we develop a correction algorithm instead???

## Lithography Metrology

- Will a new method be needed for CD beyond the 32 nm Generation?
- Can CD-SEM meet 32 nm dense line with matching
- In-line TEM Sampling and cross-sectional metrology by Dual column FIB
- Total Measurement Uncertainty vs Total Measurement Reproducibility – Sampling Plan Discussion for 2007 ITRS
- Calibration of ellipsometers and reflectometers at 193 nm



# 2006 New Areas

## FEP Metrology

- Local strain measurement in the channel
- 3D Dopant Profiling for USJ: New requirements such as new structures (MUGFETs) and new processes (dopant anneals)
- 3D structure measurements (profile, roughness) (also in **Interconnect Metrology**)
- Metrology for SiGe, Ge, and III-V Channels for transistors – epi layer quality

## Interconnect Metrology

- Metrology for “Next Gen Interconnect;” (Optical, CNT, rf???)
- Metrology for wet chemical control (plating, cleans...)

## ERM/ERD

- TEM and HR-XRD – more automated and TEM + X-ray Tomography
- Metrology to characterize nano-structure composition and properties



# 2006 ITRS Changes ?

	2005	2007	2010	2013	2016	2018	2020	
<b>Technology Node</b>	<b>80 nm</b>	<b>65 nm</b>	<b>45 nm</b>	<b>32 nm</b>	<b>22 nm</b>	<b>18nm</b>	<b>14 nm</b>	<b>Driver</b>
MPU ½ Pitch (nm)	85	67	48	34	24	19	15	
MPU Printed Gate Length (nm)	54	42	30	21	15	12	9	
MPU Physical Gate Length (nm)	32	25	18	13	9	7	6	
<b>Lithography Metrology</b>								
Printed Gate CD Control (nm)								
Allowed Litho Variance = 3/4 Total Variance of physical gate length	3.3	2.6	1.9	1.4	0.9	0.7	0.6	MPU
Wafer CD Tool 3σ Precision P/T=0.2 for Printed and Physical Isolated Lines	0.67	0.52	0.37	0.27	0.19	0.15	0.12	MPU
Wafer CD metrology tool precision (nm) * ( P/T=.2 for dense lines )	2.0	1.6	1.1	0.78	0.54	0.44	0.34	MPU
Line Width Roughness (nm) <8% of CD	2.6	2.0	1.4	1.0	0.7	0.6	0.5	MPU
Precision for LWR	0.5	0.4	0.3	0.2	0.1	0.1	0.1	c
Overlay Control (nm) (mean +3σ )	16.0	13.0	9.0	6.0	4.4	3.6	2.8	
Overlay Metrology Precision (nm) P/T=0.1	1.6	1.3	0.9	0.6	0.4	0.4	0.3	
<b>Front End Processes Metrology</b>								
High Performance Logic EOT equivalent oxide thickness (EOT) nm	1.2	1.1	0.65	0.5	0.5	0.5	0.5	MPU
Logic Dielectric EOT Precision 3σ (nm)	0.0048	0.0044	0.0026	0.002	0.002	0.002	0.002	MPU
<b>Interconnect Metrology</b>								
Barrier layer thick (nm)	7.3	5.2	3.3	2.4	1.7	1.3	1.1	MPU
Void Size for 1% Voiding in Cu Lines	8.5	6.7	4.8	3.4	2.4	1.9		MPU
Detection of Killer Pores at (nm) size	8.5	6.7	4.8	3.4	2.4	1.9		MPU



# 2006 Activities

- **Dick Verkleij** – add dual column FIB to Materials \$ Cont. Char section
- **Bart Rijpers** – work on Litho Metrology section for TMU vs TTR & check CD precision coloring for tool matching
- **Thomas Hingst** – draft standard terms for In-Line/Off-Line/In-Situ
- **STRJ-WG11** to send New Requirements lines for Stress/Dopant Profile
- **Everyone** to obtain access to the ITRS Web site
- **Steve Knight & Thomas Hingst** – define standard for references for n an k calibrations at 193 nm for lithography modeling
- **Ikeno-san** - report in LER/LWR measurement definition from SEMI Micropatterning Committee Task Force

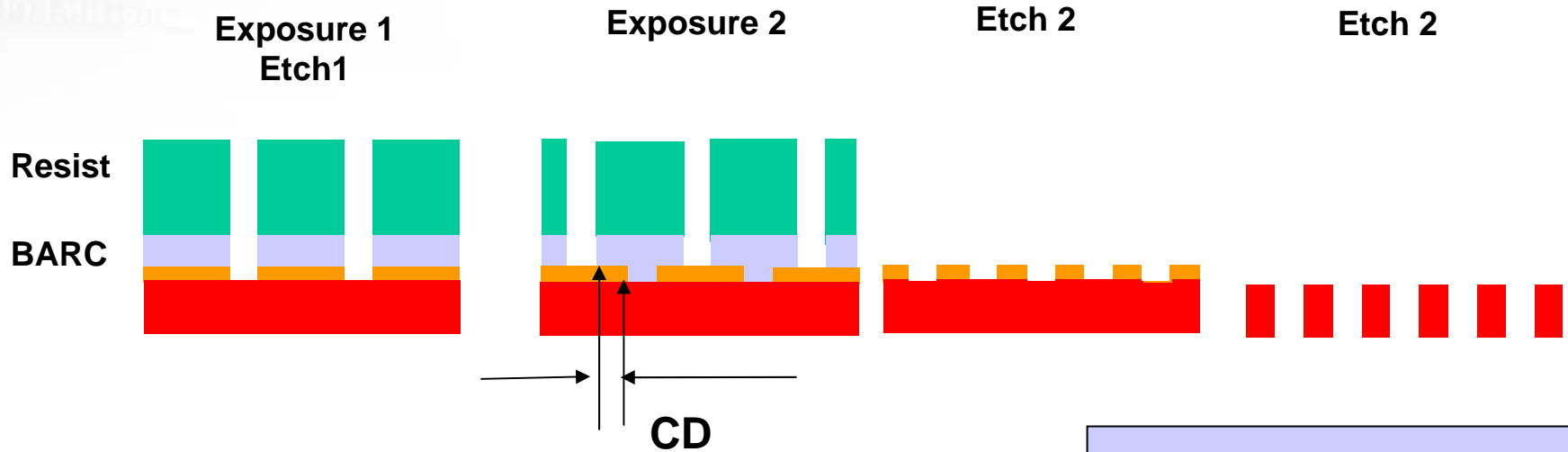


# Changes to Litho Metrology

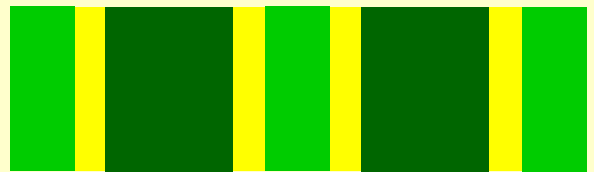
- **CD capability for single tool met(?) by single tool to 32 nm for Dense lines**
- **Box in Box Overlay structures too large and will be design ruled out soon – Litho asks if overlay metrology will meet requirements associated with smaller targets?**
- **EUV Reticle flatness at 32 nm  $\frac{1}{2}$  pitch needs to be measured on electrostatic chuck. Mask must be flat to within 32nm peak to valley**



# Dual patterning (two exposures with etch steps) overlay control



Litho 2 = Litho1  
 ■ Equal lines



Litho 2 > Litho1  
 ■ Thinner lines  
 ■ Pairs of lines (AB:AB)  
 ■ Across area CD's identical

Overlay error

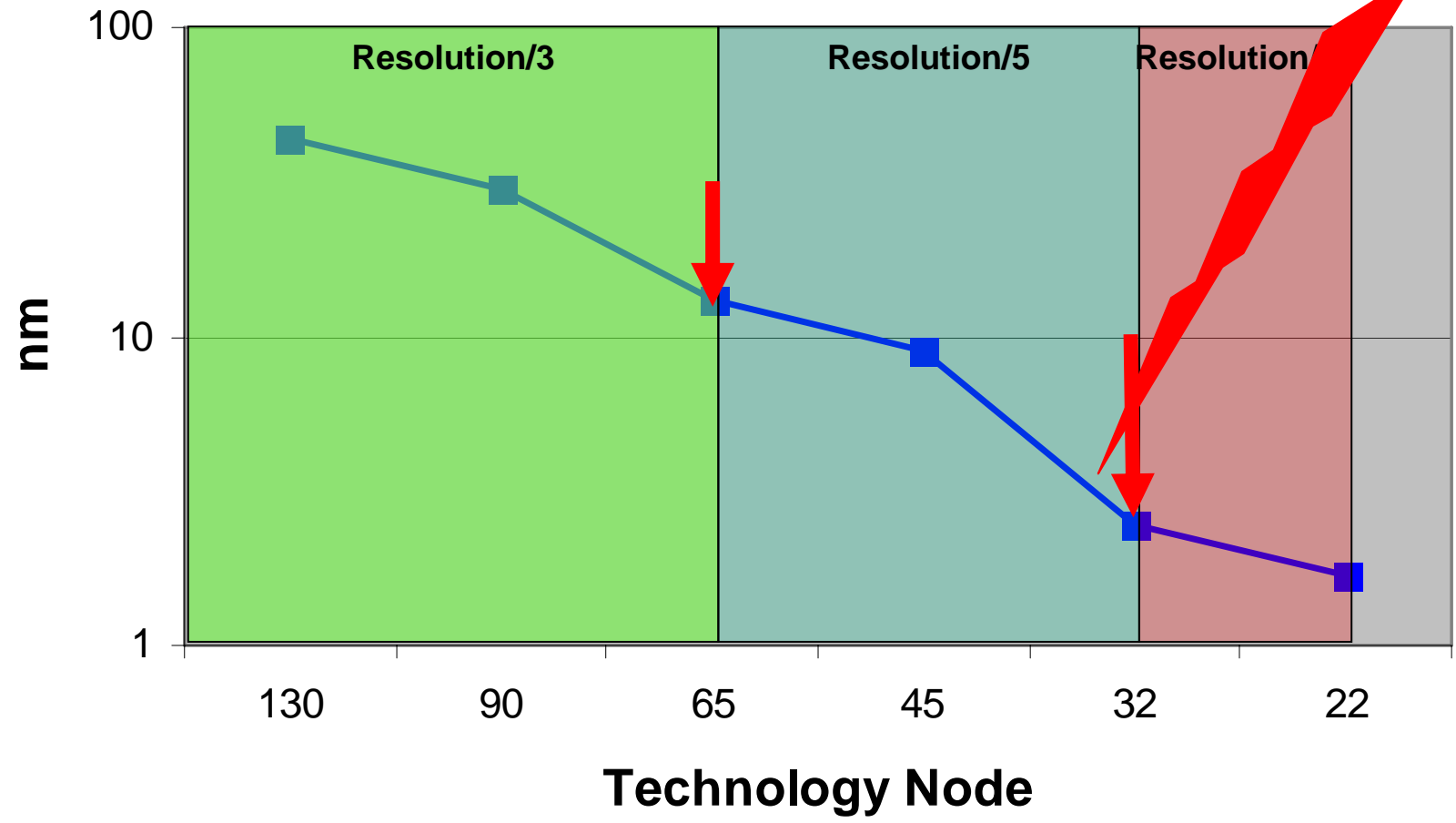
- Different line width alternating

# Overlay Requirements

## *As a function of Technology Node*

**Double  
Patterning**

Resolution = DRAM 1/2 pitch node



# LER/LWR Activities

- **SEMI – Japan Committee on LER/LWR standard measurement method**
  - SEMI Japan
  - NIST
  - ISMI
  - Global Participation



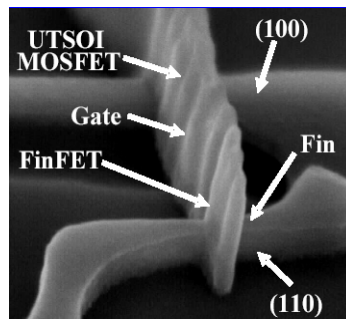
# FEP Metrology:

## Expanded Emphasis on Areas beyond High k

- Increase in Mobility by using local stressing of transistors –  
**FEP Call for local stress metrology in the channel**
- Metal Gates increasingly important – routine Work Function measurement is a new requirement.
- New transistor designs are advancing rapidly.  
**Example: FIN-FETs require 3D metrology**
- **Rapid annealing at 45/32 nm Generation will drive new dopant metrology needs & characterization of active carriers in transistors.**
- Thickness and other metrology for PD and FD-SOI, & sSOI, & GeOI
- 3D Crystal Defect mapping including mapping of patterned wafers with enhanced mobility layers or for substrates.

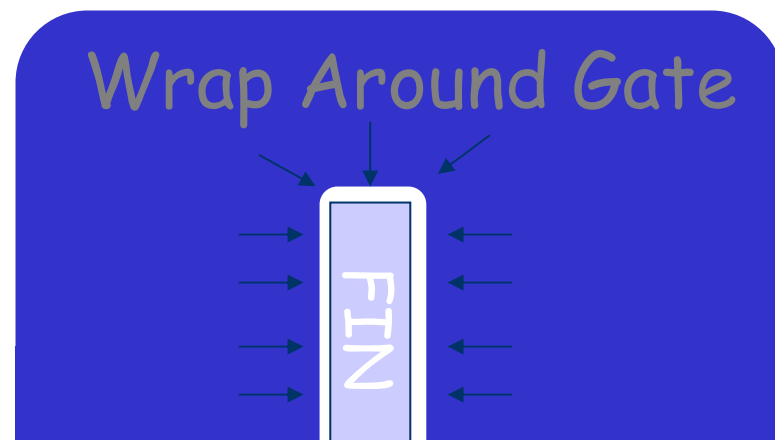
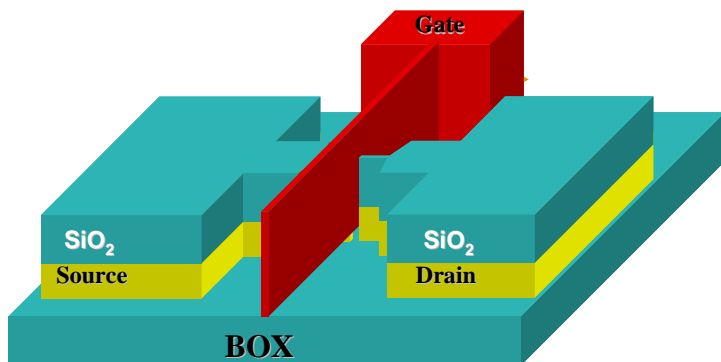


# Wrap Around Gate Metrology



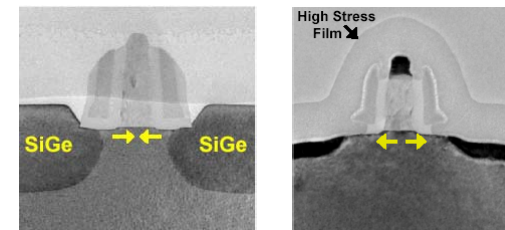
FINFET

Side Wall and Top Dielectric Thickness and Composition



# Stress Measurement from transistor to wafer

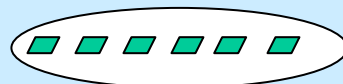
Nano-Raman and CBED



Transistor Level Stress

Micro-Raman, XRD, Photoreflectance Spectroscopy

  
Micro-Area Level Stress



Die Level Stress

Die level flatness  
Laser Interferometry  
Coherent Gradient Sensing

  
Wafer Bow

Laser Interferometry,  
Coherent Gradient Sensing



# Correlation to Test Structures

**will not be easy**

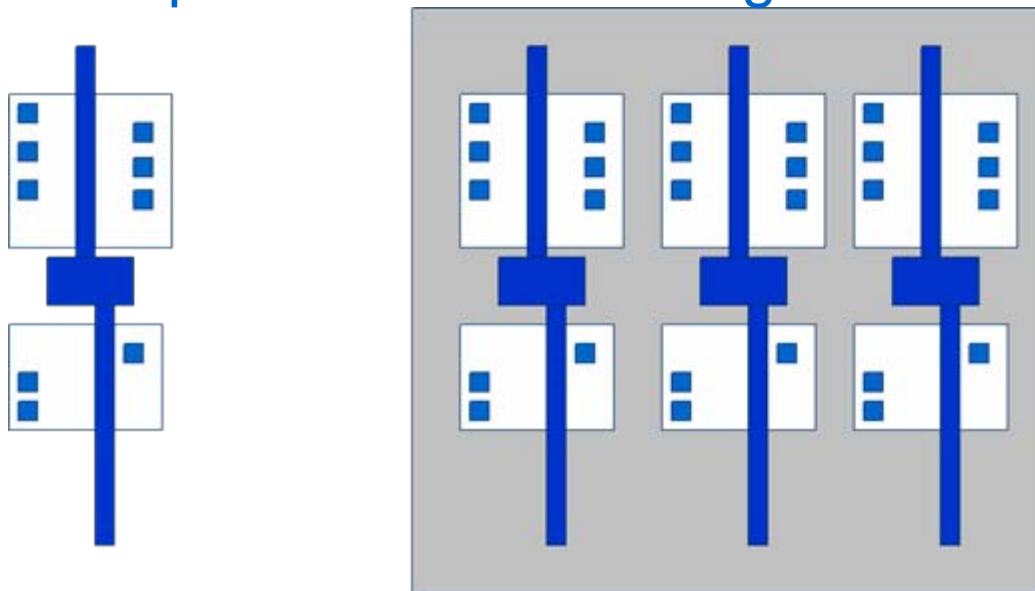
Differences in PMOS and NMOS mobility: iso vs Dense

pMOS difference 14%

nMOS difference 8%

nMOS to pMOS difference ratio 22%

Much more complicated for real design



Fichtner –at 2005 Nano Transistor Conference

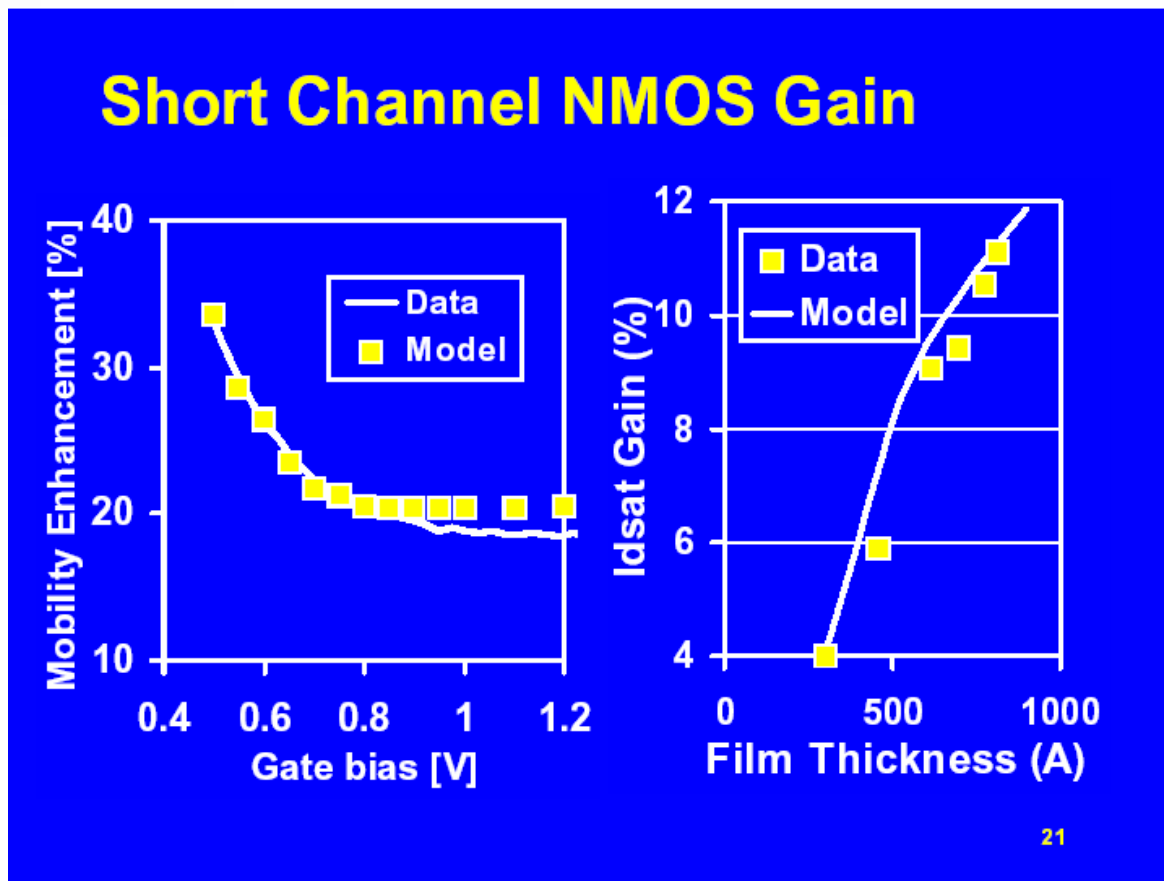


International Technology Roadmap for Semiconductors

DRAFT – Work In Progress - NOT FOR PUBLICATION 12 July 2006

Trend : Use Modeling to connect what you can measure with what you need to know

## Example: Metrology of Strained Channel Devices



MD Giles, et. al., VLSI Symposium 2004



International Technology Roadmap for Semiconductors

DRAFT - Work In Progress - NOT FOR PUBLICATION 12 July 2006

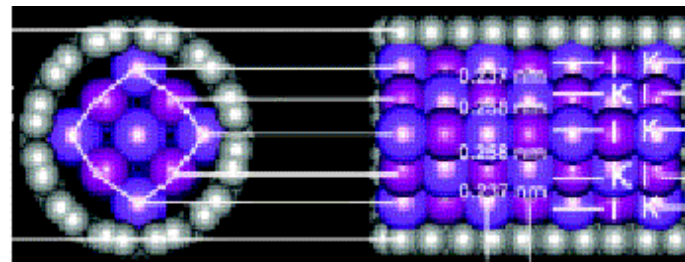
# 2006 Interconnect Activities

- **Point of Use Metrology for Plating Bath Electrolyte and Additives (Surface inhibitors, etc)**
- **Measurements of Sidewall barrier thickness and sidewall damage (compositional changes in low k) after etch remains a Major Gap - It will soon also be a Gap for FEP Metrology**
- **Porous low k is being overshadowed by the need to lower k value of barrier layer and etch stops for 45/32 nm node.**
- **There are no manufacturing solutions for void detection in copper lines and killer pores in low k**



# 2006 Interconnect Activities

- **Metrology for alternative solutions for upper level metal interconnect needs definition.**
  - 3D Interconnect
  - Optical
  - Carbon Nanotubes
  - Etc.
- **Metrology is needed for 3D Integration**
  - Alignment of chips for stacking – wafer level integration
  - Defects in bonding
  - Damage to metal layers
  - Defects in vias between wafers
  - Thickness of Thinned Wafers
- **Optical Interconnect Metrology**
  - Waveguide Properties
  - Sources & Detectors
- **Metrology of Carbon Nanotubes**
  - Resistivity
  - Chirality
  - Defects



# ERD and ERM

## Aberration corrected TEM/STEM needed for nano-electronics

- **Metrology to Characterize Nanostructure, Composition and Properties.**
- **Latest TEM and STEM results show improved imaging for sub 0.1 nm beams.**
- **Simulation of measurement tool is necessary for image interpretation.**
- **We have not reached the limit where improving beam diameter does not improve imaging**
- **Nanowires and nanotubes serve as ideal systems to test theoretical and experimental understanding of beam propagation and image formation**



# Dielectric Function of nanowires

Zhao, et al,  
PRL 92, 2004,  
pp 236805

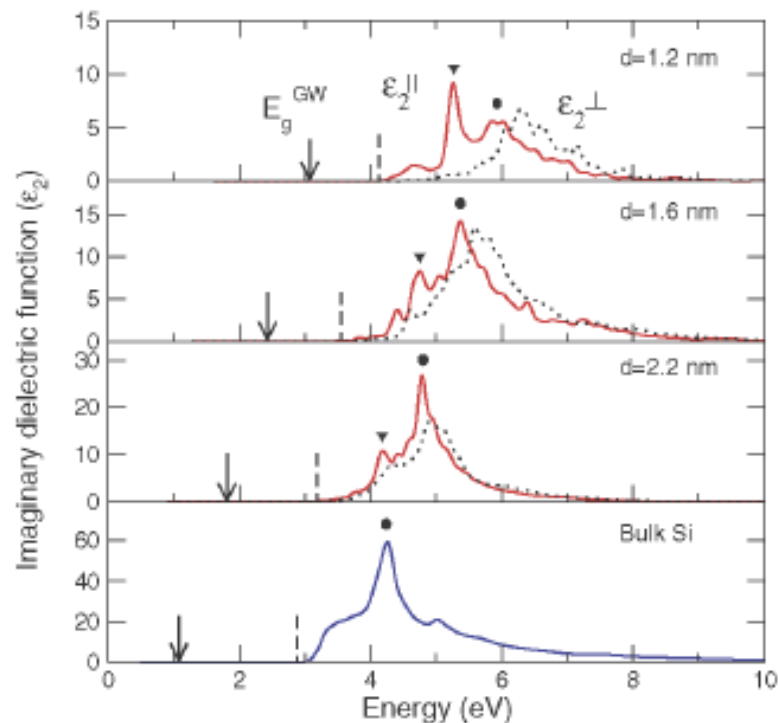


FIG. 4 (color online). Imaginary dielectric functions  $\epsilon_2(\omega)$  polarized along the  $z$  direction [ $\epsilon_2^{\parallel}(\omega)$ , solid lines] and in the  $xy$  plane [ $\epsilon_2^{\perp}(\omega)$ , dotted lines], for silicon [110] wires with  $d = 1.2, 1.6,$  and  $2.2$  nm, respectively. Shown in the bottom panel is  $\epsilon_2(\omega)$  for bulk  $c$ -Si. The dielectric functions are calculated with the scissor operator to fix the band gap at the  $GW$  values ( $E_g^{GW}$ ) and the energy zero is set at the top of the valence band. The arrows and vertical dashed lines mark  $E_g^{GW}$  and the optical absorption edges, respectively. The black dots indicate the original absorption peak in bulk Si, and the inverted triangles show the new peaks developed in nanowires.

# Conclusions

- **CD Measurement improvements show a path to the 32 nm Node**
- **Propose definition for LWR and including LER**
- **Transistor channel engineering requires Stress and Mobility Measurement**
- **Interconnect requires Sidewall Measurements for barrier/seed and low  $\kappa$  trench**
- **ERM and ERD require both improved imaging (such as aberration corrected TEM) and image simulation**

