2006 ITRS Public Conference

Emerging Research Devices

San Francisco, CA
San Francisco Marriott Hotel
July 12, 2006

Jim Hutchby – SRC
Mike Garner – Intel

ITRS

Emerging Research Devices Working Group

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2006 ERM Participants

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Victor Zhirnov	SRC

Expect the Team to Grow Through 2006

Charter of ERD Chapter

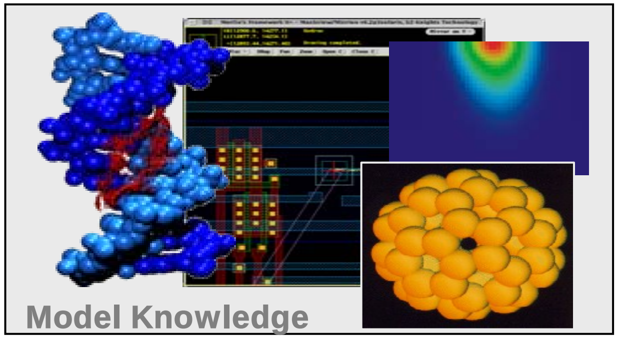
Develop an Emerging Research Devices chapter to –

- ☐ Critically assess currently proposed approaches to Information Processing beyond ultimate CMOS
- ☐ Identify promising new approaches to Information Processing technology to be implemented by 2020

Offer substantive guidance to –

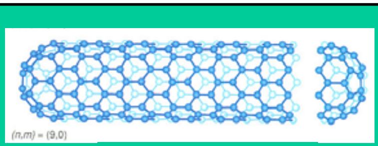
- ☐ Global research community
- ☐ Relevant government agencies
- ☐ Technology managers
- ☐ Suppliers

Scope of Emerging Research Devices 2006/7

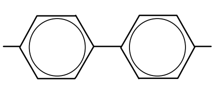


New Materials

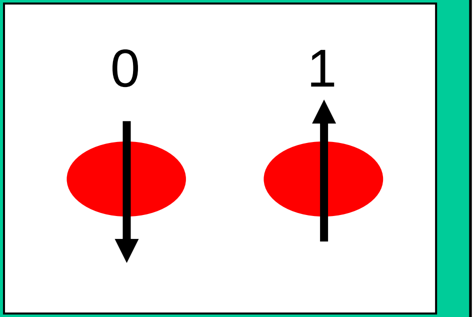
New Memory and Logic Technologies



Nanotubes



Molecular devices



Spin states

New Architecture Technologies

Emerging Information Processing Concepts

What are we looking for?

- **Required characteristics:**
  - **Scalability**
  - **Performance**
  - **Energy efficiency**
  - **Gain**
  - **Operational reliability**
  - **Room temp. operation**
- **Preferred approach:**
  - **CMOS process compatibility**
  - **CMOS architectural compatibility**

Alternative state variables (Beyond Charge State)

- **Spin state**
- **Molecular state**
- **Strongly coupled electron state**
- Phase state
- Quantum state
- Magnetic flux quanta
- Mechanical deformation
- Dipole orientation

“Guiding Principles”

Top Down Approach

Driven by Principles

- Not Based solely on Charge
- Non Thermal Equilibrium
- Novel Energy Transfer
- Nanoscale Thermal Management
- Sub-lithographic Mfg Process

? ?

- **Molecular-based system?**
- **Spin-based system?**
- **Strongly correlated electron state materials/devices**

2005 ITRS ERD: Table 57 Emerging Research Memory Devices Demonstrated and Projected Parameters

Transfer to PIDS

		Nano-floating Gate Memory	Engineered tunnel barrier Memory	Ferroelectric FET Memory	Insulator Resistance Change Memory	Polymer Memory	Molecular Memories
Cell Elements		1T	1T	1T	1T1R or 1R	1T1R or 1R	1T1R or 1R
Device Types		1 Nanocrystal 2 Direct tunneling	Graded insulator	FET with FE gate insulator	1 M-I-M 2 Solid Electrolyte 3 FE tunneling 4 FE Schottky diode 5 FE-I-FE	M-I-M(nc)-I-M	Bi-stable switch
Feature size F	Min. required	<65 nm	<65 nm	<65 nm	<65 nm	<65 nm	<65 nm
	Best projected	25 nm	10 nm [H]	22 nm [K]	5-10 nm [O]	5-10 nm	5-10 nm [AA]
Read Time	Min. required	<15 ns	<15 ns	<15 ns	<15 ns	<15 ns	<15 ns
	Best projected	2.5 ns	2.5 ns	2.5 ns	<10 ns	<10 ns	<10 ns [AA]
W/E time	Min. required	1 µs/10 ms	1 µs/10 ms	Application dependent	Application dependent	Application dependent	Application dependent
	Best projected	1 µs/10 ms	1 ns @ 9V[H]	2.5 ns [B]	<20 ns [P]	Not known	<40 ns [AA]
Retention Time	Min. required	>10 y	>10 y	>10 y	>10 y	>10 y	>10 y
	Best projected	>10 y	>10 y	>1y	>10 y	Not known	Not known
Write operating voltage (V)	Min. required	Application dependent	Application dependent	Application dependent	Application dependent	Application dependent	Application dependent
	Best projected	>3 V [F]	>3 V [F]	<0.9 V [K]	<0.5 V [U]	Not known	2 V [AE]
Write energy (J/bit)	Min. required	Application dependent	Application dependent	Application dependent	Application dependent	Application dependent	Application dependent
	Best projected	5E-16 [G]	5E-16 [G]	2E-15 [N]	1E-15 [V]	Not known	2E-14 [AA]
	Demonstrated	2E-15 [G]	Data not available	Data not available	5E-14 [P]	1E-13 [Z]	Data not available
Comments		A natural evolution of the floating gate memory		Potential for Non-destructive readout	Low read voltage presents a problem		

International Technology Roadmap for Semiconductors

⬜ > 20

🟩 >18 - 20

🟨 >16 - 18

🟥 ≤ 16

Critical Evaluation Memory

For each Technology Entry (e.g. 1D Structures, sum horizontally over the 8 Criteria
Max Sum = 24
Min Sum = 8

Memory Device Technologies (Potential)	*Scalability [A]*	*Performance [B]*	*Energy Efficiency [C]*	*OFF/ON "1"/"0" Ratio [D1]*	*Operational Reliability [E]*	*Operate Temp [F] ****	*CMOS Technological Compatibility [G]***	*CMOS Architectural Compatibility [H]**
Nano Floating Gate Memory	**2.5**	**2.5**	**2.5**	**2.5**	**2.2**	**2.7**	**2.7**	**3.0**
Engineered Tunnel Barrier Memory	**2.2**	**2.3**	**2.3**	**2.3**	**2.4**	**2.8**	**2.8**	**3.0**
Ferroelectric FET Memory	**1.9**	**2.3**	**2.5**	**2.2**	**2.0**	**3.0**	**2.6**	**3.0**
Insulator Resistance Change Memory	**2.5**	**2.5**	**2.0**	**2.2**	**1.9**	**2.8**	**2.6**	**2.8**
Polymer Memory	**2.1**	**1.5**	**2.3**	**2.2**	**1.6**	**2.9**	**2.3**	**2.5**
Molecular Memory	**2.3**	**1.5**	**2.4**	**1.6**	**1.4**	**2.6**	**1.9**	**2.3**

Table 57a: Capacitance-based memory technologies

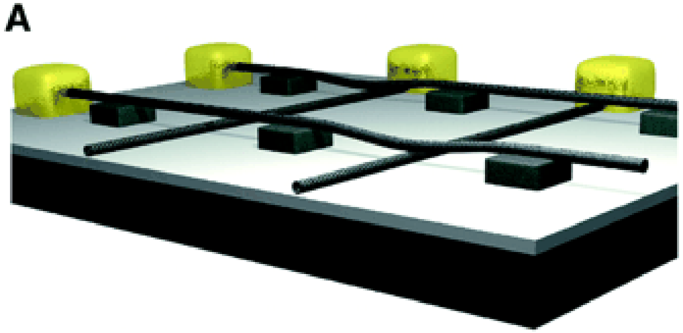
	Engineered tunnel barrier Memory	Ferroelectric FET Memory
Storage Mechanism	Charge on floating gate	Remnant polarization on a ferroelectric gate dielectric
Cell Elements	1T	1T
Device Types	Graded insulator	FET with FE gate insulator

Table 57b: Resistence-based memory technologies

	Nanomechanical memory	Unipolar Fuse/Antifuse Memory	Solid Electrolyte Memory	Ferroelectric resistive switching	Polymer Memory	Molecular Memory
Storage Mechanism	electrostatically-controlled bi-stable mechanical switch	Not known	Redox electrochemical reaction	Multiple mechanisms	Not known	Not known
Cell Elements	1T1R or 1R	1T1R or 1R	1T1R or 1R	1T1R or 1R	1T1R or 1R	1T1R or 1R
Device Types	electrostatically-controlled bi-stable mechanical switch	M-I-M, e.g. Pt/NiO/Pt	Solid Electrolyte, e.g. Ag/(GeSe$_x$+AgSe$_2$)/Pt	1) FE tunnel junction 2) FE Schottky diode 3) FE semiconductor double layer	M-I-M (nc)-I-M	Bi-stable switch

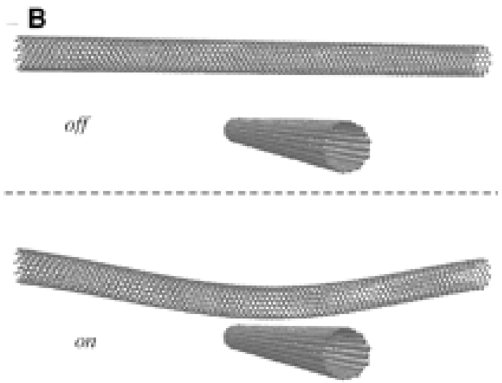
Example – CNT cross-bar memory

Rueckes T. et al., SCIENCE 289 (5476): 94-97 JUL 7 2000



Concept

Moving Atoms



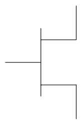
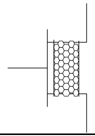
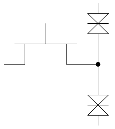
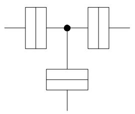
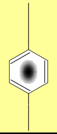
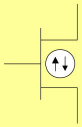
- Each memory element is based on suspended crossed carbon nanotubes.
- Cross-bar array of CNT forms mechanically bi-stable, electrostatically-switchable device elements at each cross point.
- The memory state is read out as the junction resistance.

Expectations: n=10^{12} bits/cm^2, f=100 GHz

Memory Technologies for 2007 new ERD Chapter

- Numerical data will be updated
- We will have two tables for Emerging Research Memory Technology Entries:
  - Capacitance-based memory technologies
  - Resistance-based technologies.
- Put nanomechanical memory into the new tables
- Transfer Nanofloating Gate Entry to PIDS/Transition Table.

2005 ITRS ERD: Table 59 *Emerging Research Logic Devices* Demonstrated and Projected Parameters

Device								
		FET [B]	*1D structures*	*Resonant Tunneling Devices*	*SET*	*Molecular*	*Ferromagnetic logic*	*Spin transistor*
Types		*Si CMOS*	*CNT FET* *NW FET* *NW hetero-structures* *Crossbar nanostructure*	*RTD-FET* *RTT*	*SET*	*Crossbar latch* *Molecular transistor* *Molecular QCA*	*Moving domain wall* *M: QCA*	*Spin transistor*
Supported Architectures		*Conventional*	*Conventional and Cross-bar*	*Conventional and CNN*	*CNN*	*Cross-bar and QCA*	*CNN Reconfigure logic and QCA*	*Conventional*
Cell Size (spatial pitch)	*Projected*	100 nm	100 nm [C]	100 nm [C]	40 nm [L]	10 nm [Q]	140 nm [U]	100 nm [C]
	Demonstrated	590 nm	~1.5 μm [D]	3μm [H]	~700 nm [M]	~2μm [R]	250 nm [V, W]	100 μm [X]
Density (device/cm^2)	*Projected*	1E10	4.5E9	4.5E9	6E10	1E12	5E9	4.5E9
	Demonstrated	2.8E8	4E7	1E7	2E8	2E7	1.6E9	1E4
Switch Speed	*Projected*	12 THz	6.3 THz [E]	16 THz [I]	10 THz [M]	1 THz [S]	1 GHz [U]	40 GHz [Y]
	Demonstrated	1 THz	200 MHz [F]	700 GHz [J]	2 THz [N]	100 Hz [R]	30 Hz [V, W]	Not known
Circuit Speed	*Projected*	61 GHz	61 GHz [C]	61 GHz [C]	1 GHz [L]	1 GHz [Q]	10 MHz [U]	Not known
	Demonstrated	5.6 GHz	220 Hz [G]	10 GHz [Z]	1 MHz [F]	100 Hz [R]	30 Hz [V]	Not known
Switching Energy, J	*Projected*	3E-18	3E-18	>3E-18	1×10^{-18} [L] [>1.5×10^{-17}] [O]	5E-17 [T]	~1E-17 [V]	3E-18
	Demonstrated	1E-16	1E-11 [G]	1E-13 [K]	8×10^{-17} [P] [>1.3×10^{-14}] [O]	3E-7 [R]	6E-18 [W]	Not known
Binary Throughput, GBit/ns/cm^2	*Projected*	238	238 [C]	238 [C]	10	1000	5E-2	Not known
	Demonstrated	1.6	1E-8	0.1	2E-4	2E-9	5E-8	Not known
Operational Temperature		RT	RT	4.2 – 300 K	20 K [L]	RT	RT	RT
Materials System		Si	CNT, Si, Ge, III-V, In_2O_3, ZnO, TiO_2, SiC,	III-V Si-Ge	III-V Si	Organic molecules	Ferromagnetic alloys	Si, III-V, complex metals oxides

Sub-Categorize Molecular and Spin

> 20

🟨 >16 - 18

🟩 >18 - 20

🟥 ≤ 16

Critical Evaluation Logic

For each Technology Entry (e.g. 1D Structures, sum horizontally over the 8 Criteria
Max Sum = 24
Min Sum = 8

Logic Device Technologies (Potential)	*Scalability [A]*	*Performance [B]*	*Energy Efficiency [C]*	*Gain [D2]*	*Operational Reliability [E]*	*Room Temp Operation [F] ****	*CMOS Technological Compatibility [G]***	*CMOS Architectural Compatibility [H]**
1D Structures (CNTs & NWs)	**2.4**	**2.5**	**2.3**	**2.3**	**2.1**	**2.8**	**2.3**	**2.8**
Resonant Tunneling Devices	**1.5**	**2.2**	**2.1**	**1.7**	**1.7**	**2.5**	**2.0**	**2.0**
SETs	**1.9**	**1.5**	**2.6**	**1.4**	**1.2**	**1.9**	**2.1**	**2.1**
Molecular Devices	**1.6**	**1.8**	**2.2**	**1.5**	**1.6**	**2.3**	**1.7**	**1.8**
Ferromagnetic Devices	**1.4**	**1.3**	**1.9**	**1.5**	**2.0**	**2.5**	**1.7**	**1.7**
Spin Transistor	**2.2**	**1.3**	**2.4**	**1.2**	**1.2**	**2.4**	**1.5**	**1.7**

Logic Technologies for 2007 new ERD Chapter

Logic Section: Considering reformulation of Emerging Research Logic Device Section to encourage high potential, but high risk approaches while maintaining Technology Entry evaluation function.

- Create subcategories for key Technology Entries (e.g. Spin & Molecular logic)
- Re-considering status of candidate Technology Entries (e.g. RSFQ Logic)
- Considering re-structuring Logic Section via Emerging Logic Workshop in September.

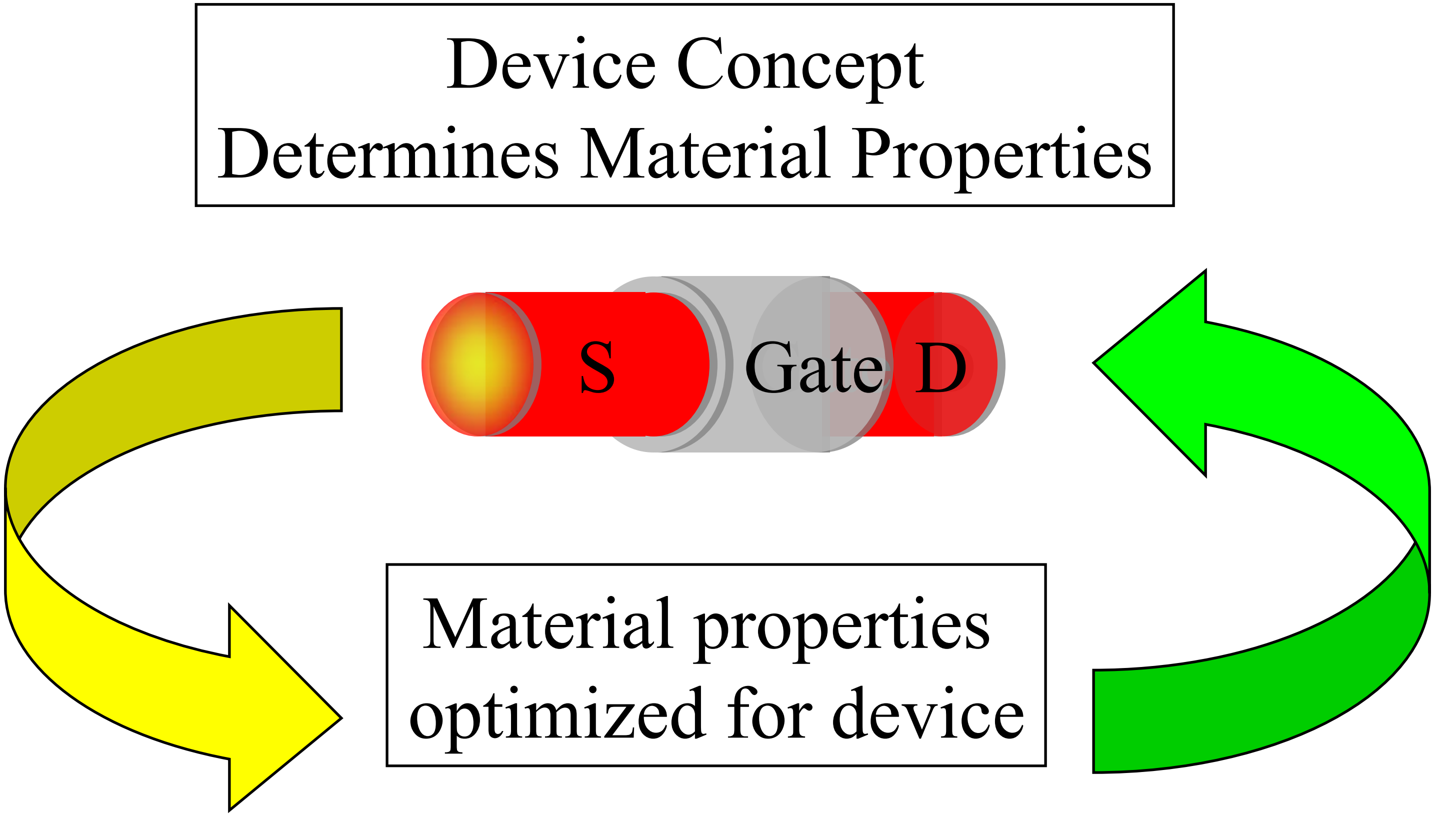
Messages

- Preparing for the 2007 re-write of the ERD Chapter.
  - Conducting four workshops in 2006 on Emerging Research Memory, Logic, Architectures and Materials (co-sponsored by ITRS and NSF)
  - Considering new Technology Entries and transfers to PIDS & FEP in 2007
- Materials Section: Spin out a new cross-cut chapter on Emerging Research Materials to include emerging research materials issues common to Devices, Litho, Interconnect and Packaging.
- Memory Section: Will add NEMS mechanical memory to section.
  - Divide Emerging Memory Tables into Resistive and Capacitive subcategories
  - Update section in 2007
- Logic Section: Considering reformulation of Logic Device Section to encourage high potential, but high risk approaches while maintaining Technology Entry evaluation function.
  - Create subcategories for key Technology Entries (e.g. Spin & Molecular logic)
  - Re-considering status of candidate Technology Entries (e.g. RSFQ Logic)
  - Considering re-structuring Logic Section via Emerging Logic Workshop in September.

2006 ERD/ERM Workshops

Workshop topic	Date	Location	Meeting	Specific technology entries
Emerging research memory devices	April 4 2006	Maastricht, Netherlands	ITRS Spring meeting	- Nanofloating gate memory - Single electron memory - Insulator Resistance Change Memory - Molecular Memory
Emerging research architectures	July 9 2006	San Francisco, CA, USA	Semicon West	- Fine-Grained Parallel Implementations in Cellular Arrays - Defect Tolerant Architectures - Biologically Inspired Architectures
Emerging research logic devices	Sept. 21 2006 (Bus.Mtg. Sept.22)	Montreux, Switzerland	ESSDERC	- 1-dimensional device structures - Resonant tunnel devices - Single-electron transistors - Molecular logic devices - Spin transistors
Emerging Research Materials	Nov. 15, 2006 (Bus.Mtg TBD)	San Francisco	AVS & APS	Metastable states and transition dynamics in Strongly correlated Electron State Materials -Energetics -Atomic level mechanisms -Transitions -Time scales -Interactions with external fields

Devices & Material Interplay



Device Concept
Determines Material Properties

Material properties
optimized for device

Critical Properties = Properties for Device Operation

Example: CNT DOS, Eg & m_{eff} α f(chirality & diameter)

Device Electrical Properties **Material Properties**