# PIDS Key Results and Issues

**Peter M. Zeitzoff for PIDS Technology Working Group**

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# PIDS Roster

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# Outline

- *Scope and Subcategories*
- **Non-Volatile Memory**
- **DRAM**
- **Logic**
- **Reliability**

# PIDS Scope

- PIDS = Process Integration, Devices, and Structures
- Main concerns
  - MOSFET, memory, and passive devices and structures
    - Device physical and electrical characteristics and requirements
  - Broad issues of device and circuit performance, density, and power dissipation, particularly as they drive overall technology requirements
  - Reliability

# PIDS Subcategories

- Logic
  - High-performance
  - Low-power (mobile applications)
- Memory
  - DRAM
  - Non-volatile memory (NVM)
- Reliability

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- **Scope and Subcategories**
- ***Non-Volatile Memory***
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# NAND Flash Roadmap: F

- F = half-pitch
  - DRAM: Metal 1
  - Flash: Poly
- <u>Flash memory scaling has pulled ahead of DRAM scaling</u>

| | 2005 | 2006 | 2007 | 2008 | 2009 | 2010 |
|---|---|---|---|---|---|---|
| 05 NAND Flash | 76 | 64 | 57 | 51 | 45 | 40 |
| 03 Flash Roadmap | 80 | 70 | 65 | 55 | 50 | 50 |
| 05 DRAM 1/2pitch | 80 | 70 | 65 | 57 | 50 | 45 |

| | 2011 | 2012 | 2013 | 2014 | 2015 | 2016 |
|---|---|---|---|---|---|---|
| 05 NAND/AND Flash | 36 | 32 | 28 | 25 | 23 | 20 |
| 03Flash Roadmap | | 39 | 35 | | 28 | |
| 03DRAM1/2pitch | | 36 | 32 | | 25 | |

# Non-Flash Memory (con’t.)

- **PCRAM**
  - **New in 2005 PIDS**
  - **For near term years, technology node similar to DRAM**
  - **Product introduction is uncertain**
- **2007: Will be evaluating transfer of devices from ERD chapter into PIDS**
  - **Probable route: to potential solutions first**
  - **Examples: nanocrystals, nitride trapping devices, etc.**

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- Scope and Subcategories
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- ***DRAM***
- Logic
- Reliability

# DRAM

- Scaling unchanged from 2003
  - DRAM half-pitch (F) : 3 year cycle
    - 65nm in 2007, 45 nm in 2010
- Other results
  - a=(cell area)/$F^2$: a=8 through 2007, a=6 thereafter
  - Array Area efficiency (% of chip area taken up by storage cells): 63% through 2007, 56% thereafter
  - STC storage node dielectric: the same as 2003 ITRS

# Scaling of DRAM Storage Dielectric

| Year | DRAM storage node cell dielectric: equivalent physical thickness, EOT nm | DRAM storage node capacitor voltage, V |
|---|---|---|
| 2005 | 1.8 | 1.5 |
| 2006 | 1.4 | 1.4 |
| 2007 | 1.1 | 1.3 |
| 2008 | 0.9 | 1.2 |
| 2009 | 0.8 | 1.1 |
| 2010 | 0.6 | 1.1 |
| 2011 | 0.6 | 1.1 |
| 2012 | 0.5 | 1 |
| 2013 | 0.5 | 1 |
| 2014 | 0.45 | 1 |
| 2015 | 0.4 | 0.9 |
| 2016 | 0.4 | 0.9 |
| 2017 | 0.3 | 0.7 |
| 2018 | 0.25 | 0.7 |
| 2019 | 0.2 | 0.7 |
| 2020 | 0.15 | 0.7 |



**Preliminary Results**

# Potential Solutions: DRAM

| | 2005 | 2006 | 2007 | 2008 | 2009 | 2010 | 2011 | 2012 | 2013 | 2014 | 2015 | 2016 | 2017 | 2018 | 2019 | 2020 | 2021 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DRAM 1/2 Pitch | | | 65nm | | | 45nm | | | 32nm | | | 22nm | | | 16nm | | |

**High-k Dialectric**

$Al_2O_3$ & $Ta_2O_5$, MIS structure (k ~ 10–25)

MIM Structures (k ~ 20–50)

New materials (k>50)

**Three dimensional array device**

**Emerging research memory devices**

Research Required | Development Underway | Qualification/Pre-Production | Continuous Improvement

This legend indicates the time during which research, development, and qualification/pre-production should be taking place for the solution.

# Capacitorless Floating Body Cell DRAM Proposal for 2007 ITRS Consideration

- This is a one-transistor (1T) SOI NMOSFET: in contrast to standard approach with one capacitor and one transistor (1T1C)
  - Signal charge is holes injected into floating body of MOSFET, rather than charge on storage capacitance
  - Advantages
    - Potential for reduced cell area (no storage capacitor needed)
    - Potentially scalable like a transistor
    - Fabrication is very consistent with SOI Logic processing technology: advantageous for embedded memory
  - Will be considered for inclusion in 2007 PIDS DRAM

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- **Reliability**

# Logic: Scaling Approach and Categories

- MASTAR (detailed analytic device model from STM and corporate partners) was used
  - MASTAR has been extensively verified against literature and other data
  - Initial choice of scaled MOSFET parameters is made
  - Using MASTAR, MOSFET parameters are iteratively varied to meet ITRS targets→examine tradeoffs
- Types of Logic
  - High Performance (HP) (e.g., MPU): target is historical 17%/year transistor performance increase
  - Low Power (for mobile applications): target is specific, low level of leakage current
    - Low Standby Power (LSTP): very low leakage; for lower performance, consumer applications (e.g., cellphone)
    - Low Operating Power (LOP): low dynamic power, rel. high performance (e.g., notebook computer)

# The “CMOS Change Crunch” Multiple, Big Technology Innovations Over Next 5 Years

*First Year of “Volume Production”*

2000 2005 2010 2015 2020

*Strained Si* — HP, LP

*High k Gate Dielectric* — LP

*Metal Gate Electrode* — LP

*Fully Depleted SOI* — HP, LP

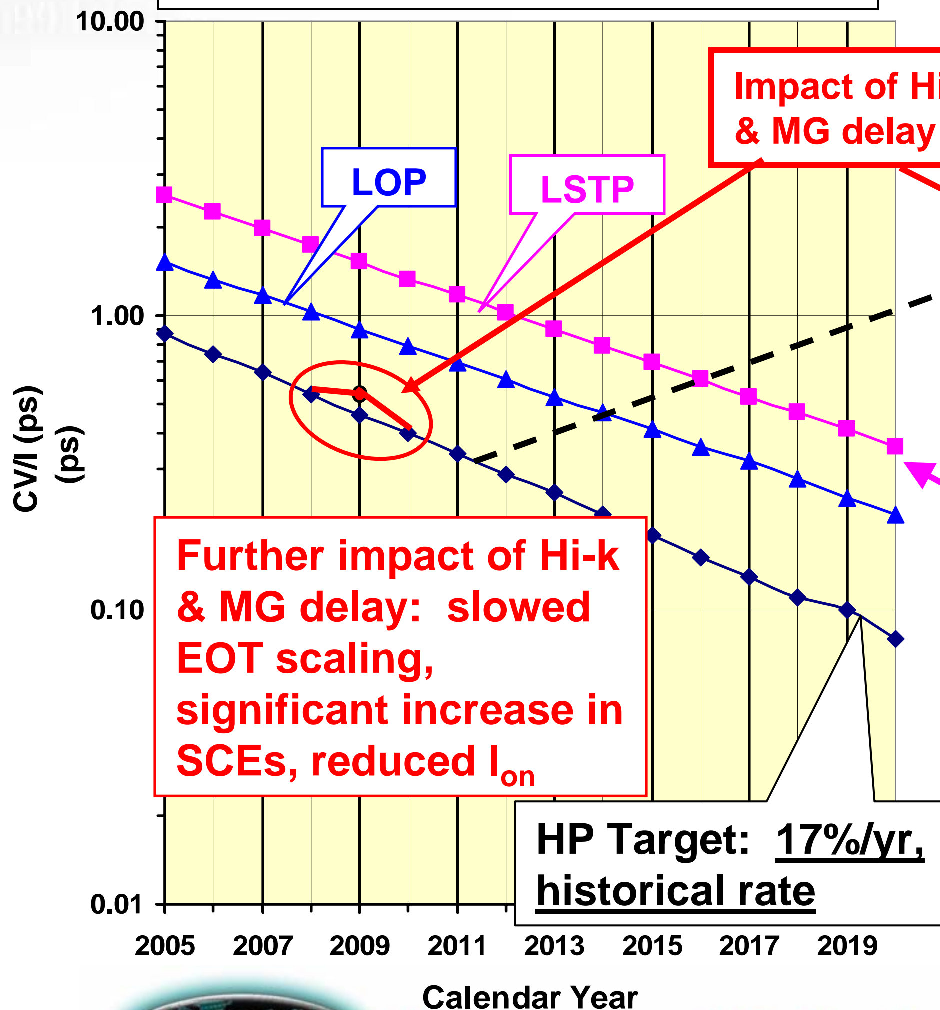
*Multiple Gate MOSFET* — LP

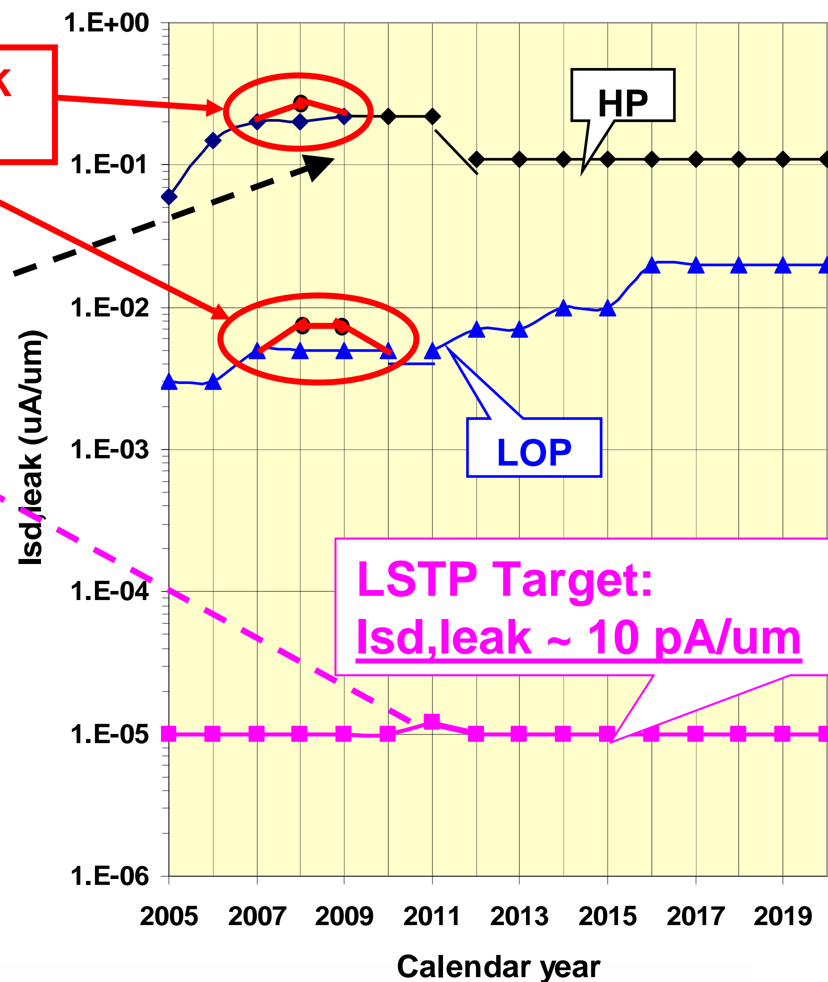
*Others*

2006 PIDS Changes: Delay Projected Date of Deployment of Key Innovations by 2 years for high-performance and LOP Logic (not LSTP). Driven by concerns about feasibility of ’08 deployment

**Driver:** HP = High Performance Applications LP = Low Power Applications

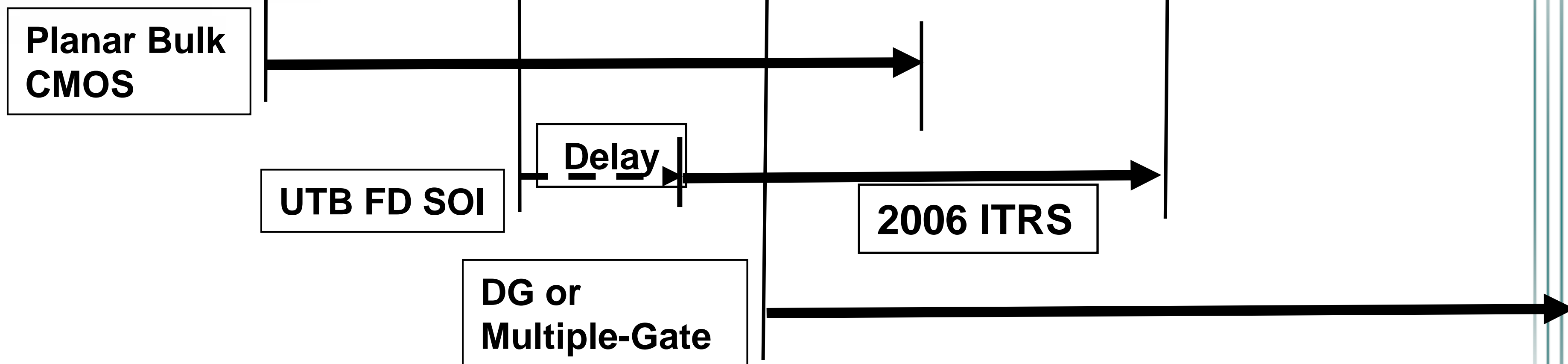
# Low Power & High Performance (HP): Impact of High-k & Metal Gate Deployment Delay



# Multiple Parallel Paths for High-Performance Logic in ITRS

| Year in Production | | 2005 | 2006 | 2007 | 2008 | 2009 | 2010 | 2011 | 2012 | 2013 | 2014 | 2015 | 2016 | 2017 | 2018 | 2019 | 2020 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Physical Lgate (High Performance) | nm | 32 | 28 | 25 | 22 | 20 | 18 | 16 | 14 | 13 | 11 | 10 | 9 | 8 | 7 | 6 | 5 |




**Multiple parallel paths reflects most likely scenario:**

- Some companies will extend planar bulk CMOS as long as possible
- Others will switch to FDSOI and/or multiple gate earlier
  - Initial deployment of FDSOI is delayed in 2006 ITRS
- Ultimate MOSFET is multiple gate
- Similar multiple paths for low-power logic

International Technology Roadmap for Semiconductors



*DRAFT – Work In Progress - NOT FOR PUBLICATION 12 July 2006*

# Outline

- **Scope and Subcategories**
- **Non-Volatile Memory**
- **DRAM**
- **Logic**
- ***Reliability***

# Reliability: Top 5 Near-Term Challenges

- High-k Gate Dielectrics
  - Dielectric breakdown; Transistor instability
- Metal Gate
  - Ion drift, $V_{TH}$ stability, oxidation; thermal-mechanical
- Cu/ Low k
  - Electromigration and voiding; stability of interfaces; TDDB
  - Impact of porous, weaker, less thermally conductive dielectrics
- Packaging
  - Solder bumps; fracture; EM in packaging; CTE mismatch
- Design & Test for Reliability
  - Reliability simulation; Reliability screens

# Reliability: Key Issues

- Reliability risk is growing
  - New materials (e.g., high k/metal gate; low k) and new devices (e.g., FDSOI) and new packaging
    - Introduce new and/or modified failure mechanisms
    - Mechanisms need to be identified, modeled and controlled
    - Have less-than-historic time and resources to ensure reliability
  - Difficult tradeoffs may require reduced reliability margins
  - Need new Design for Reliability tools and reliability screens
- *Need to sustain current high reliability levels in spite of unprecedented changes*

# Summary

- Memory
  - DRAM: Rapid scaling continuing
  - Numerous different types of NVM, with unique attributes and scaling scenarios
- Logic
  - Numerous and rapid technology innovations required
  - 2006 ITRS: delayed projected deployment of high-k and metal gate and FDSOI by 2 years, until 2010
    - Impacts transistor performance, leakage, and short channel effects
- Reliability
  - Ensuring reliability for numerous and rapid technological innovations is a critical challenge
  - Nevertheless, need to sustain current high reliability levels

# BACK UP

# EOT and Gate Leakage Current Density ($J_g$) Scaling with High-k and Metal Gate Deployment Delay

EOT, bulk: from '05 ITRS

Jg,limit: bulk, from '05 ITRS

EOT Scaling: high-k/metal gate delayed until 2010 X

Jg,sim(SiON) scaling: high-k/metal gate delayed until 2010 X

Jg,sim(SiON): bulk, from '05 ITRS

Jg (A/cm^2): 1.E+04, 1.E+03, 1.E+02, 1.E+01

EOT (A): 12, 10, 8, 6, 4, 2, 0

Calendar Year: 2005, 2007, 2009, 2011, 2013, 2015, 2017, 2019

- 2005 ITRS projection: high-k and metal gate available by 2008
- Proposal for 2006 ITRS, delay projected availability of high-k and metal gate until 2010

International Technology Roadmap for Semiconductors



DRAFT – Work In Progress - NOT FOR PUBLICATION 12 July 2006

# Flash Memory

- NOR Flash
  - Technology node (F = minimum poly half pitch) remains unchanged from 2003 ITRS
  - Interpoly EOT scaling in both near term and long term sped up by deployment of high-k
  - In general, advances here result from good engineering, not fundamental breakthroughs
- NAND Flash
  - F moves past DRAM in both near term and long term
  - Cell size area factor, a = cell size/$F^2$ remains the same (but F moves with node)

# Non-Flash Memory

- **FeRAM**
  - Technology node (F) still lags substantially behind DRAM/NAND Flash
  - Ferroelectric capacitor area scaling slows down – 3D is major challenge
  - Main applications smart cards and RFID
- **SONOS/NROM**
  - 2-bits/cell due to localized charge storage
  - Scalability expected similar to floating gate device
  - No floating gate coupling issues
- **MRAM**
  - Both switching field and switching energy are aggressively scaled after 2008. Much of this acceleration is labeled "red" indicating breakthroughs are needed for MRAM to stay competitive.

# Parallel Paths for LSTP in 2005 ITRS

| Year in Production | Units | 2005 | 2006 | 2007 | 2008 | 2009 | 2010 | 2011 | 2012 | 2013 | 2014 | 2015 | 2016 | 2017 | 2017 | 2018 | 2019 | 2020 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Technology Generation | | | | lstp65 | | | lstp45 | | | lstp32 | | | lstp22 | | | | lstp16 | |
| # of years since 2005 | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 12 | 13 | 14 | 15 |
| Physical Lgate (Low-Standby-Power) (Bulk & DG) | nm | 65 | 53 | 45 | 37 | 32 | 28 | 25 | 22 | 20 | 18 | 16 | 14 | 13 | 13 | 12 | 11 | 10 |
| Physical Lgate (Low-Standby-Power) (FD) | nm | | | | | | | | 22 | 20 | 18 | 17 | 16 | 15 | 15 | 14 | 13 | 12 |

Planar Bulk

FDSOI and MG in parallel

[FDSOI = Fully Depleted, Ultra-thin Body SOI]

[MG = Multiple Gate (e.g., FinFET)]

- **Approach**
  - –Extend planar bulk as long as possible
  - –Implement FDSOI and MG in parallel
  - –Slowed Lg scaling for FDSOI in latter years

**Preliminary Results**

# Parallel Paths for LOP in 2005 ITRS

| Year in Production | Units | 2005 | 2006 | 2007 | 2008 | 2009 | 2010 | 2011 | 2012 | 2013 | 2014 | 2015 | 2016 | 2017 | 2017 | 2018 | 2019 | 2020 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Technology Generation | | | | lstp65 | | | lstp45 | | | lstp32 | | | lstp22 | | | | lstp16 | |
| # of years since 2005 | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 12 | 13 | 14 | 15 |
| Physical Lgate (LOP) | nm | 45 | 37 | 32 | 28 | 25 | 22 | 20 | 18 | 16 | 14 | 13 | 11 | 13 | 10 | 9 | 8 | 7 |



[FDSOI = Fully Depleted, Ultra-thin Body SOI]

[MG = Multiple Gate (e.g., FinFET)]

- **Approach**
  - –Extend planar bulk as long as possible
  - –Implement FDSOI and MG in parallel
  - –FDSOI ends in 2016

**Preliminary Results**