

INTERNATIONAL TECHNOLOGY ROADMAP FOR SEMICONDUCTORS

2004 UPDATE

Modeling and Simulation

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MODELING AND SIMULATION

2004 UPDATE HIGHLIGHTS

The most important trend in the 2004 Update of the Modeling and Simulation chapter is the ever increasing need for improved integration between the various areas of simulation, like device and circuit, or interconnect and packaging. Different effects which could in the past be simulated separately will in future need to be treated simultaneously, such as thermal-mechanical, thermodynamic and electronic properties of interconnect materials. Due to the ongoing extension of the PIDS chapter to detail the requirements for high-frequency technologies, the simulation of III/V materials has been added to the short-term challenge on high-frequency device/circuit modeling. Furthermore, various new aspects and additional details were added to the items which explain the challenges and the requirements for Modeling and Simulation.

Concerning the Modeling and Simulation Technology Requirement table, four new features have been added: Full chip lithography simulation, novel memory devices, the impact of processes and materials on electrical performance, and material properties in general. The items which detail the requirements have been considerably extended, and their timing updated.

[Link to the 2003 ITRS Modeling and Simulation chapter](#)

WORKING GROUP TABLES

Table 121 Modeling and Simulation Difficult Challenges [UPDATED](#)

	<i>Difficult Challenges ≥ 45 nm/Through 2010</i>	<i>Summary of Issues</i>
WAS	High-frequency circuit modeling for 5–40 GHz applications	Efficient extraction and simulation of full-chip interconnect delay Accurate and yet efficient 3D interconnect models, especially for transmission lines and S-parameters High-frequency circuit models including non-quasi-static, substrate noise and parasitic coupling Parameter extraction assisted by numerical electrical simulation instead of RF measurements
IS	High-frequency device and circuit modeling for 5– 100 GHz applications	Efficient extraction and simulation of full-chip interconnect delay Accurate and yet efficient 3D interconnect models, especially for transmission lines and S-parameters Extension of physical device models to III/V materials High-frequency circuit models including non-quasi-static, substrate noise, 1/f noise and parasitic coupling Parameter extraction assisted by numerical electrical simulation instead of RF measurement Scalable active and passive component models for compact circuit simulation Co-design between interconnects and packaging
WAS	Front-end process modeling for nanometer Structures	Diffusion/activation/damage models and parameters including low thermal budget processes in Si-based substrate, i.e., Si, SiGe:C (incl. strain), SOI, and ultra-thin body devices Characterization tools/methodologies for these ultra shallow geometries/junctions and low dopant levels Modeling hierarchy from atomistic to continuum for dopants and defects in bulk and at interfaces
IS	Front-end process modeling for nanometer Structures	Diffusion/activation/damage models and parameters including SPE and low thermal budget processes in Si-based substrate, i.e., Si, SiGe:C, Ge (incl. strain), SOI, and ultra-thin body devices Characterization tools/methodologies for these ultra shallow geometries/junctions and low dopant levels Modeling hierarchy from atomistic to continuum for dopants and defects in bulk and at interfaces Front-end processing impact on reliability

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Table 121 Modeling and Simulation Difficult Challenges UPDATED (continued)

	<i>Difficult Challenges ≥ 45 nm/Through 2010</i>	<i>Summary of Issues</i>
WAS	Modeling of equipment Influences on features generated in deposition and etching processes	<p>Fundamental physical data (e.g., rate constants, cross sections, surface chemistry); reaction mechanisms, and reduced models for complex chemistry</p> <p>Linked equipment/feature scale models</p> <p>CMP (full wafer and chip level, pattern dependent effects)</p> <p>MOCVD, PECVD, and ALD modeling</p> <p>Multi-generation equipment/wafer models</p>
IS	<u>Integrated modeling of equipment, materials, feature scale processes and influences on devices</u>	<p>Fundamental physical data (e.g., rate constants, cross sections, surface chemistry <u>for ULK, photoresists and high-k metal gate</u>); reaction mechanisms, and reduced models for complex chemistry</p> <p>Linked equipment/feature scale models <u>(including high-k metal gate integration, damage prediction)</u></p> <p>CMP (full wafer and chip level, pattern dependent effects)</p> <p>MOCVD, PECVD, ALD, <u>electroplating and electroless deposition</u> modeling</p> <p>Multi-generation equipment/wafer models</p>
WAS	Lithography simulation including NGL	<p>Optical simulation of resolution enhancement techniques including mask optimization (OPC, PSM)</p> <p>Predictive resist models including line-edge roughness, etch resistance and mechanical stability</p> <p>Multi-generation lithography system models</p>
IS	Lithography simulation including NGL	<p>Optical simulation of resolution enhancement techniques including mask optimization (OPC, PSM)</p> <p>Predictive resist models <u>(e.g. mesoscale models)</u> including line-edge roughness, etch resistance, <u>adhesion</u>, and mechanical stability</p> <p><u>Methods to easily calibrate resist model kinetic and transport parameters</u></p> <p><u>Models that bridge requirements of OPC (speed) and process development (predictive)</u></p> <p><u>Experimental verification and simulation of ultra-high NA vector models, including polarization</u></p> <p><u>Models and experimental verification of non-optical immersion lithography effects (e.g. topography and change of refractive index distribution)</u></p> <p>Multi-generation lithography system models</p> <p><u>Simulation of defect influences/defect printing</u></p>
WAS	Ultimate nanoscale CMOS simulation capability	<p>Methods and algorithms that contribute to prediction of CMOS limits</p> <p>Quantum based simulators</p> <p>Models and analysis to enable design and evaluation of devices and architectures beyond traditional planar CMOS</p> <p>Phenomenological gate stack models for ultra-thin dielectrics</p> <p>Models for device impact of statistical fluctuations in structures and dopant distributions</p>
IS	Ultimate nanoscale CMOS simulation capability	<p>Methods and algorithms that contribute to prediction of CMOS limits</p> <p>Quantum based simulators</p> <p>Models and analysis to enable design and evaluation of devices and architectures beyond traditional planar CMOS</p> <p>Gate stack models for ultra-thin dielectrics</p> <p>Models for device impact of statistical fluctuations in structures and dopant distributions</p> <p><u>Phenomenological material models for stress engineering</u></p>

Table 121 Modeling and Simulation Difficult Challenges UPDATED (continued)

<i>Difficult Challenges ≥ 45 nm/Through 2010</i>		<i>Summary of Issues</i>
WAS	Thermal-mechanical-electrical modeling for interconnections and packaging	Model thermal-mechanical and electronic properties of low κ , high κ , and conductors and the impact of processing on these properties Model reliability of packages and interconnects, e.g. stress voiding, electromigration, piezoelectric effects; textures, fracture, adhesion
IS	Thermal-mechanical-electrical modeling for interconnections and packaging	Model thermal-mechanical, thermodynamic and electronic properties of low κ , high κ , and conductors and the impact of processing on these properties especially for interfaces and films under 1 micron dimension Model reliability of packages and interconnects, e.g. stress voiding, electromigration, piezoelectric effects; textures, fracture, adhesion. <u>Models for electron transport in ultra fine patterned conductors.</u>
<i>Difficult Challenges < 45 nm/Beyond 2010</i>		<i>Summary of Issues</i>
WAS	Modeling of processing and electrical properties of new materials	Computational materials science tools to understand materials properties, process options, and operating behavior for new materials applied in devices and interconnects, including especially for the following: gate stacks, predictive modeling of dielectric constant, bulk polarization charge, surface states, reliability, breakdown, and leakage currents including band structure, tunneling from process/materials and structure conditions
IS	Modeling of chemical, thermomechanical, and electrical properties of new materials	Computational materials science tools to describe materials properties, process options, and operating behavior for new materials applied in devices and interconnects, including especially for the following: gate stacks, predictive modeling of dielectric constant, bulk polarization charge, surface states, thermomechanical (including stress effects on mobility), optical properties, reliability, breakdown, and leakage currents including band structure, tunneling from process/materials and structure conditions. <u>Models for air gap and novel integrations in 3D interconnects including data for ultrathin material properties.</u>
WAS	Compact modeling including more physical models and statistics	Computer-efficient inclusion of influences of statistics (incl. correlations) before process freeze, quantum/ballistic transport, etc., into compact modeling
	Nano-scale modeling	Process modeling tools for the development of novel nanostructure devices (nanowires, carbon nanotubes, quantum dots, molecular electronics) Device modeling tools for analysis of nanoscale device operation (quantum transport, resonant tunneling, spintronics, contact effects)
IS	Nano-scale modeling	Process modeling tools for the development of novel nanostructure devices (nanowires, carbon nanotubes (incl. doping) , quantum dots, molecular electronics) Device modeling tools for analysis of nanoscale device operation (quantum transport, resonant tunneling, spintronics, contact effects)
	Optoelectronics modeling	Coupling between electrical and optical systems, optical interconnect models, semiconductor laser modeling Physical design tools for integrated electrical/optical systems

4 Modeling and Simulation

Table 122a Modeling and Simulation Technology Requirements: Capabilities—Near-term UPDATED

Year of Production	2003	2004	2005	2006	2007	2008	2009
Technology Node		hp90			hp65		
DRAM ½ Pitch (nm)	100	90	80	70	65	57	50
Lithography							
WAS	Exposure	Include realistic properties of masks, birefringence of lenses; non-planar topographies	Simulation of immersion, EUV, EPL, ML2 lithographic processes including CPU-efficient algorithms				
IS	Exposure	Include realistic properties of masks, birefringence of lenses; non-planar topographies	Simulation of immersion lithography	Simulation of EUV, EPL, ML2, imprint lithography options, models bridging OPC and predictive feature scale simulation			
WAS	Resist models	193 nm/157 nm resist models including ultra-thin resists	Detailed chemically amplified resist model including LER and EUV resists		Finite polymer-size effects		
IS	Resist models	193 nm/157 nm resist models including ultra-thin resists <u>and immersion (liquid-solid interface)</u>	Detailed chemically amplified resist <u>and EUV resist</u> models including LER, <u>and methods to easily calibrate parameters; coupling with etch models</u>		Finite polymer-size effects		
ADD	<u>Full-chip lithography simulation</u>		<u>Simulation of lithography and etching across whole exposure field to detect weak spots</u>				

*For 2003/2004, interim solutions are known but research is still needed towards mature commercial solutions.

Manufacturable solutions exist, and are being optimized
 Manufacturable solutions are known
 Interim solutions are known
 Manufacturable solutions are NOT known

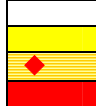
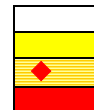


Table 122a Modeling and Simulation Technology Requirements: Capabilities—Near-term UPDATED
(continued)

Year of Production	2003	2004	2005	2006	2007	2008	2009
Technology Node		hp90			hp65		
DRAM ½ Pitch (nm)	100	90	80	70	65	57	50
Front End Process Modeling							
	Gate Stack*	♦ High-κ dielectrics and gate materials (interfaces, impurity diffusion, electrical barrier)		Model materials properties and electrical behavior of prioritized alternative dielectrics and gates (interfaces, defects, impurities, mobility, leakage)		Processing and properties of alternative materials	
WAS	Diffusion and activation models	Interfaces, ultra-shallow junctions and activation	Enhance calibrated phenomenological models by physically based ones for Si based materials, including stress/strain				
IS	Diffusion and activation models	Interfaces, ultra-shallow junctions and activation	<u>Enhancement of models for Si based materials, including stress/strain and including flash/laser anneals and solid phase epitaxy</u>				
Topography Modeling							
WAS	Deposition	Homogeneity, topography dependence	Electrical properties, stress, incl. microstructure		Adhesion and reliability, including microstructure		
IS	<u>Deposition</u>	<u>Uniformity, throughput, topography dependence</u>	<u>Electrical properties, stress, incl. microstructure; layout dependence; prediction of liquid dispense (resist, spin on ULK) on planarity and gate pattern; coupling with etching and lithography models.</u>		<u>Adhesion and reliability, including microstructure; full molecular dynamics (or atomistic) feature scale models, prediction of surface properties</u>		
WAS	Planarization	Cell-level CMP	Chip-level including dummy placement optimization		CMP process models for circuit design		
IS	Planarization	Cell-level CMP	<u>Chip-level including dummy placement optimization, padwear and conditioning disc modeling, physics-based optimizations of rates, uniformity, and defect reduction</u>		CMP process models for circuit design		
WAS	Etching	(Surface) physics based feature scale models	Integration of feature-scale simulation with equipment (plasma) models				
IS	Etching	(Surface) physics based feature scale models	<u>Integration of feature-scale simulation with equipment (plasma) models; process integration (coupling of etch-deposition-plating-CMP-lithography- including data beyond topography), full molecular dynamics (or atomistic) feature scale models</u>				

*For 2003/2004, interim solutions are known but research is still needed towards mature commercial solutions.

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 Manufacturable solutions are known
 Interim solutions are known
 Manufacturable solutions are NOT known



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Table 122a Modeling and Simulation Technology Requirements: Capabilities—Near-term **UPDATED**
(continued)

Year of Production	2003	2004	2005	2006	2007	2008	2009
Technology Node		hp90			hp65		
DRAM ½ Pitch (nm)	100	90	80	70	65	57	50
Numerical Device Modeling [1]							
Classical CMOS*	◆ Mobility models incl. stress, surface roughness and high-κ		Device models with relevant quantum effects included		Models/algorithms to the scaling limit		
Non-classical CMOS including transport-enhanced devices*	◆ Mobility models incl. stress, surface roughness and high-κ		Device models with relevant quantum effects included, especially for ultra-thin films		Ballistic transport		
ADD	Novel memory devices (MRAM, FeRAM, ..)		Processing, material properties and performance modeling of MRAMs, PCMs, FeRAMs and SONOS/NROMs				
WAS	RF Modeling	Parasitic devices	High-frequency noise				
IS	RF Modeling	Parasitic devices	Physical device models for HF noise and mobility in III/Vs				
Circuit Component Modeling [2]							
Active devices*	◆ Non-classical CMOS compact models/ non-quasi-static models and series resistance		Circuit models for non-classical CMOS devices including influences of statistics		Include ballistic effects		
Interconnects and integrated passives	On-chip inductance effects + frequency dependent resistance		Hierarchical full chip RLC		Include reliability		
ADD	Process and Materials Impact on Electrical Performance		Models that relate material properties (process related or fundamental) to electron transport (e.g. in conducting lines). Includes models for electron scattering. Models that predict paths to material property repair (e.g. low-k repair, capacitance repair)				

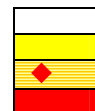
*For 2003/2004, interim solutions are known but research is still needed towards mature commercial solutions.

Manufacturable solutions exist, and are being optimized

Manufacturable solutions are known

Interim solutions are known

Manufacturable solutions are NOT known



Notes for Table 122a **ADDED**





[1] In Numerical Device Modeling equations are solved which are typically based on fundamental physics and describe the electrical behavior on spatially fine resolved quantities. This means usually partial differential equations (with respect spatial coordinates) are employed. The goal is technology optimization and device insight.

[2] In Circuit Element Modeling no spatially resolved models are used. Approximatively analytically solveable, physically based models give a guidance for the used relations between electrical quantities. The goal is a description of device behaviour (currents, charges, noise) in circuit simulators.

Table 122a Modeling and Simulation Technology Requirements: Capabilities—Near-term UPDATED
(continued)

Year of Production	2003	2004	2005	2006	2007	2008	2009
Technology Node		hp90			hp65		
DRAM ½ Pitch (nm)	100	90	80	70	65	57	50
Package Modeling							
WAS	Electrical modeling*	◆ Unified RLC extraction for package/chips		Reduced order models		Full-wave analysis	
	Thermal-mechanical modeling	◆ Thermo-mechanical-integrated models		Include non-bulk materials properties		Include reliability	
IS	Thermal-mechanical modeling	◆ Thermo-mechanical-integrated models		Include non-bulk <u>and porous</u> materials properties		Include reliability (<u>esp. life prediction</u>)	
ADD	<u>Material properties</u>	◆ <u>Improved material models (visco-elasticity, creep, plasticity), interfaces</u>		<u>Full die simulation</u>			
Numerical analysis							
WAS	Algorithms*	◆ Robust, reliable 3D grid generation especially for process simulation		Faster linear solvers		Exploit parallel computation	
IS	Algorithms*	◆ Robust, reliable 3D grid generation especially for process simulation		Faster <u>algorithms including</u> linear solvers		Exploit parallel computation	

*For 2003/2004, interim solutions are known but research is still needed towards mature commercial solutions.

Manufacturable solutions exist, and are being optimized 
 Manufacturable solutions are known 
 Interim solutions are known 
 Manufacturable solutions are NOT known 

Notes for Table 122a ADDED

[1] In Numerical Device Modeling equations are solved which are typically based on fundamental physics and describe the electrical behavior on spatially fine resolved quantities. This means usually partial differential equations (with respect spatial coordinates) are employed. The goal is technology optimization and device insight.

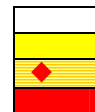
[2] In Circuit Element Modeling no spatially resolved models are used. Approximatively analytically solveable, physically based models give a guidance for the used relations between electrical quantities. The goal is a description of device behaviour (currents, charges, noise) in circuit simulators.

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Table 122b Modeling and Simulation Technology Requirements: Accuracy and Speed—Near-term
UPDATED

	Year of Production	2003	2004	2005	2006	2007	2008	2009
	Technology Node		hp90			hp65		
	DRAM ½ Pitch (nm)	100	90	80	70	65	57	50
WAS	Technology-development cost reduction (due to TCAD)	35%	35%	35%	40%	40%	40%	40%
IS	Technology-development cost reduction (due to TCAD)	35%	<u>35%</u>	35%	40%	40%	40%	40%
Lithography Modeling								
WAS	Resist profile prediction accuracy (5% of printed gate length)	3.3 nm	2.7 nm	2.3 nm	2.0 nm	1.8 nm	1.6 nm	1.4 nm
IS	<u>CD prediction accuracy (incl. OP effects) for dense and isolated lines - 2% of targetted printed gate length</u>	<u>1.3 nm</u>	<u>1.0 nm</u>	<u>0.9 nm</u>	<u>0.8 nm</u>	<u>0.7 nm</u>	<u>0.6 nm</u>	<u>0.6 nm</u>
WAS	OPC model accuracy (about 3% of physical gate length)	1.5 nm	1.5 nm	1 nm	1 nm	1 nm	1 nm	1 nm
DELETE	OPC model accuracy (about 3% of physical gate length) # (1.5 nm	1.5 nm	1 nm	1 nm	1 nm	1 nm	1 nm
Front End Process Modeling								
WAS	Vertical junction depth simulation accuracy (% of physical gate length)	10% (4.5 nm)	10% (3.7 nm)	10% (3.2 nm)	10% (2.8 nm)	10% (2.5 nm)	10% (2.2 nm)	10% (2.0 nm)
IS	Vertical junction depth simulation accuracy (% of physical gate length)	10% (4.5 nm)	10% (3.7 nm)	10% (3.2 nm)	<u>10% (2.8 nm)</u>	<u>10% (2.5 nm)</u>	<u>10% (2.2 nm)</u>	<u>10% (2.0 nm)</u>
WAS	Lateral junction depth (and abruptness) simulation accuracy (% of physical gate length)	5% (2.3 nm)	5% (1.9 nm)	5% (1.6 nm)	5% (1.4 nm)	5% (1.3 nm)	5% (1.1 nm)	5% (1.0 nm)
IS	<u>Lateral junction depth: 50% of FEP Lgate 3 sigma</u>	<u>2.2 nm</u>	<u>1.9 nm</u>	<u>1.6 nm</u>	<u>1.4 nm</u>	<u>1.3 nm</u>	<u>1.1 nm</u>	<u>1.0 nm</u>
WAS	Total source/drain series resistance (accuracy)	10%	10%	10%	10%	10%	10%	10%
IS	Total source/drain series resistance (accuracy)	10%	<u>10%</u>	10%	<u>10%</u>	10%	10%	10%

Manufacturable solutions exist, and are being optimized
 Manufacturable solutions are known
 Interim solutions are known
 Manufacturable solutions are NOT known



Notes for Table 122b ADDED:

[1] In Numerical Device Modeling equations are solved which are typically based on fundamental physics and describe the electrical behavior on spatially fine resolved quantities. This means usually partial differential equations (with respect spatial coordinates) are employed. The goal is technology optimization and device insight.

[2] In Circuit Element Modeling no spatially resolved models are used. Approximately analytically solveable, physically based models give a guidance for the used relations between electrical quantities. The goal is a description of device behaviour (currents, charges, noise) in circuit simulators.

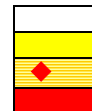
[3] Absolute values strongly differ for HP and LSTP. Important aspects for nominal devices also included in rolloff accuracy

[4] (Positive) difference in Vth of nominal and subnominal device

Table 122b Modeling and Simulation Technology Requirements: Accuracy and Speed—Near-term
 UPDATED (continued)

Year of Production		2003	2004	2005	2006	2007	2008	2009
Technology Node			hp90			hp65		
DRAM ½ Pitch (nm)		100	90	80	70	65	57	50
<i>Back-end process/Equipment/Topography Modeling</i>								
WAS	Etch/deposition cross wafer uniformity (% accuracy of the MPU physical gate length)	2.50%	2.50%	2.50%	2.50%	2.50%	2.50%	2.50%
IS	Etch/deposition cross wafer uniformity (% accuracy of the MPU physical gate length)	◆2.50%	◆2.50%	2.50%	2.50%	2.50%	2.50%	2.50%
WAS	2D/3D topography accuracy (% accuracy of MPU physical gate length)	5% (2.3 nm)	5% (1.9 nm)	5% (1.6 nm)	5% (1.4nm)	5% (1.3 nm)	5% (1.1 nm)	5% (1.0 nm)
IS	2D/3D topography accuracy (% accuracy of MPU physical gate length)	◆5% (1.9 nm)	◆5% (1.9 nm)	5% (1.6 nm)	5% (1.4nm)	5% (1.3 nm)	5% (1.1 nm)	5% (1.0 nm)
<i>Numerical Device Modeling [1]</i>								
Accuracy of ft at given ft (% of maximum chip frequency)		10%	10%	10%	10%	10%	10%	10%
WAS	Gate leakage current accuracy (%) (I_g/I_{off})	25%	25%	25%	25%	25%	25%	25%
IS	Gate leakage accuracy (% of I_g)	25%	25%	25%	25%	25%	25%	25%
WAS	I_{on} accuracy	5%	5%	5%	3%	3%	3%	3%
IS	I_{on} accuracy	5%	5%	5%	3%	3%	3%	3%
WAS	I_{off} accuracy	30%	30%	30%	30%	30%	30%	30%
IS	I_{off} accuracy	30%	30%	30%	30%	30%	30%	30%
WAS	Long-channel V_t (accuracy)	3%	3%	3%	3%	3%	3%	3%
IS	Long-channel V_t accuracy [3]	3%	3%	3%	3%	3%	3%	3%
WAS	V_t rolloff accuracy (mV)	15mV	15mV	15mV	10mV	10mV	7mV	7mV
IS	V_t rolloff accuracy (mV) [4]	15mV	15mV	15mV	10mV	10mV	7mV	7mV
WAS	V_t 3F variation (%)	25%	25%	25%	25%	25%	25%	25%
IS	V_t 3F variation (%)	25%	25%	25%	25%	25%	25%	25%

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 Interim solutions are known
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Notes for Table 122b ADDED:

[1] In Numerical Device Modeling equations are solved which are typically based on fundamental physics and describe the electrical behavior on spatially fine resolved quantities. This means usually partial differential equations (with respect spatial coordinates) are employed. The goal is technology optimization and device insight.

[2] In Circuit Element Modeling no spatially resolved models are used. Approximately analytically solveable, physically based models give a guidance for the used relations between electrical quantities. The goal is a description of device behaviour (currents, charges, noise) in circuit simulators.

[3] Absolute values strongly differ for HP and LSTP. Important aspects for nominal devices also included in rolloff accuracy

[4] (Positive) difference in V_{th} of nominal and subnominal device

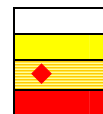
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Table 122b Modeling and Simulation Technology Requirements: Accuracy and Speed—Near-term
 UPDATED (continued)

Year of Production		2003	2004	2005	2006	2007	2008	2009
Technology Node			hp90			hp65		
DRAM 1/2 Pitch (nm)		100	90	80	70	65	57	50
<i>Circuit Element Modeling/ECAD [2]</i>								
WAS	I-V error—compact model accuracy	5%	5%	5%	3%	3%	3%	3%
IS	I-V error <u>in saturation region</u>	8%	8%	8%	6%	6%	5%	5%
ADDED	I-V error <u>in linear region</u>	4%	4%	3%	3%	3%	3%	3%
WAS	Sub-threshold current accuracy model accuracy	10%	10%	10%	10%	10%	10%	10%
IS	<u>I-V error in subthreshold and off-current</u>	20%	20%	15%	15%	10%	10%	10%
WAS	Intrinsic MOS C-V accuracy	5%	5%	5%	5%	5%	5%	5%
IS	Intrinsic MOS C-V accuracy	5%	5%	5%	5%	5%	5%	5%
WAS	Parasitic C-V accuracy	5%	5%	5%	5%	5%	5%	5%
IS	Parasitic C-V accuracy	5%	5%	5%	5%	5%	5%	5%
WAS	Accuracy of G_m and r_0 at $V_t + 150\text{mV}$ versus L , V_{bs} , V_{ds} and T	10%	10%	10%	10%	10%	10%	10%
IS	Accuracy of G_m and G_d at $V_t + 150\text{mV}$ versus L , V_{bs} , V_{ds} and T	10%	10%	10%	10%	10%	10%	10%
WAS	Circuit delay accuracy (% of maximum chip frequency)	5%	5%	5%	5%	5%	5%	5%
IS	Circuit delay accuracy (% of <u>1/maximum</u> chip frequency)	5%	5%	5%	5%	5%	5%	5%
WAS	RLC delay accuracy (% of maximum chip frequency)	5%	5%	5%	5%	5%	5%	5%
IS	RLC delay accuracy (% of <u>1/maximum</u> chip frequency)	5%	5%	5%	5%	5%	5%	5%
<i>Package Modeling</i>								
WAS	Package delay accuracy (% of off-chip clock frequency)	1%	1%	1%	1%	1%	1%	1%
IS	<u>Package delay accuracy (% of 1/off-chip clock frequency)</u>	1%	1%	1%	1%	1%	1%	1%
WAS	Temperature distribution for chip and package (accuracy)	1C	1C	1C	1C	1C	1C	1C
IS	<u>Temperature distribution for package (accuracy)</u>	1C	1C	1C	1C	1C	1C	1C
<i>Numerical Method</i>								
WAS	Speed-up of algorithms for 3D process/device (compared with year 2000)	4x	5.6x	8x	11.2x	16x	22.4x	32x
IS	Speed-up of algorithms for 3D process/device/ <u>interconnect simulation</u> (compared with year 2000)*	4x	5.6x	8x	11.2x	16x	22.4x	32x

ADDED *Numbers referring to continuum models. Estimated scaling similar to the ITRS. Different figures expected for other models.

Manufacturable solutions exist, and are being optimized
 Manufacturable solutions are known
 Interim solutions are known
 Manufacturable solutions are NOT known







Notes for Table 122b ADDED:

[1] In Numerical Device Modeling equations are solved which are typically based on fundamental physics and describe the electrical behavior on spatially fine resolved quantities. This means usually partial differential equations (with respect spatial coordinates) are employed. The goal is technology optimization and device insight.
 [2] In Circuit Element Modeling no spatially resolved models are used. Approximatively analytically solvable, physically based models give a guidance for the used relations between electrical quantities. The goal is a description of device behaviour (currents, charges, noise) in circuit simulators.
 [3] Absolute values strongly differ for HP and LSTP. Important aspects for nominal devices also included in rolloff accuracy
 [4] (Positive) difference in V_{th} of nominal and subnominal device

Table 122c Modeling and Simulation Technology Requirements: Capabilities—Long-term **UPDATED**

Year of Production	2010	2011	2012	2013	2014	2015	2016	2017	2018
Technology Node	hp45			hp32			hp22		
DRAM ½ Pitch (nm)	45	40	35	32	28	25	22	20	18
Lithography Modeling									
WAS	Next generation lithography	NGL models and modeling of materials and components (immersion, EUV, EPL, ML2 lithographic processes, imprint)							
WAS	Resist technology	Finite polymer-size effects	Non-conventional photo-resist models						
IS	Resist technology	Meso-scale resist models with finite molecule effects	Non-conventional photo-resist models and coupling with etch models						
Front End process Modeling									
	Advanced process models	Atomistic process modeling							
	Models for advanced doping techniques	New technology needed							
Topography Modeling									
WAS	Alternative material models	Calculation of thermal, mechanical and electronic properties	Atomistic material model						
IS	Alternative material models	Calculation of thermal (thermodynamic), mechanical and electronic properties; process impact on intrinsic material behavior integrity and electrical performance under strain.	Atomistic material model						
WAS	Equipment impact on process results including material properties	Computer engineered materials and process recipes							
IS	Equipment impact on process results including material properties	Computer engineered materials and process recipes; predictive manufacturability and yield; full process integration models.							

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12 Modeling and Simulation

Table 122c Modeling and Simulation Technology Requirements: Capabilities—Long-term **UPDATED**

Year of Production	2010	2011	2012	2013	2014	2015	2016	2017	2018
Technology Node	hp45			hp32			hp22		
DRAM ½ Pitch (nm)	45	40	35	32	28	25	22	20	18
<i>Numerical Device Modeling</i>									
Emerging devices	Nanoscale simulation capability including accurate quantum effects								
<i>Circuit Element Modeling/ECAD</i>									
Advanced circuit models	Circuit models for nanoscale devices and interconnects								
<i>Package Modeling</i>									
Electrical/optical models	Mixed electrical-optical analysis			Reliability prediction in coupled modeling					
<i>Numerics</i>									
WAS	Numerical algorithms	Efficient atomistic/ quantum methods			Multi-scale simulation (atomistic-continuum)				
IS	Numerical algorithms	Efficient atomistic/ quantum methods; <u>ab-initio or molecular dynamics based topography simulations.</u>			Multi-scale simulation (atomistic-continuum); <u>fast coupling of equipment-topography-electrical-reliability models; hierarchical full-chip simulation</u>				

Manufacturable solutions exist, and are being optimized

Manufacturable solutions are known

Interim solutions are known

Manufacturable solutions are NOT known

