INTERNATIONAL TECHNOLOGY ROADMAP FOR SEMICONDUCTORS

2004 UPDATE

Interconnect

Jointly Sponsored
by

European Semiconductor Industry Association

Japan Electronics and Information Technology Industries Association

Korea Semiconductor Industry Association

Taiwan Semiconductor Industry Association

Semiconductor Industry Association

TABLE OF CONTENTS

LIST OF TABLES

INTERCONNECT

2004 UPDATE HIGHLIGHTS

In general the 2004 ITRS Interconnect requirements tables will change very little from the numbers published in 2003. However, there are additions and expansions of some metrics that are intended to clarify specific interconnect issues.

- There has been further clarification of what is meant by “Metal 1” as opposed to “local wiring.” In the latest chapter, the deteriorating resistivity of copper wires, as linewidth decreases, is highlighted.
- For Logic, additional Cu resistivity numbers are being added to reflect the effect of surface or sidewall scattering. A model, which incorporates resistivity of copper ρ_o = constant 1.9 μΩ-cm at 300 K, a mean free path of charge carriers $\lambda = 3.4 \times 10^{-6}$cm (34nm), a wire width W (cm), a probability for reflection of electrons at the grain boundaries of 0.2, and the portion, p, of electrons specularly reflected from the walls (surface or interface), has been used to generate a series of new metrics in the Technology requirements tables (81a and 81b. The new metrics tabulate the impact to line resistivity at; Metal 1, intermediate, and global wiring. In these tables, interconnect delay (ps) is calculated for a one mm copper wire, assuming width dependent scattering (as described above) and a conformal barrier of thickness specified in the table. For the first time in the past 10 years, the low κ portion of the roadmap was unaltered (κ value targets not delayed) with respect to the prior edition. Small changes were made to the shading of the boxes for bulk and effective dielectric constant over the nest 5 years, recognizing that materials that deliver an effective κ =2.7 are in production today, and those material systems that will deliver an effective κ = 2.4 are expected to be available with manufacturable solutions in the next three years.
- The proposed changes for DRAM are relatively minor and center on the contacts. There are some changes in specific via and contact resistivity, with the contact A/R rising to >20 in 2018. This is now a “red” challenge associated with 16 nm DRAM half pitch. Cu has been delayed to 2007. The need to distinguish the requirements for embedded, Flash, and traditional DRAM was identified by the committee, but will not be addressed until the next major revision in 2005.
- In the Interconnect surface cleans tables, the notes clarifying the contributors to damage due to rework, strip, and clean, have been updated.

In assessing the Interconnect roadmap as a whole, however, it still becomes almost entirely “red bricks” (red = “no known solution”) by the end of this decade. No new discoveries or major breakthroughs have occurred in the year since closing the 2003 roadmap to change the outlook.

Link to the 2003 ITRS Interconnect chapter

WORKING GROUP TABLES

Table 80 Interconnect Difficult Challenges

Five Difficult Challenges *≥45 nm/Through 2009*	*Summary of Issues*
Introduction of new materials to meet conductivity requirements and reduce the dielectric permittivity*	The rapid introductions of new materials/processes that are necessary to meet conductivity requirements and reduce the dielectric permittivity create integration and material characterization challenges.
Engineering manufacturable interconnect structures compatible with new materials and processes*	Integration complexity, CMP damage, resist poisoning, dielectric constant degradation. Lack of interconnect/packaging architecture design optimization tool.
Achieving necessary reliability	New materials, structures, and processes create new chip reliability (electrical, thermal, and mechanical) exposure. Detecting, testing, modeling and control of failure mechanisms will be key.
Three-dimensional control (3D CD) of interconnect features (with its' associated metrology) is required to achieve necessary circuit performance and reliability.	Line edge roughness, trench depth and profile, via shape, etch bias, thinning due to cleaning, CMP effects. The multiplicity of levels combined with new materials, reduced feature size, and pattern dependent processes create this challenge.
Manufacturability and defect management that meet overall cost/performance requirements	As feature sizes shrink, interconnect processes must be compatible with device roadmaps and meet manufacturing targets at the specified wafer size. Plasma damage, contamination, thermal budgets, cleaning of high A/R features, defect tolerant processes, elimination/reduction of control wafers are key concerns. Where appropriate, global wiring and packaging concerns will be addressed in an integrated fashion.
Five Difficult Challenges *<45 nm/Beyond 2009*	*Summary of Issues*
Mitigate impact of size effects in interconnect structures	Line and via sidewall roughness, intersection of porous low-κ voids with sidewall, barrier roughness, and copper surface roughness will all adversely affect electron scattering in copper lines and cause increases in resistivity.
Three-dimensional control (3D CD) of interconnect features (with its' associated metrology) is required	Line edge roughness, trench depth and profile, via shape, etch bias, thinning due to cleaning, CMP effects. The multiplicity of levels, combined with new materials, reduced feature size and pattern dependent processes, use of alternative memories, optical and RF interconnect, continues to challenge.
Patterning, cleaning, and filling at nano dimensions	As features shrink, etching, cleaning, and filling high aspect ratio structures will be challenging, especially for low-κ dual-Damascene metal structures and DRAM at nano dimensions.
Integration of new processes and structures, including interconnects for emerging devices	Combinations of materials and processes used to fabricate new structures create integration complexity. The increased number of levels exacerbate thermomechanical effects. Novel/active devices may be incorporated into the interconnect.
Identify solutions which address global wiring scaling issues*	Traditional interconnect scaling will no longer satisfy performance requirements. Defining and finding solutions beyond copper and low κ will require material innovation, combined with accelerated design, packaging and unconventional interconnect.

** Top three challenges*

Table 81a MPU Interconnect Technology Requirements—Near-term UPDATED

	Year of Production	*2003*	*2004*	*2005*	*2006*	*2007*	*2008*	*2009*
	Technology Node		*hp90*			*hp65*		
	DRAM ½ Pitch (nm)	*100*	*90*	*80*	*70*	*65*	*57*	*50*
	MPU/ASIC ½ Pitch (nm)	*120*	*107*	*95*	*85*	*76*	*67*	*60*
	MPU Printed Gate Length (nm)	*65*	*53*	*45*	*40*	*35*	*32*	*28*
	MPU Physical Gate Length (nm)	*45*	*37*	*32*	*28*	*25*	*22*	*20*
	Number of metal levels	9	10	11	11	11	12	12
	Number of optional levels – ground planes/capacitors	4	4	4	4	4	4	4
	Total interconnect length (m/cm^2) – active wiring only, excluding global levels [1]	579	688	907	1002	1117	1401	1559
	FITs/m length/cm^2 × 10^{-3} excluding global levels [2]	8.6	7.3	5.5	5	4.5	3.6	3.3
WAS	Jmax (A/cm^2) – intermediate wire (at 105°C)	3.70E+05	5.00E+05	6.80E+05	7.80E+05	1.00E+06	1.40E+06	2.50E+06
IS	Jmax (A/cm^2) – intermediate wire (at 105°C)	**3.40E+05**	**5.30E+05**	**6.80E+05**	**9.30E+05**	**1.40E+06**	**1.60E+06**	**1.90E+06**
	Metal 1 wiring pitch (nm) *	240	214	190	170	152	134	120
	Metal 1 A/R (for Cu)	1.6	1.7	1.7	1.7	1.7	1.8	1.8
WAS	Interconnect RC delay (ps) for 1 mm Metal 1 line	191	224	284	355	384	477	595
IS	Interconnect RC delay (ps) for a 1 mm Cu Metal 1 wire, **assumes no scattering and an effective ρ of 2.2 µΩ-cm**	191	224	284	355	384	477	595
ADD	**Interconnect RC delay (ps) for 1 mm Cu Metal 1 wire, assumes width-dependent scattering and a conformal barrier of thickness specified below**	**254**	**304**	**3.95**	**502**	**553**	**714**	**930**
ADD	**Conductor effective resistivity (µΩ-cm) Cu Metal 1 wiring including effect of width-dependent scattering and a conformal barrier of thickness specified below**	**2.93**	**2.99**	**3.06**	**3.11**	**3.22**	**3.35**	**3.5**
ADD	**Barrier/cladding thickness (for Cu Metal 1 wiring) (nm) [3]**	**9**	**8**	**7**	**6**	**5.4**	**4.9**	**4.5**
WAS	Line length (mm) where τ = RC delay (Metal 1 wire)	79	65	55	46	41	34	28
IS	Line length (µm) where τ = RC delay (Metal 1 wire) **no scattering**	79	65	55	46	41	34	28
	Cu thinning at minimum pitch due to erosion (nm), 10% × height, 50% areal density, 500 µm square array	19	18	16	14	13	12	11
	Intermediate wiring pitch (nm)	320	275	240	215	195	174	156
	Intermediate wiring dual Damascene A/R (Cu wire/via)	1.7/1.5	1.7/1.5	1.7/1.5	1.7/1.6	1.8/1.6	1.8/1.6	1.8/1.6

**Refer to Executive Summary Figure 4 for definition of Metal 1 pitch*

Manufacturable solutions exist, and are being optimized	⬜
Manufacturable solutions are known	🟨
Interim solutions are known	◆
Manufacturable solutions are NOT known	🟥

Table 81a MPU Interconnect Technology Requirements—Near-term UPDATED

	Year of Production	*2003*	*2004*	*2005*	*2006*	*2007*	*2008*	*2009*
	Technology Node		*hp90*			*hp65*		
	DRAM ½ Pitch (nm)	*100*	*90*	*80*	*70*	*65*	*57*	*50*
	MPU/ASIC ½ Pitch (nm)	*120*	*107*	*95*	*85*	*76*	*67*	*60*
	MPU Printed Gate Length (nm)	*65*	*53*	*45*	*40*	*35*	*32*	*28*
	MPU Physical Gate Length (nm)	*45*	*37*	*32*	*28*	*25*	*22*	*20*
WAS	Interconnect RC delay (ps) for 1 mm intermediate line	**105**	**139**	**182**	**224**	**229**	**288**	**358**
IS	Interconnect RC delay (ps) for a 1 mm **Cu intermediate wire, assumes no scattering and an effective ρ of 2.2 μΩ-cm**	**105**	**139**	**182**	**224**	**229**	**288**	**358**
ADD	**Interconnect RC delay (ps) for 1 mm Cu intermediate wire, assumes width-dependent scattering and a conformal barrier of thickness specified below**	**130**	**173**	**235**	**294**	**299**	**381**	**498**
ADD	**Conductor effective resistivity (μΩ-cm) Cu intermediate wiring including effect of width-dependent scattering and a conformal barrier of thickness specified below**	**2.71**	**2.75**	**2.84**	**2.89**	**2.92**	**2.96**	**3.11**
	Barrier/cladding thickness (for Cu intermediate wiring) (nm) [3]	**12**	**10**	**9**	**8**	**7**	**6**	**6**
WAS	Line length (mm) where τ = RC delay (intermediate wire)	**107**	**83**	**69**	**58**	**53**	**43**	**37**
IS	Line length (μm) where τ = RC delay (intermediate wire) **no scattering**	**107**	**83**	**69**	**58**	**53**	**43**	**37**
	Cu thinning at minimum intermediate pitch due to erosion (nm), 10% × height, 50% areal density, 500 μm square array	**27**	**23**	**20**	**18**	**18**	**15**	**10**
	Minimum global wiring pitch (nm)	**475**	**410**	**360**	**320**	**290**	**260**	**234**
	Ratio range (global wiring pitches/intermediate wiring pitch)	**1.5–5.0**	**1.5–6.7**	**1.5–6.7**	**1.5–6.7**	**1.5–8.0**	**1.5–8.0**	**1.5–8.0**
	Global wiring dual Damascene A/R (Cu wire/via)	**2.1/1.9**	**2.1/1.9**	**2.2/2.0**	**2.2/2.0**	**2.2/2.0**	**2.3/2.0**	**2.3/2.0**

**Refer to Executive Summary Figure 4 for definition of Metal 1 pitch*

Manufacturable solutions exist, and are being optimized	⬜
Manufacturable solutions are known	🟨
Interim solutions are known	◆
Manufacturable solutions are NOT known	🟥

Table 81a MPU Interconnect Technology Requirements—Near-term UPDATED

	Year of Production	*2003*	*2004*	*2005*	*2006*	*2007*	*2008*	*2009*
	Technology Node		*hp90*			*hp65*		
	DRAM ½ Pitch (nm)	*100*	*90*	*80*	*70*	*65*	*57*	*50*
	MPU/ASIC ½ Pitch (nm)	*120*	*107*	*95*	*85*	*76*	*67*	*60*
	MPU Printed Gate Length (nm)	*65*	*53*	*45*	*40*	*35*	*32*	*28*
	MPU Physical Gate Length (nm)	*45*	*37*	*32*	*28*	*25*	*22*	*20*
WAS	Interconnect RC delay (ps) for 1 mm global line at minimum pitch	42	55	69	87	92	112	139
IS	Interconnect RC delay (ps) for a 1 mm Cu min. pitch global wire, **assumes no scattering and an effective ρ of 2.2 μΩ-cm**	42	55	69	87	92	112	139
ADD	**Interconnect RC delay (ps) for 1 mm Cu min. pitch global wire, assumes width-dependent scattering and a conformal barrier of thickness specified below**	**46**	**61**	**78**	**101**	**106**	**130**	**167**
ADD	**Conductor effective resistivity (μΩ-cm) Cu global wiring including effect of width-dependent scattering and a conformal barrier of thickness specified below**	**2.42**	**2.45**	**2.5**	**2.54**	**2.57**	**2.6**	**2.69**
ADD	**Barrier/cladding thickness (for min. pitch Cu global wiring) (nm) [3]**	**12**	**10**	**9**	**8**	**7**	**6**	**6**
WAS	Line length (mm) where τ = RC delay (global wire at minimum pitch)	169	132	112	93	83	69	59
IS	Line length (μm) where τ = RC delay **(**global wire at minimum pitch **- no scattering)**	169	132	112	93	83	69	59
	Cu thinning of maximum width global wiring due to dishing and erosion (nm), 10% × height, 80% areal density	168	193	176	158	172	160	144
	Cu thinning global wiring due to dishing (nm), 100 μm wide feature	30	29	24	21	19	17	15
WAS	Conductor effective resistivity (μΩ-cm) Cu intermediate wiring	2.2	2.2	2.2	2.2	2.2	2.2	2.2
IS	Conductor effective resistivity (μΩ-cm) **Cu wiring, assumes no scattering**	2.2	2.2	2.2	2.2	2.2	2.2	2.2
WAS	Interlevel metal insulator (minimum expected) – effective dielectric constant (κ)	3.3–3.6	3.1–3.6	3.1–3.6	3.1–3.6	2.7–3.0	2.7–3.0	2.7–3.0
IS	Interlevel metal insulator (minimum expected) – effective dielectric constant (κ)**[4]**	3.3–3.6	3.1–3.6	3.1–3.6	3.1–3.6	2.7–3.0	2.7–3.0	2.7–3.0
WAS	Interlevel metal insulator (minimum expected) – bulk dielectric constant (κ)	<3.0	<2.7	<2.7	<2.7	<2.4	<2.4	<2.4
IS	Interlevel metal insulator (minimum expected) – bulk dielectric constant (κ)	<3.0	≤2.7	≤2.7	≤2.7	<2.4	<2.4	<2.4

**Refer to Executive Summary Figure 4 for definition of Metal 1 pitch*

Manufacturable solutions exist, and are being optimized	⬜
Manufacturable solutions are known	🟨
Interim solutions are known	◆
Manufacturable solutions are NOT known	🟥

Table 81b MPU Interconnect Technology Requirements—Long-term UPDATED

	Year of Production	*2010*	*2011*	*2012*	*2013*	*2014*	*2015*	*2016*	*2017*	*2018*
	Technology Node	*hp45*			*hp32*			*hp22*		
	DRAM ½ Pitch (nm)	*45*	*40*	*35*	*32*	*28*	*25*	*22*	*20*	*18*
	MPU/ASIC ½ Pitch (nm)	*54*	*48*	*42*	*38*	*34*	*30*	*27*	*24*	*21*
	MPU Printed Gate Length (nm)	*25*	*22*	*20*	*18*	*16*	*14*	*13*	*11*	*10*
	MPU Physical Gate Length (nm)	*18*	*16*	*14*	*13*	*11*	*10*	*9*	*8*	*7*
WAS	Number of metal levels	**12**		**12**	**12**		**13**	**14**		**14**
IS	Number of metal levels	**12**	**12**	**12**	**12**	**13**	**13**	**14**	**14**	**14**
WAS	Number of optional levels – ground planes/capacitors	**4**		**4**	**4**		**4**	**4**		**4**
IS	Number of optional levels – ground planes/capacitors	**4**	**4**	**4**	**4**	**4**	**4**	**4**	**4**	**4**
WAS	Total interconnect length (m/cm^2) – active wiring only, excluding global levels [1]	**1784**		**2214**	**2544**		**3544**	**4208**		**5035**
IS	Total interconnect length (m/cm^2) – active wiring only, excluding global levels [1]	**1784**	**1994**	**2214**	**2544**	**3203**	**3544**	**4208**	**4583**	**5035**
WAS	FITs/m length/cm^2 × 10^{-3} excluding global levels [2]	**2.8**		**2.3**	**2**		**1.4**	**1.2**		**1**
IS	FITs/m length/cm^2 × 10^{-3} excluding global levels [2]	**2.8**	**2.5**	**2.3**	**2**	**1.6**	**1.4**	**1.2**	**1.1**	**1**
WAS	Jmax (A/cm^2) – intermediate wire (at 105°C)	**3.00E+06**		**3.70E+06**	**4.30E+06**		**5.10E+06**	**5.80E+06**		**6.90E+06**
IS	Jmax (A/cm^2) – intermediate wire (at 105°C)	**2.50E+06**	**2.60E+06**	**2.90E+06**	**3.90E+06**	**4.30E+06**	**5.10E+06**	**7.10E+06**	**7.10E+06**	**8.00E+06**
WAS	Metal 1 wiring pitch (nm) *	**108**		**84**	**76**		**60**	**54**		**42**
IS	Metal 1 wiring pitch (nm) *	**108**	**94**	**84**	**76**	**68**	**60**	**54**	**48**	**42**
WAS	Metal 1 A/R (for Cu)	**1.8**		**1.8**	**1.9**		**1.9**	**2**		**2**
IS	Metal 1 A/R (for Cu)	**1.8**	**1.8**	**1.8**	**1.9**	**1.9**	**1.9**	**2**	**2**	**2**
WAS	Interconnect RC delay (ps) for 1 mm Metal 1 line	**616**		**963**	**970**		**1510**	**2008**		**2679**
IS	Interconnect RC delay (ps) for a 1 mm **Cu Metal 1 wire, assumes no scattering and an effective ρ of 2.2 µΩ-cm**	**616**	**819**	**963**	**970**	**1237**	**1510**	**2008**	**2413**	**2679**

**Refer to Executive Summary Figure 4 for definition of Metal 1 pitch*

Manufacturable solutions exist, and are being optimized	⬜
Manufacturable solutions are known	🟨
Interim solutions are known	◆
Manufacturable solutions are NOT known	🟥

Table 81b MPU Interconnect Technology Requirements—Long-term UPDATED (continued)

	Year of Production	*2010*	*2011*	*2012*	*2013*	*2014*	*2015*	*2016*	*2017*	*2018*
	Technology Node	*hp45*			*hp32*			*hp22*		
	DRAM ½ Pitch (nm)	*45*	*40*	*35*	*32*	*28*	*25*	*22*	*20*	*18*
	MPU/ASIC ½ Pitch (nm)	*54*	*48*	*42*	*38*	*34*	*30*	*27*	*24*	*21*
	MPU Printed Gate Length (nm)	*25*	*22*	*20*	*18*	*16*	*14*	*13*	*11*	*10*
	MPU Physical Gate Length (nm)	*18*	*16*	*14*	*13*	*11*	*10*	*9*	*8*	*7*
ADD	**Interconnect RC delay (ps) for 1 mm Cu Metal 1 wire, assumes width-dependent scattering and a conformal barrier of thickness specified below**	**1021**	**1418**	**1875**	**2051**	**2692**	**3672**	**4229**	**5736**	**8122**
ADD	**Conductor effective resistivity (μΩ-cm) Cu Metal 1 wiring including effect of width dependent scattering and a conformal barrier of thickness specified below**	**3.62**	**3.81**	**4.02**	**4.14**	**4.35**	**4.62**	**4.88**	**5.23**	**5.67**
ADD	**Barrier/cladding thickness (for Cu M1 wiring) (nm) [3]**	**4**	**3.5**	**3.2**	**2.8**	**2.5**	**2.2**	**2**	**1.8**	**1.6**
WAS	Line length (mm) where τ = RC delay (Metal 1 wire)	**25**		**18**	**15**		**11**	**9**		**6**
IS	Line length (μm) where τ = RC delay (Metal 1 wire) **no scattering**	**25**	**21**	**18**	**15**	**13**	**11**	**9**	**7**	**6**
WAS	Cu thinning at minimum pitch due to erosion (nm), 10% × height, 50% areal density, 500 μm square array	**10**		**8**	**7**		**6**	**5**		**4**
IS	Cu thinning at minimum pitch due to erosion (nm), 10% × height, 50% areal density, 500 μm square array	**10**	**8**	**8**	**7**	**7**	**6**	**5**	**5**	**4**
WAS	Intermediate wiring pitch (nm)	**135**		**110**	**95**		**78**	**65**		**55**
IS	Intermediate wiring pitch (nm)	**135**	**122**	**110**	**95**	**86**	**78**	**65**	**60**	**55**
WAS	Intermediate wiring dual Damascene A/R (Cu wire/via)	**1.8/1.6**		**1.9/1.7**	**1.9/1.7**		**1.9/1.7**	**2.0/1.8**		**2.0/1.8**
IS	Intermediate wiring dual Damascene A/R (Cu wire/via)	**1.8/1.6**	**1.8/1.6**	**1.9/1.7**	**1.9/1.7**	**1.9/1.7**	**1.9/1.7**	**2.0/1.8**	**2.0/1.8**	**2.0/1.8**
WAS	Interconnect RC delay (ps) for 1 mm intermediate line	**380**		**552**	**614**		**908**	**1203**		**1582**
IS	Interconnect RC delay (ps) for a 1 mm **Cu intermediate wire, assumes no scattering and an effective ρ of 2.2 μΩ-cm**	**380**	**468**	**552**	**614**	**746**	**908**	**1203**	**1421**	**1582**

**Refer to Executive Summary Figure 4 for definition of Metal 1 pitch*

Manufacturable solutions exist, and are being optimized	⬜
Manufacturable solutions are known	🟨
Interim solutions are known	🟨◆
Manufacturable solutions are NOT known	🟥

Table 81b MPU Interconnect Technology Requirements—Long-term UPDATED (continued)

	Year of Production	2010	2011	2012	2013	2014	2015	2016	2017	2018
	Technology Node	hp45			hp32			hp22		
	DRAM ½ Pitch (nm)	45	40	35	32	28	25	22	20	18
	MPU/ASIC ½ Pitch (nm)	54	48	42	38	34	30	27	24	21
	MPU Printed Gate Length (nm)	25	22	20	18	16	14	13	11	10
	MPU Physical Gate Length (nm)	18	16	14	13	11	10	9	8	7
ADD	Interconnect RC delay (ps) for 1 mm Cu intermediate wire, assumes width-dependent scattering and a conformal barrier of thickness specified below	586	743	903	1152	1465	1834	2527	3043	3774
ADD	Conductor effective resistivity (µΩ-cm) Cu intermediate wiring including effect of width-dependent scattering and a conformal barrier of thickness specified below	3.19	3.3	3.38	3.58	3.73	3.84	4.17	4.28	4.46
WAS	Barrier/cladding thickness (for Cu intermediate wiring) (nm) [3]	5		4	3.5		3	2.5		2
IS	Barrier/cladding thickness (for Cu intermediate wiring) (nm) [3]	4.9	4.5	4	3.6	3.3	2.9	2.5	2.2	2
WAS	Line length (mm) where τ = RC delay (intermediate wire)	32		23	19		14	11		8
IS	Line length (µm) where τ = RC delay (intermediate wire) no scattering	32	27	23	19	16	14	11	9	8
WAS	Cu thinning at minimum intermediate pitch due to erosion (nm), 10% ' height, 50% areal density, 500 µm square array	12		10	9		7	7		6
IS	Cu thinning at minimum intermediate pitch due to erosion (nm), 10% x height, 50% areal density, 500 µm square array	12	11	10	9	8	7	7	6	6
WAS	Minimum global wiring pitch (nm)	205		165	140		117	100		83
IS	Minimum global wiring pitch (nm)	205	185	165	140	130	117	100	90	83
WAS	Ratio range (global wiring pitches/intermediate wiring pitch)	1.5–10		1.5–10	1.5–13		1.5–13	1.5–16		1.5–16
IS	Ratio range (global wiring pitches/intermediate wiring pitch)	1.5–10	1.5-10	1.5–10	1.5–13	1.5-13	1.5–13	1.5–16	1.5-16	1.5–16
WAS	Global wiring dual-Damascene A/R (Cu wire/via)	2.3/2.1		2.3/2.1	2.4/2.2		2.4/2.2	2.5/2.3		2.5/2.3
IS	Global wiring dual-Damascene A/R (Cu wire/via)	2.3/2.1	2.3/2.1	2.3/2.1	2.4/2.2	2.4/2.2	2.4/2.2	2.5/2.3	2.5/2.3	2.5/2.3
WAS	Interconnect RC delay (ps) for 1 mm global line at minimum pitch	143		220	248		354	452		618
IS	Interconnect RC delay (ps) for a 1 mm Cu global wire, assumes no scattering and an effective ρ of 2.2 µΩ-cm	143	169	220	248	301	354	452	561	618

**Refer to Executive Summary Figure 4 for definition of Metal 1 pitch*

Manufacturable solutions exist, and are being optimized	⬜
Manufacturable solutions are known	🟨
Interim solutions are known	◆
Manufacturable solutions are NOT known	🟥

Table 81b MPU Interconnect Technology Requirements—Long-term UPDATED (continued)

		2010	2011	2012	2013	2014	2015	2016	2017	2018
	Technology Node	*hp45*			*hp32*			*hp22*		
	DRAM ½ Pitch (nm)	45	40	35	32	28	25	22	20	18
	MPU/ASIC ½ Pitch (nm)	54	48	42	38	34	30	27	24	21
	MPU Printed Gate Length (nm)	25	22	20	18	16	14	13	11	10
	MPU Physical Gate Length (nm)	18	16	14	13	11	10	9	8	7
ADD	**Interconnect RC delay (ps) for 1 mm Cu min. pitch global wire, assumes width-dependent scattering and a conformal barrier of thickness specified below**	**189**	**238**	**308**	**396**	**468**	**596**	**767**	**983**	**1189**
ADD	**Conductor effective resistivity (µΩ-cm) Cu global wiring including effect of width-dependent scattering and a conformal barrier of thickness specified below**	**2.74**	**2.81**	**2.89**	**3.04**	**3.1**	**3.2**	**3.37**	**3.5**	**3.6**
ADD	Barrier/cladding thickness (for min. pitch Cu global wiring) (nm) **[3]**	**4.9**	**4.5**	**4**	**3.6**	**3.3**	**2.9**	**2.5**	**2.2**	**2**
WAS	Line length (mm) where τ = RC delay (global wire at minimum pitch)	**52**		**37**	**30**		**23**	**19**		**13**
IS	Line length (µm) where τ = RC delay (global wire at minimum pitch - no scattering)	**52**	**44**	**37**	**30**	**26**	**23**	**19**	**16**	**13**
WAS	Cu thinning of maximum width global wiring due to dishing and erosion (nm), 10% × height, 80% areal density	**155**		**127**	**148**		**122**	**130**		**130**
IS	Cu thinning of maximum width global wiring due to dishing and erosion (nm), 10% × height, 80% areal density	**155**	**140**	**127**	**148**	**134**	**122**	**130**	**120**	**130**
WAS	Cu thinning global wiring due to dishing (nm), 100 µm wide feature	**14**		**13**	**10**		**9**	**8**		**7**
IS	Cu thinning global wiring due to dishing (nm), 100 µm wide feature	**14**	**13**	**13**	**10**	**10**	**9**	**8**	**7**	**7**
WAS	Conductor effective resistivity (µΩ-cm) Cu intermediate wiring	**2.2**		**2.2**	**2.2**		**2.2**	**2.2**		**2.2**
IS	Conductor effective resistivity (µΩ-cm) Cu wiring, assumes **no scattering**	**2.2**	**2.2**	**2.2**	**2.2**	**2.2**	**2.2**	**2.2**	**2.2**	**2.2**
WAS	Interlevel metal insulator – effective dielectric constant (κ)	**2.3-2.6**		**2.3-2.6**	**2.0-2.4**		**2.0-2.4**	**<2.0**		**<2.0**
IS	Interlevel metal insulator – effective dielectric constant (κ)**[4]**	**2.3-2.6**	**2.3-2.6**	**2.3-2.6**	**2.0-2.4**	**2.0-2.4**	**2.0-2.4**	**<2.0**	**<2.0**	**<2.0**
WAS	Interlevel metal insulator (minimum expected) – bulk dielectric constant (κ)	**<2.1**		**<2.1**	**<1.9**		**<1.9**	**<1.7**		**<1.7**
IS	Interlevel metal insulator (minimum expected) – bulk dielectric constant (κ)	**<2.1**	**<2.1**	**<2.1**	**<1.9**	**<1.9**	**<1.9**	**<1.7**	**<1.7**	**<1.7**

**Refer to Executive Summary Figure 4 for definition of Metal 1 pitch*

Manufacturable solutions exist, and are being optimized	⬜
Manufacturable solutions are known	🟨
Interim solutions are known	◆
Manufacturable solutions are NOT known	🟥

Notes for Tables 81a and 81b:
[1] Calculated by assuming that only one of every three minimum pitch wiring tracks for local and semi-global wiring levels are populated. The wiring lengths for each level are then summed to calculate the total interconnect length per square centimeter of active area.
[2] This metric is calculated by assuming that a 5 FIT reliability budget is apportioned to interconnect for the highest reliability grade MPUs. This number is then divided by the total interconnect length to arrive at the FITs per meter of wiring per one square centimeter of active area.
[3] Calculated for a conformal layer in intermediate wiring to meet minimum effective conductor resistivity.

[4] Achievement of these effective dielectric constant targets will require: at the 45 nm and 32 nm node (for an effective dielectric constant of 2.5) bulk dielectric constant of k<2.2 with minimal sidewall damage from etch, ash or cleans, hard-mask, and dielectric barrier layers all of k<2.8 and total thickness not exceeding 26 nm, along with elimination of the trench etch-stop; at the 22nm node virtually damage free processing (etch ash, clean, cmp, metal barrier deposition) is required, with the trench etch stop eliminated and any hard-mask, and/or dielectric barrier layers must all be of k<2.2.

Table 82a DRAM Interconnect Technology Requirements—Near-term UPDATED

	Year of Production	*2003*	*2004*	*2005*	*2006*	*2007*	*2008*	*2009*
	Technology Node		*hp90*			*hp65*		
	DRAM ½ Pitch (nm)	*100*	*90*	*80*	*70*	*65*	*57*	*50*
	MPU/ASIC ½ Pitch (nm)	*107*	*90*	*80*	*70*	*65*	*57*	*50*
	MPU Printed Gate Length (nm)	*65*	*53*	*45*	*40*	*35*	*32*	*28*
	MPU Physical Gate Length (nm)	*45*	*37*	*32*	*28*	*25*	*22*	*20*
	Number of metal layers	**4**	**4**	**4**	**4**	**4**	**4**	**4**
	Contact A/R – stacked capacitor	**13**	**15**	**15**	**16**	**16**	**17**	**17**
	Metal 1 wiring pitch (nm) *	**180**	**160**	**140**	**130**	**114**	**100**	**90**
WAS	Specific contact resistance (Ω-cm^2)	**1.00E-07**	**8.50E-08**	**7.00E-08**	**5.00E-08**	**4.00E-08**	**3.50E-08**	**3.00E-08**
IS	**Specific contact resistance (Ω-cm^2) for n^+ Si**	**3.80E-08**	**3.20E-08**	**2.50E-08**	**2.30E-08**	**2.00E-08**	**1.70E-08**	**1.40E-08**
IS	**Specific contact resistance (Ω-cm^2) for p^+ Si**	**8.20E-08**	**6.10E-08**	**4.50E-08**	**3.80E-08**	**3.20E-08**	**2.70E-08**	**2.20E-08**
WAS	Specific via resistance (Ω-cm^2)	**1.10E-09**	**9.00E-10**	**7.50E-10**	**5.80E-10**	**5.00E-10**	**4.00E-10**	**3.50E-10**
IS	Specific via resistance (Ω-cm^2)	**7.00E-10**	**7.00E-10**	**7.00E-10**	**6.00E-10**	**5.00E-10**	**4.00E-10**	**3.50E-10**
WAS	Conductor effective resistivity (μΩ-cm)	**3.3**	**3.3**	**3.3**	**3.3**	**2.2**	**2.2**	**2.2**
IS	Conductor effective resistivity (μΩ-cm) **assumes no scattering for Cu**	**3.3**	**3.3**	**3.3**	**3.3**	**2.2**	**2.2**	**2.2**
	Interlevel metal insulator – effective dielectric constant (κ)	**3.6–4.1**	**3.6–4.1**	**3.6–4.1**	**3.6–4.1**	**3.1–3.6**	**3.1–3.6**	**3.1–3.6**

**Refer to Executive Summary Figure 4 for definition of Metal 1 pitch*

Manufacturable solutions exist, and are being optimized	⬜
Manufacturable solutions are known	🟨
Interim solutions are known	◆
Manufacturable solutions are NOT known	🟥

Table 82b DRAM Interconnect Technology Requirements—Long-term UPDATED

	Year of Production	*2010*	*2011*	*2012*	*2013*	*2014*	*2015*	*2016*	*2017*	*2018*
	Technology Node	*hp45*			*hp32*			*hp22*		
WAS	*DRAM ½ Pitch (nm)*	*45*	*40*	*35*	*32*	*28*	*25*	*22*	*20*	*18*
WAS	*MPU/ASIC ½ Pitch (nm)*	*45*		*35*	*32*		*25*	*22*		*18*
WAS	*MPU Printed Gate Length (nm)*	*25*		*20*	*18*		*14*	*13*		*10*
WAS	*MPU Physical Gate Length (nm)*	*18*		*14*	*13*		*10*	*9*		*7*
WAS	Number of metal levels	**4**		**4**	**4**		**4**	**4**		**4**
IS	Number of metal levels	**4**	**4**	**4**	**4**	**4**	**4**	**4**	**4**	**4**
WAS	Contact A/R – stacked capacitor	**>20**		**>20**	**>20**		**>20**	**>20**		**>20**
IS	Contact A/R – stacked capacitor	**>20**	**>20**	**>20**	**>20**	**>20**	**>20**	**>20**	**>20**	**>20**
WAS	Metal 1 wiring pitch (nm) *	**80**		**64**	**57**		**44**	**40**		**32**
IS	Metal 1 wiring pitch (nm) *	**80**	**70**	**64**	**57**	**50**	**44**	**40**	**36**	**32**
WAS	Specific contact resistance (Ω-cm^2)	**2.30E-08**		**1.60E-08**	**1.20E-08**		**7.70E-09**	**5.50E-09**		**3.90E-09**
IS	**Specific contact resistance (Ω-cm^2) for n^+ Si**	**1.20E-08**	**9.80E-09**	**8.20E-09**	**6.90E-09**	**5.80E-09**	**4.80E-09**	**4.00E-09**	**3.40E-09**	**2.80E-09**
IS	**Specific contact resistance (Ω-cm^2) for p^+ Si**	**1.80E-08**	**1.50E-08**	**1.30E-08**	**1.10E-08**	**9.20E-09**	**7.40E-09**	**6.20E-09**	**5.10E-09**	**4.30E-09**
WAS	Specific via resistance (Ω-cm^2)	**3.20E-10**		**2.20E-10**	**1.60E-10**		**1.00E-10**	**7.60E-11**		**5.00E-11**
IS	Specific via resistance (Ω-cm^2)	**2.90E-10**	**2.50E-10**	**2.10E-10**	**1.70E-10**	**1.40E-10**	**1.20E-10**	**1.00E-10**	**8.40E-11**	**7.00E-11**
WAS	Conductor effective resistivity (μΩ-cm)	**2.2**		**2.2**	**2.2**		**2.2**	**2.2**		**2.2**
IS	Conductor effective resistivity (μΩ-cm) assumes **no scattering**	**2.2**	**2.2**	**2.2**	**2.2**	**2.2**	**2.2**	**2.2**	**2.2**	**2.2**
WAS	Interlevel metal insulator – effective dielectric constant (κ)	**2.7–3.1**		**2.7–3.1**	**2.7–3.1**		**2.7–3.1**	**2.0–2.4**		**2.0–2.4**
IS	Interlevel metal insulator – effective dielectric constant (κ)	**2.7–3.1**	**2.7-3.1**	**2.7–3.1**	**2.7–3.1**	**2.7-3.1**	**2.7–3.1**	**2.0–2.4**	**2.0-2.4**	**2.0–2.4**

**Refer to Executive Summary Figure 4 for definition of Metal 1 pitch*

Manufacturable solutions exist, and are being optimized	⬜
Manufacturable solutions are known	🟨
Interim solutions are known	◆
Manufacturable solutions are NOT known	🟥

Notes for Tables 82a and 82b:

[1] Calculated by assuming that only one of every three minimum pitch wiring tracks for local and semi-global wiring levels are populated. The wiring lengths for each level are then summed to calculate the total interconnect length per square centimeter of active area.

[2] This metric is calculated by assuming that a 5 FIT reliability budget is apportioned to interconnect for the highest reliability grade MPUs. This number is then divided by the total interconnect length to arrive at the FITs per meter of wiring per one square centimeter of active area.

[3] Calculated for a conformal layer in intermediate wiring to meet minimum effective conductor resistivity.

Table 83a Interconnect Surface Preparation Technology Requirements—Near-term*

Year of Production	*2003*	*2004*	*2005*	*2006*	*2007*	*2008*	*2009*	*Driver*
Technology Node		*hp90*			*hp65*			
DRAM ½ Pitch (nm)	*100*	*90*	*80*	*70*	*65*	*57*	*50*	*D ½*
MPU/ASIC ½ Pitch (nm)	*107*	*90*	*80*	*70*	*65*	*57*	*50*	*M*
MPU Printed Gate Length (nm)	*65*	*53*	*45*	*40*	*35*	*32*	*28*	*M*
MPU Physical Gate Length (nm)	*45*	*37*	*32*	*28*	*25*	*22*	*20*	*M*
Wafer diameter (mm)	**300**	**300**	**300**	**300**	**300**	**300**	**300**	*D ½, M*
Wafer edge exclusion (mm)	**2**	**2**	**2**	**2**	**2**	**2**	**2**	*D ½, M*
Front surface particles								
Killer defect density, D_pR_p (#/cm^2) [A]	**0.0172**	**0.0217**	**0.0283**	**0.0185**	**0.0233**	**0.0158**	**0.0199**	*D ½*
Critical particle diameter, d_c (nm) [B]	**50**	**45**	**40**	**35**	**32.5**	**27.5**	**25**	*D ½*
Critical particle density, D_{pw} (#/wafer) [C]	**59**	**75**	**97**	**64**	**80**	**54**	**68**	*D ½*
Back surface particles								
Back surface critical particle diameter (nm) [D]	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	*D ½, M*
Back surface critical particle density (#/wafer) [E]	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	*D ½, M*
Edge bevel particles								
Edge bevel critical particle diameter (nm) [F]	**200**	**180**	**160**	**140**	**130**	**114**	**100**	*D ½, M*
Particles (cm^{-2}) (G)	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	*M*
Particles (#/wafer) (G)	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	*M*
Metallic Contamination								
Critical front surface metals (10^9 atoms/cm^2) (H)	**50**	**50**	**10**	**10**	**10**	**10**	**10**	*M*
Critical back surface metals (Cu) (10^9 atoms/cm^2) (I)	**1000**	**1000**	**1000**	**1000**	**500**	**500**	**500**	*M*
Mobile ions (10^{10} atoms/cm^2) [J]	**5**	**5**	**5**	**5**	**2.5**	**2.5**	**2.5**	*D ½*
Organic contamination (10^{13} C atoms/cm^2) [K]	**1.8**	**1.6**	**1.4**	**1.3**	**1.2**	**1**	**0.9**	*M*
Cleaning Effects on Dielectric Material								
Maximum dielectric constant increase due to Strip + Clean [L]	**4.00%**	**2.50%**	**2.50%**	**2.50%**	**2.50%**	**2.50%**	**2.50%**	*M*
Maximum dielectric constant increase due to rework [L]	**4.00%**	**2.50%**	**2.50%**	**2.50%**	**2.50%**	**2.50%**	**2.50%**	*M*
Maximum effect on dielectric critical dimension due to Strip + Clean [M]	**2.50%**	**2.50%**	**2.50%**	**2.50%**	**2.50%**	**2.50%**	**2.50%**	*M*

Manufacturable solutions exist, and are being optimized	⬜
Manufacturable solutions are known	🟨
Interim solutions are known	◆
Manufacturable solutions are NOT known	🟥

Table 83b Interconnect Surface Preparation Technology Requirements—Long-term UPDATED*

	Year of Production	*2010*	*2011*	*2012*	*2013*	*2014*	*2015*	*2016*	*2017*	*2018*	*Driver*
	Technology Node	*hp45*			*hp32*			*hp22*			
	DRAM ½ Pitch (nm)	*45*	*40*	*35*	*32*	*28*	*25*	*22*	*20*	*18*	*D ½*
WAS	*MPU / ASIC ½ Pitch (nm)*	*45*		*35*	*32*		*25*	*22*		*18*	*M*
IS	*MPU / ASIC ½ Pitch (nm)*	**45**	**35**	**35**	**32**	**25**	**25**	**22**	**18**	**18**	*M*
WAS	*MPU Printed Gate Length (nm)*	*25*		*20*	*18*		*14*	*13*		*10*	*M*
IS	*MPU Printed Gate Length (nm)*	**25**	**22**	**20**	**18**	**16**	**14**	**13**	**11**	**10**	*M*
WAS	*MPU Physical Gate Length (nm)*	*18*		*14*	*13*		*10*	*9*		*7*	*M*
IS	*MPU Physical Gate Length (nm)*	**18**	**16**	**14**	**13**	**11**	**10**	**9**	**8**	**7**	*M*
WAS	*Wafer diameter (mm)*	**300**		**300**	**300**		**450**	**450**		**450**	*D ½, M*
IS	*Wafer diameter (mm)*	**300**	**300**	**300**	**300**	**450**	**450**	**450**	**450**	**450**	*D ½, M*
WAS	*Wafer edge exclusion (mm)*	**2**		**2**	**2**		**2**	**2**		**2**	*D ½, M*
IS	*Wafer edge exclusion (mm)*	**2**	**2**	**2**	**2**	**2**	**2**	**2**	**2**	**2**	*D ½, M*
	Front surface particles										
WAS	Killer defect density, D_pR_p (#/cm^2) [A]	**0.025**		**0.0199**	**0.025**		**0.0199**	**0.0136**		**0.0215**	*D ½*
IS	Killer defect density, D_pR_p (#/cm^2) [A]	**0.025**	**0.016**	**0.0199**	**0.025**	**0.016**	**0.0199**	**0.0136**	**0.017**	**0.0215**	
WAS	Critical particle diameter, d_c (nm) [B]	**22.5**		**17.5**	**16**		**12.5**	**11**		**9**	*D ½*
IS	Critical particle diameter, d_c (nm) [B]	**22.5**	**20**	**17.5**	**16**	**14**	**12.5**	**11**	**10**	**9**	*D ½*
WAS	Critical particle density, D_{pw} (#/wafer) [C]	**86**		**155**	**195**		**155**	**106**		**168**	*D ½*
IS	Critical particle density, D_{pw} (#/wafer) [C]	**86**	**123**	**155**	**195**	**123**	**155**	**106**	**133**	**168**	*D ½*
	Back surface particles										
WAS	Back surface critical particle diameter (nm) [D]	**TBD**		**TBD**	**TBD**		**TBD**	**TBD**		**TBD**	*D ½, M*
IS	Back surface critical particle diameter (nm) [D]	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	*D ½, M*
WAS	Back surface critical particle density (#/wafer) [E]	**TBD**		**TBD**	**TBD**		**TBD**	**TBD**		**TBD**	*D ½, M*
IS	Back surface critical particle density (#/wafer) [E]	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	*D ½, M*
	Edge bevel particles										
WAS	Edge bevel critical particle diameter (nm) [F]	**90**		**70**	**64**		**50**	**44**		**36**	*D ½, M*
IS	Edge bevel critical particle diameter (nm) [F]	**90**		**70**	**64**		**50**	**44**		**36**	*D ½, M*
WAS	Particles (cm^{-2}) (G)	**TBD**		**TBD**	**TBD**		**TBD**	**TBD**		**TBD**	*M*
IS	Particles (cm^{-2}) (G)	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	*M*
WAS	Particles (#/wafer) (G)	**TBD**		**TBD**	**TBD**		**TBD**	**TBD**		**TBD**	*M*
IS	Particles (#/wafer) (G)	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	*M*

Manufacturable solutions exist, and are being optimized	⬜
Manufacturable solutions are known	🟨
Interim solutions are known	◆
Manufacturable solutions are NOT known	🟥

Table 83b Interconnect Surface Preparation Technology Requirements—Long-term UPDATED (continued)*

	Year of Production	*2010*	*2011*	*2012*	*2013*	*2014*	*2015*	*2016*	*2017*	*2018*	*Driver*
	Technology Node	*hp45*			*hp32*			*hp22*			
	DRAM ½ Pitch (nm)	*45*	*40*	*35*	*32*	*28*	*25*	*22*	*20*	*18*	*D ½*
	Metallic Contamination										
WAS	Critical front surface metals (10^{9} atoms/cm^{2}) (H)	**10**		**10**	**10**		**10**	**10**		**10**	*M*
IS	Critical front surface metals (10^{9} atoms/cm^{2}) (H)	**10**	**10**	**10**	**10**	**10**	**10**	**10**	**10**	**10**	*M*
WAS	Critical back surface metals (Cu) (10^{9} atoms/cm^{2}) (I)	**250**		**250**	**100**		**100**	**100**		**100**	*M*
IS	Critical back surface metals (Cu) (10^{9} atoms/cm^{2}) (I)	**250**	**250**	**250**	**100**	**100**	**100**	**100**	**100**	**100**	*M*
WAS	Mobile ions (10^{10} atoms/cm^{2}) [J]	**2.5**		**2.5**	**2.4**		**2.4**	**2.3**		**2.3**	*D ½*
IS	Mobile ions (10^{10} atoms/cm^{2}) [J]	**2.5**	**2.5**	**2.5**	**2.4**	**2.4**	**2.4**	**2.3**	**2.3**	**2.3**	*D ½*
WAS	Organic contamination (10^{13} C at/cm^{2}) [K]	**0.9**		**0.9**	**0.9**		**0.9**	**0.9**		**0.9**	*M*
IS	Organic contamination (10^{13} C atoms/cm^{2}) [K]	**0.9**	**0.9**	**0.9**	**0.9**	**0.9**	**0.9**	**0.9**	**0.9**	**0.9**	*M*
	Cleaning Effects on Dielectric Material										
WAS	Maximum dielectric constant increase due to Strip + Clean [L]	**2.00%**		**2.00%**	**2.00%**		**2.00%**	**0.00%**		**0.00%**	*M*
IS	Maximum dielectric constant increase due to Strip + Clean [L]	**2.00%**	**2.00%**	**2.00%**	**2.00%**	**2.00%**	**2.00%**	**0.00%**	**0.00%**	**0.00%**	*M*
WAS	Maximum dielectric constant increase due to rework [L]	**2.00%**		**2.00%**	**2.00%**		**2.00%**	**0.00%**		**0.00%**	*M*
IS	Maximum dielectric constant increase due to rework [L]	**2.00%**	**2.00%**	**2.00%**	**2.00%**	**2.00%**	**2.00%**	**0.00%**	**0.00%**	**0.00%**	*M*
WAS	Maximum effect on dielectric critical dimension due to Strip + Clean [M]	**2.50%**		**2.50%**	**2.50%**		**2.50%**	**2.50%**		**2.50%**	*M*
IS	Maximum effect on dielectric critical dimension due to Strip + Clean [M]	**2.50%**	**2.50%**	**2.50%**	**2.50%**	**2.50%**	**2.50%**	**2.50%**	**2.50%**	**2.50%**	*M*

Manufacturable solutions exist, and are being optimized	⬜
Manufacturable solutions are known	🟨
Interim solutions are known	◆
Manufacturable solutions are NOT known	🟥

Notes for Tables 83a and b:

*(A) Killer defect density is calculated from the formula for 99% yield, Y=0.99=exp[-DpRpAeff]. Aeff is the effective chip area, Dp is the defect density, and Rp is a defect kill factor indicating the probability that a given defect will kill the device. The product DpRp is the density of device-killing defects on the wafer. Rp is dependent on numerous things including the size and shape of the particle, the composition of the particle, and specifics of the device layout. In previous years, Rp was assumed to be 0.2 for any particle > the critical particle size, dc. Aeff is assumed to be the same as for Front End Surface Preparation. For DRAM, Aeff=2.5F2T+(1-aF2T/Achip)*0.6Achip. where F is the minimum feature size, a is the cell fill factor, T is the number of DRAM bits (transistors) per chip, and Achip is the DRAM chip size. For MPUs, Aeff=aT(GL)2, where GL is the gate length. Because Aeff can increase or decrease with each successive technology node, DpRp does not always decrease over time.*

(B) Critical particle diameter, dc, is defined by Yield Enhancement as ½ of the metal ½-pitch dimension. This should be considered an "effective" particle diameter as most particulate contamination is irregular in shape.

*(C) An example is provided which assumes that the kill factor, Rp, is 0.2 for all particles larger than the critical particle size. This is the assumption made in previous versions of the roadmap, but is not universally valid and is included only for purposes of an example calculation. Particles/wafer is calculated using [Rp*3.14159*(wafer radius-edge exclusion)2]. To convert from particles/wafer at the critical particle size to particles/wafer at an alterative size, a suggested conversion formula is: Dalternate=Dcritical*(dcritical/ dalternate)2*

(D) & (E) Metrics for critical back surface particle size and back surface particle count are not being listed in 2003. While it is recognized that back surface particles are important to control and are assessed during equipment qualification, there is no clear empirical or theoretical model which links back surface particles to device yield. In the past, arguments have been made that back surface particles affect device yield mainly at the lithographic steps by causing the front surface of the wafer to move out of the focal plane leading to critical dimension variations. However, it is not clear how the limited back surface contact achievable with pin chucks interacts with back surface particle density to cause front surface flatness variations. In addition, it is also not clear how lithographic depth-of-focus (DOF) will change from year to year as this is not specified in the lithography roadmap. In general, it is felt that a good rule is to control back surface particles at a critical diameter equal to one-half of the DOF for critical lithographic steps. In 2003, DOF is about 0.4 micron, so the critical back surface particle diameter is generally considered to be 0.2 micron.

It is not possible to measure absolute levels of back surface particles on in-process wafers due to large variations in back surface finish and films. A generally accepted practice is to process wafers with the polished front surface down in order to assess back surface particle adders for a particular process or operation. Current best practice indicates that back surface particle adders for any particular process step in 2003 should be less than 400 at 0.2 micron.

(F) & (G) Edge bevel critical particle size is taken as 2 DRAM ½ Pitch. The size was determined to be particles that could be shed and then distributed onto the wafer surface causing detrimental yield reduction. Few references exist correlating edge defects with yield, however, minimization of the particle size and density is important. The levels are still under evaluations, however, and no values are presented here, although current practices indicate edge bevel particle adders for any interconnect process step, in particular CMP, should be less than 4 defects per quadrant of the wafer. Again, this value should be treated as guidance, not a specification.*

(H) Front surface metallic contamination levels are based on degradation of yield from metallic diffusion into the transistor or leakage of the device from metal migration. Data shows that Cu levels <1E13 can cause interconnect leakage and <1E10 can cause transistor degradation. The ability of the Cu to diffuse into the dielectric and then through the silicon to the transistors is questionable as many references site Cu cannot diffuse though thick silicon, nevertheless, the lower the Cu contamination the better. The levels are still under evaluations, however, and the values presented here should be treated as guidance, not a specification.

(I) Back surface Cu contamination level are based on degradation of electrical parameters of the transistor caused by Cu diffusion through the silicon. Many studies have been undertaken that evaluates the effects of backside Cu contamination on the transistors. The most profound affect is TDDB due to electric field drift. Oxygen on the back surface prevents the diffusion into the silicon. However, once in the silicon the Cu will diffuse and precipitate, dependent on thermal treatments. Various references quote a concentration as high as 1E15 and other quote as low as 1E11 as degrading device performance, dependent on test device structures and film thicknesses. Again, the levels are still under evaluation and the values presented here should be treated as guidance, not a specification. Reference: A. A. Isrtatov and E. R. Weber, J. Electrochem. Soc. 149(1) G21(2002).

(J) Mobile ions for interconnect is less stringent than the front end line metrics. Although the mobile ions can lead to the same electrical degradation and do the same damage from migration though the dielectric, the oxide does getter some of the sodium. For backside contamination levels, use the front end values. For interconnect, the cause shown here are guidance as to allowable levels, approximately twice the value of the front end metrics.

WAS *(K) Organic contamination is usually in the form of a thin layer of hydrocarbon remaining on the wafer after resist strip and clean. Leaving this film may result in undesirable delamination of subsequently deposited layers. Carbon residues may also come from inadequately stripped resist or shedding of particles from process chambers. The same metric is used for interconnect as the front end, Dc at the 180nm corresponded to 10% carbon atom coverage of a bare silicon wafer (7.3E+13atoms/cm2). Dc for subsequent nodes was scaled linearly with the ratio of CD to 180nm. Dc = (CD/180)(7.3E+13)*

IS *(K) Organic contamination is usually in the form of a thin layer of hydrocarbon remaining on the wafer after resist strip and clean* ***and after post-CMP clean.*** *Leaving this film may result in undesirable delamination of subsequently deposited layers or "carbon spots" caused by a monolayer or more of BTA (benzotriazole)-copper complex.* ***A monolayer, about 1 nm of BTA on copper yield a carbon atom density of about 4E14 atoms/cm2.*** *Carbon residues may also come from inadequately stripped resist or shedding of particles from process chambers. The same metric is used for interconnect as the front end, Dc at the 180nm corresponded to 10% carbon atom coverage of a bare silicon wafer (7.3E+13atoms/cm2). Dc for subsequent nodes was scaled linearly with the ratio of CD to 180nm. Dc = (CD/180)(7.3E+13)*

WAS *(L) Stripping and cleaning processes are known to have a detrimental effect on the dielectric constant of insulating layers. This is especially true for porous dielectric materials. It is essential to minimize and eventually eliminate this effect. Rework of photolithographic patterning involves stripping and cleaning and can have similar effects on the dielectric constant. These values are guidance for allowable degradation of the dielectric constant.*

IS *(L) Stripping and cleaning processes are known to have a detrimental effect on the dielectric constant of insulating layers. This is especially true for porous dielectric materials. It is essential to minimize and eventually eliminate this effect. Rework of photolithographic patterning involves stripping and cleaning and can have similar effects on the dielectric constant. These values are guidance for allowable degradation of the dielectric constant.* ***Changes in dielectric constant are measured on blanket film MISCAP structures. While these materials are not directly representative of integrated structures, no in-plane structure can directly measure dielectric constant change specifically due to strip + cleans. Additional impacts to reliability can arise from residual fluorine. Methods should be considered to defluorinate films after strip + cleans.***

WAS *(M) Stripping and cleaning processes generally involve some removal of the insulator. In particular the carbon can be leaked from the CDO films, leaving a thin layer of SiOx. This must be minimized in order to maintain critical dimensions. These values are guidance for allowable degradation of the dielectric constant.*

IS ***(M)Current etch and strip methods can damage porous low-κ films through the removal of carbon species; however, the extent of this damage may not be fully determined until after subsequent wet cleans. The CD loss after etch and strip may be negligible, but, following wet clean, the CD loss may become significant. Because the clean can remove film thicknesses rendered vulnerable by the etch, the extent of CD loss after wet cleans can be the result of both the etch and cleans processes. While not explicit in measurable CD loss, bowing of the trench and via structures should be minimized to allow conformal liners and plating base deposition and to reduce copper voiding effects.***