INTERNATIONAL TECHNOLOGY ROADMAP FOR SEMICONDUCTORS

2004 UPDATE

Lithography

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2004 UPDATE HIGHLIGHTS

In the 2004 update of the ITRS Lithography tables, no significant changes were made to the coloring or values in the overall lithography requirements tables other than adding a definition of overlay. For the long term, solutions are not known to reach the overall lithographic requirements for resolution combined with adequate overlay or CD control for any circuit type with any known lithographic technology. The lithography working group has participated in discussion with working groups developing other chapters to define CD control requirements. The US and Japan working groups separately conducted simulation studies that concluded that <4nm 3σ CD control has no known solutions with any technology presently being developed. The simulations also predict that if the gate length in resist were increased, CD control would be improved. However, this change would require larger post-development linewidth reduction using reactive ion etching or other processes.

Significant changes were made to the tables on difficult challenges and potential solutions. In developing the 2004 update, working group members defined new criteria for evaluating near-term potential solutions. Solutions shown in the table for the present and next two nodes must address leading edge requirements in at least two geographic regions, and all infrastructure including resist and mask must be ready for the timing of the node. Solutions for three nodes or more in the future are somewhat more broad ranging and inclusive to encourage continued innovation. With these criteria 193nm wavelength exposure systems, including 193nm immersion systems, became dominant solutions for the next two nodes; in addition, 157-nm wavelength exposure was only listed with immersion as a less likely option. Furthermore, immersion lithography appears as potential solution at the 32-nm and 22-nm nodes. In the difficult challenges tables, stronger emphasis was placed on challenges related to immersion lithography. Continued emphasis was placed on challenges for implementing cost-effective post-optical lithography solutions.

Many individual parameters for masks and resist were evaluated, and colors or values were changed. In the tables of mask requirements, the scaling of data volume requirements was delayed by one year. Manufacturing solutions are also available for mask protection and for achieving phase and transmission control for attenuated phase shift masks in 2007 since the use of 157-nm wavelength technology is not likely before the 45-nm node. Pellicles and phase-shifting materials are mature for use with 193-nm wavelength exposure. Minor changes were made to the EUV and EPL mask tables. In the resist tables, thickness requirements for single layer and ultrathin layer resist strategies were merged since resist thickness will need to be less than 300nm to maintain aspect ratio values where the resist doesn't collapse. The range of resist dose for 193-nm wavelength exposure was increased, and the dose values for electron beam exposure were adjusted to account for sensitivity differences in resist for exposure with low and high beam energies. Furthermore, the definition of line width roughness was adjusted to account for metrology precision.

Link to the 2003 ITRS Lithography chapter

WORKING GROUP TABLES

Table 76 Lithography Difficult Challenges UPDATED

	Five Difficult Challenges/ ≥ 50 nm Through 2009	*Summary of Issues*
WAS	Optical masks with features for resolution enhancement and post-optical mask fabrication	--Registration, CD control, defectivity, and 157 nm pellicles; defect free multi-layer EUV substrates or EPL membrane masks --Equipment infrastructure (writers, inspection, repair)
IS	Optical masks with features for resolution enhancement and post-optical mask fabrication	**--Registration, CD control, defect control for optical masks** **--Development of defect free multi-layer EUV mask blanks or EPL membrane masks** **--Equipment infrastructure (writers, inspection, repair)** **--Data volume**
WAS	Cost Control and Return on Investment (ROI)	--Achieving constant/improved ratio of tool cost to throughput over time --Cost-effective resolution enhanced optical masks and post-optical masks --Sufficient lifetimes for the technologies --Resources for developing multiple technologies at the same time --High output, cost-effective, EUV light source
IS	Cost Control and Return on Investment (ROI)	**--Achieving constant/improved ratio of exposure related tool cost to throughput over time** **--Cost-effective resolution enhanced optical masks and post-optical masks** **--Sufficient lifetimes for exposure tool technologies** **--Resources for developing multiple technologies at the same time** **--ROI for small volume products**
WAS	Process Control	--Processes to control gate CDs to less than 1.8 nm (3 sigma) --New and improved alignment and overlay control methods independent of technology option to < 19 nm overlay --Accuracy of OPC
IS	Process Control	**--Processes to control gate CDs to less than 4nm (3 sigma)** **--New and improved alignment and overlay control methods independent of technology option to < 19 nm overlay** **--Accuracy of OPC, especially in presence of polarization effects** **--Control of flare in exposure tool** **--Lithography friendly design and design for manufacturing**
WAS	Resists for ArF, Immersion Lithography and F_2	--Outgassing, LER, SEM-induced CD changes, defects ≥ 30 nm.
IS	**Resists for 193nm and 193nm immersion lithography**	**--Outgassing and leaching during immersion** **--Reduction of line edge and line width roughness** **--Finding and eliminating defects >30nm in size** **--Reducing SEM-induced CD changes**
~~**Delete**~~	~~CaF_2~~	~~--Yield, cost, quality~~
IS	**Defect control**	**--Control of defects caused in immersion environment**

Table 76 Lithography Difficult Challenges (continued)

	Five Difficult Challenges/ < 45 nm Beyond 2010	
WAS	Mask Fabrication and Process Control	--Defect-free NGL masks --Equipment infrastructure (writers, inspection, repair) --Mask process control methods
IS	Mask Fabrication and Process Control	**--Defect-free NGL masks, especially for 1X masks for nanoimprint and EUVL mask blanks free of printable defects** **--Timeliness and capability of mask equipment infrastructure (writers, inspection, repair), especially for 1X masks** **--Mask process control methods and yield enhancement** **--Pellicles for 157nm immersion and protection of EUVL masks from defects without pellicles**
WAS	Metrology and Defect Inspection	--Capability for critical dimensions down to 7 nm and metrology for overlay down to 7.2 nm, and patterned wafer defect inspection for defects < 30 nm
IS	Metrology and Defect Inspection	**--Resolution and precision for critical dimension measurement down to 7 nm, including metrology for 2.2nm 3 sigma line width roughness** **--Metrology for overlay down to 7.2 nm** **--Defect inspection for patterned wafers for defects < 30 nm**
WAS	Cost Control and ROI	--Achieving constant/improved ratio of tool cost to throughput --Development of cost-effective post-optical masks --Achieving ROI for industry with sufficient lifetimes for the technologies
IS	**Cost Control and return on investment (ROI)**	**--Achieving constant/improved ratio of exposure related tool cost to throughput** **--Development of cost-effective optical and post-optical masks** **--Achieving ROI for industry with sufficient lifetimes for exposure tool technologies and ROI for small volume products**
WAS	Gate CD Control Improvements, Process Control, Resist Materials	--Development of processes to control gate CDs < 1 nm (3 sigma) with appropriate line-edge roughness --Development of new and improved alignment and overlay control methods independent of technology option to < 7.2 nm overlay
IS	Gate CD Control Improvements, Process Control, Resist Materials	**--Development of processes to control gate CDs < 4 nm (3 sigma) with appropriate line-edge roughness** **--Development of new and improved alignment and overlay control methods independent of technology option to < 7.2 nm overlay, especially for nanoimprint** **--Process control and design for low k1 lithography** **--Resists with high index of refraction, high index fluids and high index optical materials to extend optical immersion to its limits** **--Limits of chemically amplified resist sensitivity for <50-nm linewidths due to acid diffusion length**
WAS	Tools for Mass Production	--Optical and NGL exposure tools capable of meeting requirements of the Roadmap --EUV sources with power sufficient for high throughput
IS	Tools for Mass Production	**--Optical and NGL exposure tools capable of meeting requirements of the ITRS** **--High output, cost-effective EUV sources** **--CaF2 cost, yield, and quantity for 157nm immersion**

Table 77a Lithography Technology Requirements—Near-term UPDATED

	Year of Production	2003	2004	2005	2006	2007	2008	2009
	Technology Node		*hp90*			*hp65*		
	DRAM							
	DRAM ½ Pitch (nm)	100	90	80	70	65	57	50
	Contact in resist (nm)	130	110	100	90	80	70	60
	Contact after etch (nm)	115	100	90	80	70	65	55
WAS	*Overlay*	35	32	28	25	23	21	19
IS	***Overlay [A]***	35	32	28	25	23	21	19
	CD control (3 sigma) (nm)	12.2	11	9.8	8.6	8	7	6.1
	MPU							
	MPU/ASCI Metal 1 (M1) ½ pitch (nm)	120	107	95	85	76	67	60
	MPU ½ Pitch (nm) (uncontacted gate)	107	90	80	70	65	57	50
WAS	*MPU gate in resist (nm)*	◆ 65	53	45	40	35	32	28
IS	*MPU gate in resist (nm)*	65	◆ 53	45	40	35	32	28
	MPU gate length after etch (nm)	45	37	32	28	25	22	20
	Contact in resist (nm)	130	122	100	90	80	75	60
	Contact after etch (nm)	120	107	95	85	76	67	60
WAS	*Gate CD control (3 sigma) (nm)*	◆ 4.0	3.3	2.9	2.5	2.2	2	1.8
IS	*Gate CD control (3 sigma) (nm)*	◆ 4.0	◆ 3.3	2.9	2.5	2.2	2	1.8
	ASIC/LP							
	ASIC ½ Pitch (nm) (uncontacted gate)	107	90	80	70	65	57	50
	ASIC/LP gate in resist (nm)	90	75	65	53	45	40	36
WAS	*ASIC/LP gate length after etch (nm)*	65	53	45	37	32	28	25
IS	*ASIC/LP gate length after etch (nm)*	65	◆ 53	45	37	32	28	25
	Contact in resist (nm)	130	122	100	90	80	75	60
	Contact after etch (nm)	120	107	95	85	76	67	60
	CD control (3 sigma) (nm)	5.8	4.7	4	3.3	2.9	2.5	2.2
	Chip size (mm^2)							
	DRAM, introduction	485	383	568	419	662	449	356
	DRAM, production	139	110	82	122	97	131	104
	MPU, high volume at introduction	280	280	280	280	280	280	280
	MPU, high volume at production	140	140	140	140	140	140	140
	MPU, high performance	310	310	310	310	310	310	310
	ASIC	704	704	704	704	704	704	704
	Minimum field area	704	704	704	704	704	704	704
	Wafer size (diameter, mm)	300	300	300	300	300	300	300

Manufacturable solutions exist, and are being optimized (white)
Manufacturable solutions are known (yellow)
Interim solutions are known (◆)
Manufacturable solutions are NOT known (red)

Notes for Table 77a—Lithography Technology Requirements—Near-term:

ADD	*[A] Overlay—Overlay is a vector component (in X and Y directions) quantity defined at every point on the wafer. It is the difference, O, between the vector position, P1, of a substrate geometry, and the vector position of the corresponding point, P2, in an overlaying pattern, which may consist of resist. O=P1-P2. The difference, O, is expressed in terms of vector components in the X and Y directions, and the value shown is three times the standard deviation of overlay values on the wafer.*

Table 77b Lithography Technology Requirements—Long-term UPDATED

	Year of Production	2010	2011	2012	2013	2014	2015	2016	2017	2018
	Technology Node	hp45			hp32			hp22		
	DRAM									
WAS	DRAM ½ Pitch (nm)	45	40	35	32	28	25	22	20	18
IS	DRAM ½ Pitch (nm)	45	40	35	32	28	25	22	20	18
WAS	Contact in resist (nm)	55		45	40		35	30		25
IS	Contact in resist (nm)	55	50	45	40	37	35	30	27	25
WAS	Contact after etch (m)	50		35	30		25	21		18
IS	Contact after etch (m)	50	40	35	30	28	25	21	20	18
WAS	Overlay	18		14	12.8		10	8.8		7.2
IS	**Overlay [A]**	18	16	14	13	12	10	8.8	8	7.2
WAS	CD control (3 sigma) (nm)	5.5		4.3	3.9		3.1	2.7		2.2
IS	CD control (3 sigma) (nm)	5.5	4.8	4.3	3.9	3.4	3.1	2.7	2.4	2.2
	MPU									
WAS	MPU/ASCI Metal 1 (M1) ½ pitch (nm)	54		42	38		30	27		21
IS	MPU/ASCI Metal 1 (M1) ½ pitch (nm)	54	48	42	38	34	30	27	24	21
WAS	MPU ½ Pitch (nm) (uncontacted gate)	45		35	32		25	22		18
IS	MPU ½ Pitch (nm) (uncontacted gate)	45	40	35	32	28	25	22	20	18
WAS	MPU gate in resist (nm)	25		20	18		15	13		10
IS	MPU gate in resist (nm)	25	22	20	18	17	15	13	11	10
WAS	MPU gate length after etch (nm)	18		14	13		10	9		7
IS	MPU gate length after etch (nm)	18	16	14	13	11	10	9	8	7
WAS	Contact in resist (nm)	59		46	42		33	30		23
IS	Contact in resist (nm)	59	53	46	42	37	33	30	26	23
WAS	Contact after etch (nm)	54		42	38		30	27		21
IS	Contact after etch (nm)	54	48	42	38	34	30	27	24	21
WAS	CD control (3 sigma) (nm)	1.6		1.3	1.2		0.9	0.8		0.6
IS	CD control (3 sigma) (nm)	1.6	1.4	1.3	1.2	1.0	0.9	0.8	0.7	0.6
	ASIC/LP									
WAS	ASIC ½ Pitch (nm) (uncontacted gate)	45		35	32		25	22		16
IS	ASIC ½ Pitch (nm) (uncontacted gate)	45	40	35	32	28	25	22	19	16
WAS	ASIC/LP gate in resist (nm)	32		27	22		19	16		13
IS	ASIC/LP gate in resist (nm)	32	30	27	22	20	19	16	14	13
WAS	ASIC/LP gate length after etch (nm)	22		19	16		14	11		9
IS	ASIC/LP gate length after etch (nm)	22	20	19	16	15	14	11	10	9
WAS	Contact in resist (nm)	59		46	42		33	30		23
IS	Contact in resist (nm)	59	52	46	42	37	33	30	26	23
WAS	Contact after etch (nm)	54		42	38		30	27		21
IS	Contact after etch (nm)	54	47	42	38	34	30	27	24	21
WAS	CD control (3 sigma) (nm)	2		1.7	1.4		1.3	1		0.8
IS	CD control (3 sigma) (nm)	2	1.8	1.7	1.4	1.3	1.3	1	0.9	0.8

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known

Table 77b Lithography Technology Requirements—Long-term (continued)

	Year of Production	2010	2011	2012	2013	2014	2015	2016	2017	2018
	Technology Node	hp45			hp32			hp22		
	Chip size (mm^2)									
WAS	DRAM, introduction	563		353	560		351	464		292
IS	DRAM, introduction	563	458	353	560	456	351	464	378	292
WAS	DRAM, production	83		104	83		104	138		87
IS	DRAM, production	83	94	104	83	94	104	138	113	87
WAS	MPU, high volume at introduction	280		280	280		280	280		280
IS	MPU, high volume at introduction	280	280	280	280	280	280	280	280	280
WAS	MPU, high volume at production	140		140	140		140	140		140
IS	MPU, high volume at production	140	140	140	140	140	140	140	140	140
WAS	MPU, high performance	310		310	310		310	310		310
IS	MPU, high performance	310	310	310	310	310	310	310	310	310
WAS	ASIC	704		704	704		704	704		704
IS	ASIC	704	704	704	704	704	704	704	704	704
WAS	Minimum field area	704		704	704		704	704		704
IS	Minimum field area	704	704	704	704	704	704	704	704	704
WAS	Wafer size (diameter, mm)	300		450	450		450	450		450
IS	Wafer size (diameter, mm)	300	300	450	450	450	450	450	450	450

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known

Notes for Table 77b—Lithography Technology Requirements—Long-term:

ADD	*[A] Overlay—Overlay is a vector component (in X and Y directions) quantity defined at every point on the wafer. It is the difference, O, between the vector position, P1, of a substrate geometry, and the vector position of the corresponding point, P2, in an overlaying pattern, which may consist of resist. O=P1-P2. The difference, O, is expressed in terms of vector components in the X and Y directions, and the value shown is three times the standard deviation of overlay values on the wafer.*

Table 78a Resist Requirements—Near-term UPDATED

	Year of Production	2003	2004	2005	2006	2007	2008	2009
	Technology Node		*hp90*			*hp65*		
	DRAM ½ Pitch (nm)	*100*	*90*	*80*	*70*	*65*	*57*	*50*
	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	**120**	**107**	**95**	**85**	**76**	**67**	**60**
	MPU/ASIC ½ Pitch (nm) (un-contacted gate)	**107**	**90**	**80**	**70**	**65**	**57**	**50**
	MPU Gate in resist Length (nm)	**65**	**53**	**45**	**40**	**35**	**32**	**28**
	MPU Gate Length after etch (nm)	**45**	**37**	**32**	**28**	**25**	**22**	**20**
	*Resist Characteristics **							
WAS	*Resist meets requirements for gate resolution and gate CD control (nm, 3 sigma) ***	◆ **4.0**	**3.3**	**2.9**	**2.5**	**2.2**	**2**	**1.8**
IS	*Resist meets requirements for gate resolution and gate CD control (nm, 3 sigma) ***	◆ **4.0**	◆ **3.3**	**2.9**	**2.5**	**2.2**	**2**	**1.8**
WAS	*Resist thickness (nm, imaging layer) ****	**250–400**	**220–360**	**200–320**	**170–250**	**160–220**	**140–200**	**130–180**
IS	***Resist thickness (nm, single layer) ******	**200–350**	**180–315**	**160–280**	**140–245**	**130–225**	**115–200**	**100–175**
WAS	*Ultra thin resist thickness (nm)*****	**120–150**	**120–150**	**120–150**	**100–150**	**100–130**	**100–130**	**80-120**
~~DELETE~~	~~*Resist thickness (nm, imaging layer) *****~~	~~**120–150**~~	~~**120–150**~~	~~**120–150**~~	~~**100–150**~~	~~**100–130**~~	~~**100–130**~~	~~**80-120**~~
	PEB temperature sensitivity (nm/C)	**2.5**	**2**	**2**	**1.5**	**1.5**	**1.5**	**1.5**
	Backside particles (particles/m^2 at critical size, nm)	**2000 @ 150**	**2000 @ 150**	**1500 @ 100**	**1500 @ 100**	**1500 @ 100**	**1500 @ 100**	**1000 @ 50**
WAS	*Defects in spin-coated resist films† #/cm^2*	**0.02**	**0.01**	**0.01**	**0.01**	**0.01**	**0.01**	**0.01**
IS	*Defects in spin-coated resist films† #/cm^2*	**0.02**	◆**0.01**	**0.01**	**0.01**	**0.01**	**0.01**	**0.01**
WAS	*(size in nm)*	**60**	**55**	**50**	**45**	**40**	**35**	**30**
IS	*(size in nm)*	**60**	◆**55**	**50**	**45**	**40**	**35**	**30**
WAS	*Defects in patterned resist films, gates, contacts, etc. #/cm^2*	**0.07**	**0.06**	**0.05**	**0.04**	**0.04**	**0.03**	**0.03**
IS	*Defects in patterned resist films, gates, contacts, etc. #/cm^2*	**0.07**	◆**0.06**	**0.05**	**0.04**	**0.04**	**0.03**	**0.03**
WAS	*(size in nm)*	**60**	**55**	**50**	**45**	**40**	**35**	**30**
IS	*(size in nm)*	**60**	◆**55**	**50**	**45**	**40**	**35**	**30**
WAS	*Line Width Roughness (nm, 3 sigma) <8% of CD *******	◆ **3.6**	**3**	**2.6**	**2.2**	**2**	**1.8**	**1.6**
IS	*Line Width Roughness (nm, 3 sigma) <8% of CD* *********	**5.2**	**4.2**	**3.6**	**3.2**	**2.8**	**2.6**	**2.2**

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known ◆
Manufacturable solutions are NOT known

Table 78b Resist Requirements—Long-term UPDATED

		2010	2011	2012	2013	2014	2015	2016	2017	2018
	Year of Production	2010	2011	2012	2013	2014	2015	2016	2017	2018
	Technology Node	hp45			hp32			hp22		
	DRAM ½ Pitch (nm)	45	40	35	32	28	25	22	20	18
	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	54		42	38		30	27		21
	MPU/ASIC ½ Pitch (nm)	45		35	32		25	22		18
	MPU Printed Gate Length (nm)	25		20	18		15	13		10
	MPU Physical Gate Length (nm)	18		14	13		10	9		7
	*Resist Characteristics **									
WAS	*Resist meets requirements for resolution and gate CD Control (nm, 3 sigma) ***	1.6		1.3	1.2		0.9	0.8		0.6
IS	*Resist meets requirements for gate resolution and gate CD control (nm, 3 sigma) ***	1.8	1.4	1.3	1.2	1	0.9	0.9	0.7	0.6
WAS	*Resist thickness (nm, imaging layer) ****	120–160		80–140	80–140		60–100	50–80		40–70
IS	***Resist thickness (nm, single layer) ******	90-160	80-140	70-120	65-110	55-100	50-90	45-80	40-70	35-65
WAS	*Ultra thin resist thickness (nm)*****	80–120		60–100	60–100		40–80	40–60		40–60
Delete	~~*Resist thickness (nm, imaging layer) *****~~	~~80–120~~	-	~~60–100~~	~~60–100~~	-	~~40–80~~	~~40–60~~	-	~~40–60~~
WAS	*PEB temperature sensitivity (nm/C)*	1.5		1.5	1		1	1		1
IS	*PEB temperature sensitivity (nm/C)*	1.5	1.5	1.5	1	1	1	1	1	1
WAS	*Backside particles (particles/m^2 at critical size, nm)*	1000 @ 50		1000 @ 50	1000 @ 50		1000 @ 50	500 @ 50		500 @ 50
IS	*Backside particles (particles/m^2 at critical size, nm)*	1000 @ 50	1000 @ 50	1000 @ 50	1000 @ 50	1000 @ 50	1000 @ 50	500 @ 50	500 @ 50	500 @ 50
WAS	*Defects in spin-coated resist films† #/cm^2*	0.01		0.01	0.01		0.01	0.01		0.01
IS	*Defects in spin-coated resist films† #/cm^2*	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
WAS	*(size in nm)*	30		20	20		10	10		10
IS	*(size in nm)*	30	20	20	20	20	10	10	10	10
WAS	*Defects in patterned resist films, gates, contacts, etc. #/cm^2*	0.03		0.01	0.01		0.01	0.01		0.01
IS	*Defects in patterned resist films, gates, contacts, etc. #/cm^2*	0.03	0.02	0.02	0.02	0.02	0.01	0.01	0.01	0.01
WAS	*(size in nm)*	30		20	20		10	10		10
IS	*(size in nm)*	30	20	20	20	20	10	10	10	10
WAS	*Line Width Roughness (nm, 3 sigma) <8% of CD *******	1.4		1.1	1		0.8	0.7		0.6
IS	*Line Width Roughness (nm, 3 sigma) <8% of CD ******	2	1.8	1.6	1.4	1.3	1.2	1	0.9	0.8

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known

Table 78c Resist Sensitivities UPDATED

	Exposure Technology	Sensitivity
	248 nm	**20–50 mJ/ cm^2**
WAS	*193 nm*	**10–30 mJ/ cm^2**
IS	*193 nm*	**10–50 mJ/ cm^2**
	157 nm	**5–15 mJ/ cm^2**
	Extreme Ultraviolet at 13.5 nm	**2–15 mJ/ cm^2**
WAS	*Electron Beam Projection at 100 kV ******	**2–10 uC/ cm^2**
IS	*High Voltage Electron Beam (50-100 kV) *****	**5–10 uC/ cm^2**
WAS	*E-beam Direct Write at 50 kV ******	**5–10 uC/ cm^2**
IS	*Low Voltage Electron Beam (1-2 kV) *****	**0.2–1.0 uC/ cm^2**

Notes for Tables 78a and 78b:

Exposure Dependent Requirements

* *Resist sensitivity is treated separately in the second resist sensitivities table (separate sheet).*

** *Indicates whether the resist has sufficient resolution, CD control, and profile to meet the resolution and gate CD control values.*

*** *Resist thickness is determined by the aspect ratio range of 2.5:1 to 4:1, limited by pattern collapse.*

IS *** *Resist thickness is determined by the aspect ratio range **of 2.0:1 to 3.5:1**, limited by pattern collapse.*

WAS **** *Resist thickness of top imaging layer of a multi-layer resist determined by opacity to the exposure source.*

Delete ~~**** *Resist thickness of top imaging layer of a multi-layer resist determined by opacity to the exposure source and etch resistance.*~~

WAS ***** *Linked with resolution.*

IS ******** *Linked with resolution.*

WAS ****** *LWR is 3σ of the linewidth over a range of spatial frequencies given by* $\frac{1}{P} \leq$ *spatial frequences* $\leq \frac{1}{0.5X_j}$ *, where P is the pitch and* X_j *is the low-end-of-range of the drain extension found in the Thermal and Thin Film, Doping and Etching Technology Requirements Table. LWR=SQRT(2)*LER.*

IS ******** LWR is 3σ deviation of the linewidth measured at less than or equal 10 nm intervals over a greater than or equal 2 micron line length.***

† Defects in coated films are those detectable as physical objects, such as pinholes, that may be distinguished from the resist film by optical detection methods.

Other requirements:

[A] Need for a positive tone resist and a negative tone resist will depend upon critical feature type and density.

[B] Feature wall profile should be 90 ±2 degrees.

[C] Thermal stability should be ≥130°C.

[D] Etching selectivity should be > that of poly hydroxystyrene (PHOST).

[E] Upon removal by stripping there should be no detectible residues.

[F] Sensitive to basic airborne compounds such as amines and amides. Clean handling space should have <1000 pptM of these materials.

[G] Metal contaminants < 5 ppb.

WAS *[H] Organic material outgassing (molecules/cm^2-sec) for two minutes (under the lens). Value for 157 nm lithography tool is <1e12. Value for EUV lithography tool is <5e13. Values for electron projection are being determined.*

IS *[H] Organic material outgassing (molecules/cm^2-sec) for two minutes (under the lens). Value for 157 nm lithography tool is <1e12. Value for EUV lithography tool is <5e13. Values for electron **beam** are being determined.*

WAS *[I] Si containing material outgassing (molecules/cm^2-sec) for two minutes (under the lens). Value for 157 nm lithography tool is <1e8. Value for EUV lithography tool is <5e13. Values for electron projection are being determined.*

IS *[I] Si containing material outgassing (molecules/cm^2-sec) for two minutes (under the lens). Value for 157 nm lithography tool is <1e8. Value for EUV lithography tool is <5e13. Values for electron **beam** are being determined.*

Table 79a Optical Mask Requirements UPDATED

	Year of Production	2003	2004	2005	2006	2007	2008	2009
	Technology Node		hp90			hp65		
	DRAM ½ Pitch (nm)	100	90	80	70	65	57	50
	MPU/ASIC ½ Pitch (nm)	120	107	95	85	76	67	60
	MPU Printed Gate Length (nm)	65	53	45	40	35	32	28
	MPU Physical Gate Length (nm)	45	37	32	28	25	22	20
	Wafer minimum half pitch (nm)	100	90	80	70	65	57	50
	Wafer minimum line (nm, in resist) [A]	◆ 65	53	45	40	35	32	30
	Wafer minimum line (nm, post etch)	45	37	32	28	25	22	20
	Overlay	35	32	28	25	23	21	19
	Wafer minimum contact hole (nm, post etch)	115	100	90	80	70	65	55
	Magnification [B]	4	4	4	4	4	4	4
WAS	Mask nominal image size (nm) [C]	260	212	180	160	140	128	112
IS	Mask nominal image size (nm) [C]	260	212	180	160	140	128	112
WAS	Mask minimum primary feature size [D]	182	148.4	126	112	98	89.6	78.4
IS	Mask minimum primary feature size [D]	182	148	126	112	98	90	78
	Mask OPC feature size (nm) clear	200	180	160	140	130	114	100
	Mask sub-resolution feature size (nm) opaque [E]	130	106	90	80	70	64	56
	Image placement (nm, multi-point) [F]	21	19	17	15	14	13	12
	CD uniformity allocation to mask (assumption)	0.4	0.4	0.4	0.4	0.4	0.4	0.4
	MEF isolated lines, binary [G]	1.4	1.4	1.4	1.4	1.6	1.6	1.6
WAS	CD uniformity (nm, 3 sigma) isolated lines (MPU gates), binary mask [H]	◆ 4.6	3.8	3.3	2.9	2.2	2	1.8
IS	CD uniformity (nm, 3 sigma) isolated lines (MPU gates), binary mask [H]	◆ 4.6	◆ 3.8	3.3	2.9	2.2	2	1.8
	MEF isolated lines, alternating phase shift [G]	1	1	1	1	1	1	1
WAS	CD uniformity (nm, 3 sigma) isolated lines (MPU gates), alternating phase shift mask [I]	6.4	5.3	4.6	4	3.6	3.1	2.9
IS	CD uniformity (nm, 3 sigma) isolated lines (MPU gates), alternating phase shift mask [I]	6.4	◆ 5.3	4.6	4	3.6	3.1	2.9
	MEF dense lines [G]	2	2	2	2	2.5	3	3
	CD uniformity (nm, 3 sigma) dense lines (DRAM half pitch), binary or attenuated phase shift mask [J]	9.8	8.8	7.8	6.9	5.1	3.7	3.3
	MEF contacts [G]	3	3	3	3	3.5	4	4
WAS	CD uniformity (nm, 3 sigma), contact/vias [K]	◆ 5.0	4.4	3.9	3.5	2.6	2.1	1.8
IS	CD uniformity (nm, 3 sigma), contact/vias [K]	◆ 5.0	◆ 4.4	3.9	3.5	2.6	2.1	1.8
	Linearity (nm) [L]	15.2	13.7	12.2	10.6	9.9	8.7	7.6
	CD mean to target (nm) [M]	8	7.2	6.4	5.6	5.2	4.6	4
	Defect size (nm) [N] *	80	72	64	56	52	45.6	40
	Substrate form factor	152 × 152 × 6.35						
	Blank flatness (nm, peak-valley) [O]	480	410	365	320	298	252	192
	Transmission uniformity to mask (pellicle and clear feature) (±% 3 sigma)	1	1	1	1	1	1	1
WAS	Data volume (GB) [P]	144	216	324	486	729	1094	1640
IS	Data volume (GB) [P]	96	144	216	324	486	729	1094
	Mask design grid (nm) [Q]	4	4	4	2	2	2	2

The requirements are for critical layers at defined year. Early volumes are assumed to be relatively small and difficult to produce.
180 degree phase defects are 70% of number shown.

Manufacturable solutions exist, and are being optimized (white)
Manufacturable solutions are known (yellow)
Interim solutions are known (◆)
Manufacturable solutions are NOT known (red)

Table 79a Optical Mask Requirements (continued

	Year of Production	2003	2004	2005	2006	2007	2008	2009
	Technology Node		hp90			hp65		
	DRAM ½ Pitch (nm)	100	90	80	70	65	57	50
	MPU/ASIC ½ Pitch (nm)	120	107	95	85	76	67	60
	MPU Printed Gate Length (nm)	65	53	45	40	35	32	28
	MPU Physical Gate Length (nm)	45	37	32	28	25	22	20
WAS	Attenuated PSM transmission mean deviation from target (± % of target) [R]	5	5	5	4	4	4	4
IS	Attenuated PSM transmission mean deviation from target (± % of target) [R]	5	5	5	4	4	4	4
WAS	Attenuated PSM transmission uniformity (±% of target) [R]	4	4	4	4	4	4	4
IS	Attenuated PSM transmission uniformity (±% of target) [R]	4	4	4	4	4	4	4
WAS	Attenuated PSM phase mean deviation from 180º (± degree) [S]	3	3	3	3	3	3	3
IS	Attenuated PSM phase mean deviation from 180º (± degree) [S]	3	3	3	3	3	3	3
	Alternating PSM phase mean deviation from nominal phase angle target 180º degrees (± degree) [S]	2	2	2	1	1	1	1
	Alternating PSM phase uniformity (± degree) [T]	2	◆ 2	◆ 2	1	1	1	1
WAS	Nominal reflectivity (%) [U]	20%	20%	15%	15%	15%	10%	10%
Delete	~~Nominal reflectivity (%) [U]~~	~~20%~~	~~20%~~	~~15%~~	~~15%~~	~~15%~~	~~10%~~	~~10%~~
WAS	Mask materials and substrates	Absorber on fused silica, except for 157 nm optical that will be absorber on fluorine doped, low OH fused silica substrate.						
IS	Mask materials and substrates	Absorber on fused silica						
WAS	Strategy for protecting mask from defects	Pellicle for optical masks down to 193 nm.				Modified fused silica pellicles have demonstrated feasibility for 157- nm scanners, and removable pellicles might be useful for small lot production. Research continues on organic membrane pellicles materials in a search for viable solutions.		
IS	Strategy for protecting mask from defects	Pellicle for optical masks for exposure wavelengths down to 193nm, including masks for 193nm immersion.						
WAS	(Exposure tool dependent)	Primary PSM choices are attenuated shifter and alternating aperture						
Delete	~~(Exposure tool dependent)~~	~~Primary PSM choices are attenuated shifter and alternating aperture~~						

The requirements are for critical layers at defined year. Early volumes are assumed to be relatively small and difficult to produce.
180 degree phase defects are 70% of number shown

Manufacturable solutions exist, and are being optimized	
Manufacturable solutions are known	
Interim solutions are known	◆
Manufacturable solutions are NOT known	

Notes for Table 79a—Optical Mask requirements:

[A] Wafer Minimum Line Size—Minimum wafer line size imaged in resists. Line size as drawn or printed to zero bias (Most commonly applied to isolated lines. Drives CD uniformity and linearity.)

[B] Magnification—Lithography tool reduction ratio, N:1.

[C] Mask Nominal Image Size— Equivalent to wafer minimum feature size in resist multiplied by the mask reduction ratio which equals 4×.

[D] Mask Minimum Primary Feature Size—Minimum printable feature after OPC application to be controlled on the mask for CD placement and defects.

[E] Mask Sub-Resolution Feature Size—The minimum width of isolated non-printing features on the mask such as sub-resolution assist features.

[F] Image Placement—The maximum component deviation (X or Y) of the array of the images centerline relative to a defined reference grid after removal of isotropic magnification error post pellicle mount. These values do not comprehend additional image placement error induced by pellicle mount and mask clamping in the exposure tool.

[G] The CD error on the wafer is directly proportional to the CD error on the mask where mask error factor (MEF) is the constant of proportionality. An MEF value greater than unity therefore imposes a more stringent CD uniformity requirement on the mask to maintain the CD uniformity budget on the wafer.

[H] CD Uniformity—The three-sigma deviation of actual image sizes on a mask for a single size and tone critical feature. Applies to features in X and Y and isolated features on a binary mask.

[I] CD Uniformity—The three-sigma deviation of actual image sizes on a mask for a single size and tone critical feature. Applies to features in X and Y and multiple pitch features on a quartz shifter phase mask.

[J] CD Uniformity—The three-sigma deviation of actual image sizes on a mask for a single size and tone critical feature. Applies to features in X and Y and multiple pitch features on a binary or attenuated phase shift mask.

[K] CD Uniformity—The three-sigma deviation of square root of contact area on a mask through multiple pitches.

[L] Linearity—Maximum deviation between mask "Mean to Target" for a range of features of the same tone and different design sizes. This includes features that are equal to the smallest sub-resolution assist mask feature and up to three times the minimum wafer half pitch multiplied by the magnification.

[M] CD Mean to Target—The maximum difference between the average of the measured feature sizes and the agreed to feature size (design size). Applies to a single feature size and tone. Σ(Actual-Target)/Number of measurements.

[N] Defect Size—A mask defect is any unintended mask anomaly that prints or changes a printed image size by 10% or more. The mask defect size listed in the roadmap are the square root of the area of the smallest opaque or clear "defect" that is expected to print for the stated generation.

[O] Blank Flatness—Flatness is nanometers, peak-to-valley across the 110 mm × 110 mm central area image field on a 6-inch × 6-inch square mask blank. Flatness is derived from wafer lithography DOF requirements for each node.

[P] Data Volume—This is the expected maximum file size for uncompressed data for a single layer as presented to a raster write tool.

[Q] Mask Design Grid—Wafer design grid multiplied by the mask magnification.

[R] Transmission—Ratio, expressed in percent, of the fraction of light passing through an attenuated PSM layer relative to the mask blank with no opaque films.

WAS *[S] Phase—Change in optical path length between two regions on the mask expressed in degrees.*

IS *[S] Phase—Change in optical path length between two regions on the mask expressed in degrees. The mean value is determined by averaging phase measured for many features on the mask.*

WAS *[T] Alt PSM phase uniformity is a range specification equal to the maximum phase error deviation of any point from the target.*

IS *[T] Alt PSM phase uniformity is a range specification equal to the maximum phase error deviation of any point from the mean value.*

[U] Optimization of mask reflectivity for wavelengths used for optical (laser) mask patterning versus optical inspection versus wafer exposure is a recognized issue to be addressed in the future.

Table 79b EUVL Mask Requirements UPDATED

		2008	2009	2010	2011	2012	2013	2014	2015	2016	2017	2018
	Year of Production	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*	*2014*	*2015*	*2016*	*2017*	*2018*
	Technology Node			*hp45*			*hp32*			*hp22*		
	DRAM ½ Pitch (nm)	*57*	*50*	*45*	*40*	*35*	*32*	*28*	*25*	*22*	*20*	*18*
WAS	*Wafer minimum half pitch (nm)*	57	50	45		35	32		25	22		18
IS	*Wafer minimum half pitch (nm)*	57	50	45	40	35	32	28	25	22	20	18
WAS	*Wafer minimum line (nm, in resist) [A]*	32	30	25		20	18		15	13		10
IS	*Wafer minimum line (nm, in resist) [A]*	32	28	25	23	20	18	17	15	13	12	10
WAS	*Wafer minimum line (nm, post etch)*	22	20	18		14	13		10	9		7
IS	*Wafer minimum line (nm, post etch*	22	20	18	16	14	13	12	10	9	8	7
WAS	*Overlay*	21	19	18		14	12.8		10	8.8		7.2
IS	*Overlay*	21	19	18	16	14	12.8	11	10	8.8	8	7.2
WAS	*Wafer minimum contact hole (nm, after etch)*	65	55	50		35	30		25	21		18
IS	*Wafer minimum contact hole (nm, after etch)*	65	55	50	43	35	30	28	25	21	20	18
	Generic Mask Requirements											
WAS	Magnification [B]	4	4	4		4	4		4	4		4
IS	Magnification [B]	4	4	4	4	4	4	4	4	4	4	4
WAS	Mask nominal image size (nm) [C]	128	120	100		80	72		60	52		40
IS	Mask nominal image size (nm) [C]	128	120	100	90	80	72	66	60	52	46	40
WAS	Mask minimum primary feature size [D]	114	100	90		70	64		50	44		36
IS	Mask minimum primary feature size [D]	114	100	90	80	70	64	57	50	44	40	36
WAS	Image placement (nm, multi-point) [E]	13	11.5	11	10	9	8		6	6		5
IS	Image placement (nm, multi-point) [E]	13	12	11	10	9	8	7	6	6	5	5
	CD Uniformity (nm, 3 sigma) [F]											
WAS	Isolated lines (MPU gates)	3.0	2.5	2.0		1.5	1.3		0.7	0.5		0.4
IS	Isolated lines (MPU gates)	3	2.5	2	1.8	1.5	1.3	1.0	0.7	0.5	0.5	0.4
WAS	Dense lines DRAM (half pitch)	12.5	11.0	9.0		6.5	5.5		2.0	1.5		1.0
IS	Dense lines DRAM (half pitch)	13	11	9	7.8	6.5	5.5	3.8	2	1.5	1.3	1
WAS	Contact/vias	8	7	6.5		4.5	3.5		2.5	2		1.5
IS	Contact/vias	8	7	6.5	5.5	4.5	3.5	3.0	2.5	2.0	1.8	1.5
WAS	Linearity (nm) [G]	8	7	6.5		5	4.5		3.5	3.5		2.5
IS	Linearity (nm) [G]	8	7	6.5	5.8	5	4.5	4.0	3.5	3.5	3.0	2.5
WAS	CD mean to target (nm) [H]	4	3.5	3		2.5	2		1.5	1.5		1
IS	CD mean to target (nm) [H]	4	3.5	3	2.8	2.5	2	1.8	1.5	1.5	1.3	1
WAS	Defect size (nm) [I]	40	36	32		26	23		18	16		13
IS	Defect size (nm) [I]	40	36	32	29	26	23	21	18	16	15	13
WAS	Data volume (GB) [J]	730	1096	1644		2466	3700		5550	8326		12490
IS	Data volume (GB) [J]	730	1096	1644	2055	2466	3700	4625	5550	8326	10408	12490
WAS	Mask design grid (nm) [K]	4	4	4		4	4		4	4		4
IS	Mask design grid (nm) [K]	2	2	2	2	2	2	2	2	2	2	2

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known

Table 79b EUVL Mask Requirements (continued)

	Year of Production	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*	*2014*	*2015*	*2016*	*2017*	*2018*
	Technology Node			*hp45*			*hp32*			*hp22*		
	DRAM ½ Pitch (nm)	*57*	*50*	*45*	*40*	*35*	*32*	*28*	*25*	*22*	*20*	*18*
	EUVL-specific Mask Requirements											
WAS	Substrate defect size (nm) [L]	30	29	27		24	23		19	18		14
IS	Substrate defect size (nm) [L]	30	29	27	26	24	23	21	19	18	16	14
WAS	Mean peak reflectivity	65%	66%	66%		67%	67%		67%	67%		67%
IS	Mean peak reflectivity	65%	66%	66%	66%	67%	67%	67%	67%	67%	67%	67%
WAS	Peak reflectivity uniformity (% 3 sigma absolute)	0.58%	0.56%	0.54%		0.48%	0.42%		0.36%	0.30%		0.24%
IS	Peak reflectivity uniformity (% 3 sigma absolute)	0.58%	0.56%	0.54%	0.51%	0.48%	0.42%	0.39%	0.36%	0.30%	0.27%	0.24%
WAS	Reflected centroid wavelength uniformity (nm 3 sigma) [M]	0.06	0.06	0.06		0.05	0.05		0.05	0.04		0.04
IS	Reflected centroid wavelength uniformity (nm 3 sigma) [M]	0.06	0.06	0.06	0.06	0.05	0.05	0.05	0.05	0.04	0.04	0.04
WAS	Minimum absorber sidewall angle (degrees)	85	85	85		85	85		85	85		85
~~DELETE~~		~~85~~	~~85~~	~~85~~	~~85~~	~~85~~	~~85~~	~~85~~	~~85~~	~~85~~	~~85~~	~~85~~
WAS	Absorber sidewall angle tolerance (± degrees)	1	1	0.75		0.62	0.5		0.5	0.5		0.5
IS	Absorber sidewall angle tolerance (± degrees) [P]	1	1	0.75	0.69	0.62	0.5	0.5	0.5	0.5	0.5	0.5
WAS	Absorber LER (3 sigma nm) [N]	4	4	3		2.5	90		3	2		2
IS	Absorber LER (3 sigma nm) [N]	4	4	3	3	2.5	2.5	3	3	2	2	2
WAS	Mask substrate flatness (nm peak-to-valley) [O]	◆65	◆60	55		45	40		30	25		20
IS	Mask substrate flatness (nm peak-to-valley) [O]	65	60	55	50	45	40	35	30	25	22	20
WAS	Maximum aspect ratio of absorber stack	1	1.1	1.3		1.4	1.5		1.6	1.7		1.7
IS	Maximum aspect ratio of absorber stack	1	1.1	1.3	1.4	1.4	1.5	1.5	1.6	1.7	1.7	1.7

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known ◆
Manufacturable solutions are NOT known

Notes for Table 79b—EUV Mask requirements:

EUVL masks are patterned absorber layers on top of multilayers that are deposited on low thermal expansion material substrates.

[A] Wafer Minimum Feature Size—Minimum wafer line size imaged in resists. Line size as drawn or printed to zero bias (Most commonly applied to isolated lines. Drives CD uniformity and linearity.)

[B] Magnification—Lithography tool reduction ratio, N:1.

[C] Mask Nominal Image Size— Equivalent to wafer minimum feature size in resist multiplied by the mask reduction ratio.

[D] Mask Minimum Primary Feature Size—Minimum printable feature after OPC application to be controlled on the mask for CD, placement, and defects.

[E] Image Placement—The maximum component deviation (X or Y) of the array of the images centerline relative to a defined reference grid after removal of isotropic magnification error.

[F] CD Uniformity—The three sigma deviation of actual image sizes on a mask for a single size and tone critical feature. Applies to features in X and Y and multiple pitches from isolated to dense. Contacts: Measure and tolerance refer to the area of the mask feature. For table simplicity the roadmap numbers normalize back to one dimension. sqrt (Area)—sqrt (Target Area).

[G] Linearity—Maximum deviation between mask "Mean to Target" for a range of features of the same tone and different design sizes. This includes features that are greater than the mask minimum primary feature size and up to three times the minimum wafer half pitch multiplied by the magnification.

[H] CD Mean to Target—The maximum difference between the average of the measured feature sizes and the agreed-to feature size (design size). Applies to a single feature size and tone. Σ(Actual-Target)/Number of measurements.

[I] Defect Size—A mask defect is any unintended mask anomaly that prints or changes a printed image size by 10% or more. The mask defect size listed in the roadmap are the square root of the area of the smallest opaque or clear "defect" that is expected to print for the stated generation.

[J] Data Volume—This is the expected maximum file size for uncompressed data for a single layer as presented to a raster write tool.

[K] Mask Design Grid—Wafer design grid multiplied by the mask magnification.

[L] Substrate Defect Size—the minimum diameter spherical defect (in polystyrene latex sphere equivalent dimensions) on the substrate beneath the multilayers that causes an unacceptable linewidth change in the printed image. Substrate defects might cause phase errors in the printed image and are the smallest mask blank defects that would unacceptably change the printed image.

[M] Includes variation in median wavelength over the mask area and mismatching of the average wavelength to the wavelength of the exposure tool optics.

[N] Line edge roughness (LER)—is defined a roughness 3 sigma one-sided for spatial period <mask primary feature size.

[O] Mask Substrate Flatness—Residual flatness error (nm peak-to-valley) over the mask excluding a 5 mm edge region on all sides after removing wedge, which may be compensated by the mask mounting and leveling method in the exposure tool. The flatness error is defined as the deviation of the surface from the plane that minimizes the maximum deviation. This flatness requirement applies to each of the front and backsides individually.

ADD *[P] The sidewall angle tolerance applies to the mean absorber sidewall angle agreed upon between mask user and supplier.*

Table 79c EPL Mask Requirements UPDATED

	Year of Production	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*	*2014*	*2015*	*2016*	*2017*	*2018*
	Technology Node			*hp45*			*hp32*			*hp22*		
	DRAM ½ Pitch (nm)	***57***	***50***	***45***	***40***	***35***	***32***	***28***	***25***	***22***	***20***	***18***
WAS	*Wafer minimum half pitch (nm) [A]*	**57**	**50**	**45**		**35**	**32**		**25**	**22**		**18**
IS	*Wafer minimum half pitch (nm) [A]*	**57**	**50**	**45**	**40**	**35**	**32**	**28**	**25**	**22**	**20**	**18**
WAS	*Wafer minimum line (nm, in resist)*	**32**	**30**	**25**		**20**	**18**		**15**	**13**		**10**
IS	*Wafer minimum line (nm, in resist)*	**32**	**30**	**25**	**22**	**20**	**18**	**17**	**15**	**13**	**11**	**10**
WAS	*Wafer minimum line (nm, post etch)*	**22**	**20**	**18**		**14**	**13**		**10**	**9**		**7**
IS	*Wafer minimum line (nm, post etch)*	**22**	**20**	**18**	**16**	**14**	**13**	**11**	**10**	**9**	**8**	**7**
WAS	*Overlay*	**21**	**19**	**18**		**14**	**12.8**		**10**	**8.8**		**7.2**
IS	*Overlay*	**21**	**19**	**18**	**16**	**14**	**13**	**12**	**10**	**8.8**	**8**	**7.2**
WAS	*Wafer minimum contact hole (nm, post etch)*	**65**	**55**	**50**		**35**	**30**		**25**	**21**		**18**
IS	*Wafer minimum contact hole (nm, post etch)*	**67**	**60**	**54**	**53**	**42**	**38**	**37**	**30**	**27**	**26**	**21**

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known

Table 79c EPL Mask Requirements UPDATED (continued)

	Year of Production	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*	*2014*	*2015*	*2016*	*2017*	*2018*
	Technology Node			*hp45*			*hp32*			*hp22*		
	DRAM ½ Pitch (nm)	***57***	***50***	***45***	***40***	***35***	***32***	***28***	***25***	***22***	***20***	***18***
Generic mask requirements												
WAS	Magnification [B]	**4**	**4**	**4**		**4**	**4**		**4**	**4**		**4**
IS	Magnification [B]	**4**	**4**	**4**	**4**	**4**	**4**	**4**	**4**	**4**	**4**	**4**
WAS	Mask minimum image size (nm) [C]	**89**	**84**	**70**		**56**	**50**		**42**	**36**		**28**
IS	Mask minimum image size (nm) [C]	**89**	**84**	**70**	**63**	**56**	**50**	**46**	**42**	**36**	**32**	**28**
WAS	Image placement error in sub-field (nm, multi-point) [D]	**9**	**8.5**	**8**		**6**	**5.5**		**4.5**	**4**		**3.5**
IS	Image placement error in sub-field (nm, multi-point) [D]	**9**	**8.5**	**8**	**7**	**6**	**5.5**	**5**	**4.5**	**4**	**3.8**	**3.5**
WAS	Sub-field placement error on mask (nm, 3 sigma, non-linear term) [E]	**9**	**8.5**	**8**		**6**	**5.5**		**4.5**	**4**		**3.5**
IS	Sub-field placement error on mask (nm, 3 sigma, non-linear term) [E]	**9**	**8.5**	**8**	**7**	**6**	**5.5**	**5**	**4.5**	**4**	**3.8**	**3.5**

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known

Table 79c EPL Mask Requirements UPDATED (continued)

	Year of Production	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*	*2014*	*2015*	*2016*	*2017*	*2018*
	Technology Node			*hp45*			*hp32*			*hp22*		
	DRAM ½ Pitch (nm)	***57***	***50***	***45***	***40***	***35***	***32***	***28***	***25***	***22***	***20***	***18***
CD Uniformity (nm, 3 sigma) [F]												
WAS	Isolated lines (MPU gates)	3	2.8	2.5		2	1.8		1.4	1.2		1
IS	Isolated lines (MPU gates)	3.0	2.8	2.5	2.3	2.0	1.8	1.6	1.4	1.2	1.1	1.0
WAS	Dense lines (DRAM half pitch)	13	12	9		7	6.5		5	4.5		4
IS	Dense lines (DRAM half pitch)	13	12	9	8	7	6.5	5.8	5	4.5	4.3	4
WAS	Contact/vias	8	7	6.5		3.5	2.5		3.5	3		2.5
IS	Contact/vias	8	7	6.5	6.0	5.5	4.9	4.4	3.9	3.5	3.1	2.7
WAS	Linearity (nm) [G]	9	8	7		5.5	5		4	3.5		3
IS	Linearity (nm) [G]	9	8	7	6.3	5.5	5	4.5	4	3.5	3.3	3
WAS	CD mean to target (nm) [H]	4.5	4	3.5		2.5	2.5		2	1.5		1
IS	CD mean to target (nm) [H]	4.5	4	3.5	3.0	2.5	2.5	2.2	2	1.5	1.2	1
WAS	Pattern corner rounding (nm)	35	31	28		22	20		16	14		11
IS	Pattern corner rounding (nm)	35	31	28	25	22	20	18	16	14	12.0	11
WAS	Defect size (nm) [I]	45	40	35		25	25		20	15		10
IS	Defect size (nm) [I]	45	40	35	30.0	25	25	22.0	20	15	12.0	10
WAS	Data volume (GB) [J]	730	1096	1644		2466	3700		5550	8326		12490
IS	Data volume (GB) [J]	730	1096	1644	2055	2466	3700	4625	5550	8326	10408	12490
WAS	Mask design grid (nm) [K]	4	4	4		4	4		4	4		4
IS	Mask design grid (nm) [K]	4	4	4	4	4	4	4	4	4	4	4

Table 79c EPL Mask Requirements UPDATED (continued)

	Year of Production	*2008*		*2009*		*2010*		*2011*		*2012*		*2013*		*2014*		*2015*		*2016*		*2017*		*2018*	
	Technology Node					*hp45*						*hp32*						*hp22*					
	DRAM ½ Pitch (nm)	***57***		***50***		***45***		***40***		***35***		***32***		***28***		***25***		***22***		***20***		***18***	
	EPL-specific Mask Requirements																						
WAS	Mask type	Mem-brane [T]	Stencil [U]	Mem-brane [T]	Stencil [U]	Mem-brane [T]	Stencil [U]	Mem-brane [T]	Stencil [U]	Mem-brane [T]	Stencil [U]	Mem-brane [T]	Stencil [U]	Mem-brane [T]	Stencil [U]	Mem-brane [T]	Stencil [U]	Mem-brane [T]	Stencil [U]	Mem-brane [T]	Stencil [U]	Mem-brane [T]	Stencil [U]
IS	Mask type																						
WAS	Clear area transmission factor [L]	50%	100%	50%	100%	50%	100%			70%	100%	70%	100%			70%	100%	70%	100%			70%	100%
IS	Clear area transmission factor [L]	50%	100%	50%	100%	50%	100%	50%	100%	70%	100%	70%	100%	70%	100%	70%	100%	70%	100%	70%	100%	70%	100%
WAS	Membrane thickness uniformity (3 sigma %) [M]	2%	N/A	2%	N/A	2%	N/A			2%	N/A	2%	N/A			2%	N/A	2%	N/A			2%	N/A
IS	Membrane thickness uniformity (3 sigma %) [M]	2%	N/A	2%	N/A	2%	N/A	2%	N/A	2%	N/A	2%	N/A	2%	N/A	2%	N/A	2%	N/A	2%	N/A	2%	N/A
WAS	Membrane thickness uniformity in sub-field (3 sigma %) [N]	1%	N/A	1%	N/A	1%	N/A			1%	N/A	1%	N/A			1%	N/A	1%	N/A			1%	N/A
IS	Membrane thickness uniformity in sub-field (3 sigma %) [N]	1%	N/A	1%	N/A	1%	N/A	1%	N/A	1%	N/A	1%	N/A	1%	N/A	1%	N/A	1%	N/A	1%	N/A	1%	N/A
WAS	Membrane mean thickness error (%) [O]	10%	N/A	10%	N/A	10%	N/A			10%	N/A	10%	N/A			10%	N/A	10%	N/A			10%	N/A
IS	Membrane mean thickness error (%) [O]	10%	N/A	10%	N/A	10%	N/A	10%	N/A	10%	N/A	10%	N/A	10%	N/A	10%	N/A	10%	N/A	10%	N/A	10%	N/A

Table 79c EPL Mask Requirements UPDATED (continued)

	Year of Production	2008		2009		2010		2011		2012		2013		2014		2015		2016		2017		2018	
	Technology Node					hp45						hp32						hp22					
	DRAM ½ Pitch (nm)	57		50		45		40		35		32		28		25		22		20		18	
WAS	Scatterer thickness uniformity in mask (3 sigma %) [P]	5%	5%	5%	5%	5%	5%			5%	5%	5%	5%			5%	5%	5%	5%			5%	5%
IS	Scatterer thickness uniformity in mask (3 sigma %) [P]	5%	5%	5%	5%	5%	5%	5%	5%	5%	5%	5%	5%	5%	5%	5%	5%	5%	5%	5%	5%	5%	5%
WAS	Scatterer mean thickness error (%) [Q]	10%	10%	10%	10%	10%	10%			10%	10%	10%	10%			10%	10%	10%	10%			10%	10%
IS	Scatterer mean thickness error (%) [Q]	10%	10%	10%	10%	10%	10%	10%	10%	10%	10%	10%	10%	10%	10%	10%	10%	10%	10%	10%	10%	10%	10%
WAS	Pattern sidewall angle (degrees)	90	90	90	90	90	90			90	90	90	90			90	90	90	90			90	90
IS	Pattern sidewall angle (degrees)	90	90	90	90	90	90	90	90	90	90	90	90	90	90	90	90	90	90	90	90	90	90
WAS	Pattern sidewall angle tolerance (+ degrees) [R]	0.3		0.3		0.3				0.3		0.3				0.3		0.3				0.3	
IS	Pattern sidewall angle tolerance (+ degrees) [R]	0.3		0.3		0.3		0.3		0.3		0.3		0.3		0.3		0.3		0.3		0.3	
WAS	Scatterer/stencil LER (3 sigma nm) [S]	4.5		4		3.5				3		3				3		3				3	
IS	Scatterer/stencil LER (3 sigma nm) [S]	4.5		4		3.5		3.2		3		3		3		3		3		3		3	

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known

Table 79c EPL Mask Requirements UPDATED (continued)

	Year of Production	2008	2009	2010	2011	2012	2013	2014	2015	2016	2017	2018
	Technology Node			*hp45*			*hp32*			*hp22*		
	DRAM ½ Pitch (nm)	**57**	**50**	**45**	**40**	**35**	**32**	**28**	**25**	**22**	**20**	**18**
WAS	Mask substrate flatness (micron peak-to-valley)	**10**	**5**	**5**		**5**	**5**		**4**	**4**		**3**
IS	Mask substrate flatness (micron peak-to-valley)	**10**	**5**	**5**	**5**	**5**	**5**	**4.5**	**4**	**4**	**3.5**	**3**
WAS	Mask flatness within a sub-field (micron peak-to-valley)	**1**	**1**	**1**		**1**	**1**		**1**	**1**		**1**
IS	Mask flatness within a sub-field (micron peak-to-valley)	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**

Manufacturable solutions exist, and are being optimized (white)
Manufacturable solutions are known (yellow)
Interim solutions are known (hatched yellow with red diamond)
Manufacturable solutions are NOT known (red)

Notes for Table 79c—EPL Mask requirements

EPL masks have hundreds of sub-fields (~1 by 1 mm), and each sub-field corresponds to a membrane surrounded by Si struts

[A] Wafer Minimum Feature Size—Minimum wafer line size imaged in resists. Line size as drawn or printed to zero bias (Most commonly applied to isolated lines. Drives CD uniformity and linearity).

[B] Magnification—Lithography tool reduction ratio, N:1.

[C] Mask Minimum Image Size—The nominal mask size of the smallest primary feature to be transferred to the wafer (Includes biasing for proximity effect correction).

[D] Image Placement Error in Sub-field—The three sigma deviation (X or Y) of the images in a sub-field relative to a defined reference grid. Please note that a sub-field is 1 mm × 1 mm on the mask. These values do not comprehend additional image placement error induced by mask clamping in the exposure tool.

[E] Sub-field Placement in Mask—The three sigma non-linear deviation (X or Y) of the position of sub-fields on mask relative to a defined reference grid. The position of each sub-field can be represented by a mark on the strut adjacent to the sub-field. Note that the EPL exposure tool can correct sub-field positions on wafer in accordance with the measurement results of sub-field positions on mask. These values do not comprehend additional image placement error induced by mask clamping in the exposure tool.

[F] CD Uniformity—The three sigma deviation of actual image sizes on a mask for a single size and tone critical feature. Applies to features in X and Y and multiple pitches from isolated to dense. Contacts: Measure and tolerance refer to the area of the mask feature.

[G] Linearity—Maximum deviation between mask "Mean to Target" for a range of features of the same tone and different design sizes. This includes features that are greater than the mask minimum primary feature size and less than three times the minimum wafer half pitch multiplied by the magnification.

[H] CD Mean to Target—The maximum difference between the average of the measured feature sizes and the agreed upon feature size (design size). Applies to a single feature size and tone. S(Actual-Target)/Number of measurements.

[I] Defect Size—A mask defect is any unintended mask anomaly that prints or changes a printed image size by 10% or more. The mask defect size listed in the roadmap are the square root of the area of the smallest opaque or clear "defect" that is expected to print for the stated generation.

[J] Data Volume—This is the expected maximum file size for uncompressed data for a single layer as presented to a raster write tool.

[K] Mask Design Grid—Wafer design grid multiplied by the mask magnification.

[L] Clear Area Transmission Factor—Percentage of current incident on a clear area on the mask relative to that arriving at wafer through the axial back focal plane aperture of the projection optics of the exposure tool (for NA of 6–8 mrad).

[M] Membrane Thickness Uniformity in Mask—The three sigma variation of membrane thickness over a mask.

[N] Membrane Thickness Uniformity in Sub-field—The three sigma variation of membrane thickness over a sub-field. Note that a sub-field is a 1×1 mm area.

[O] Membrane Mean Thickness Error—Maximum deviation of mean membrane thickness from designed value.

[P] Scatterer Thickness Uniformity in Mask—The three sigma variation of scatterer thickness over a mask.

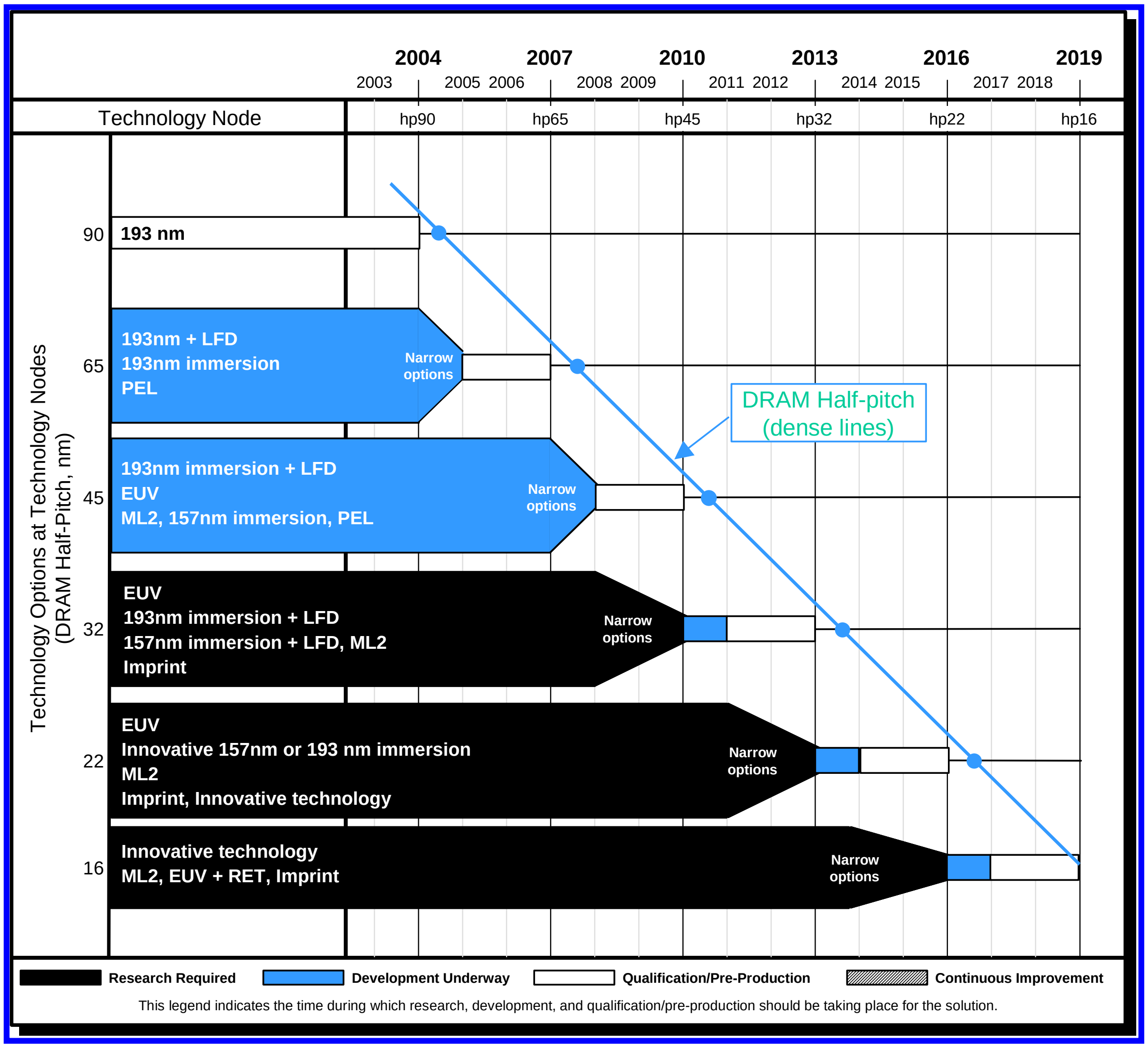
[Q] Scatterer Mean Thickness Error—Maximum deviation of scatterer thickness from designed value.

[R] Pattern Sidewall Angle—Sidewall angle must be 90 degrees with respect to the plane of the membrane surface. The sidewall may only be slightly retrograde, so the angle must be 90 degrees plus the tolerance.

[S] Scatterer/stencil LER—Line edge roughness (LER) is defined as roughness 3 sigma one-sided for spatial period < minimum linewidth.

[T] Membrane masks have patterned scattering layers on each membrane.

[U] Stencil masks have patterns etched through the membranes in each sub-field.



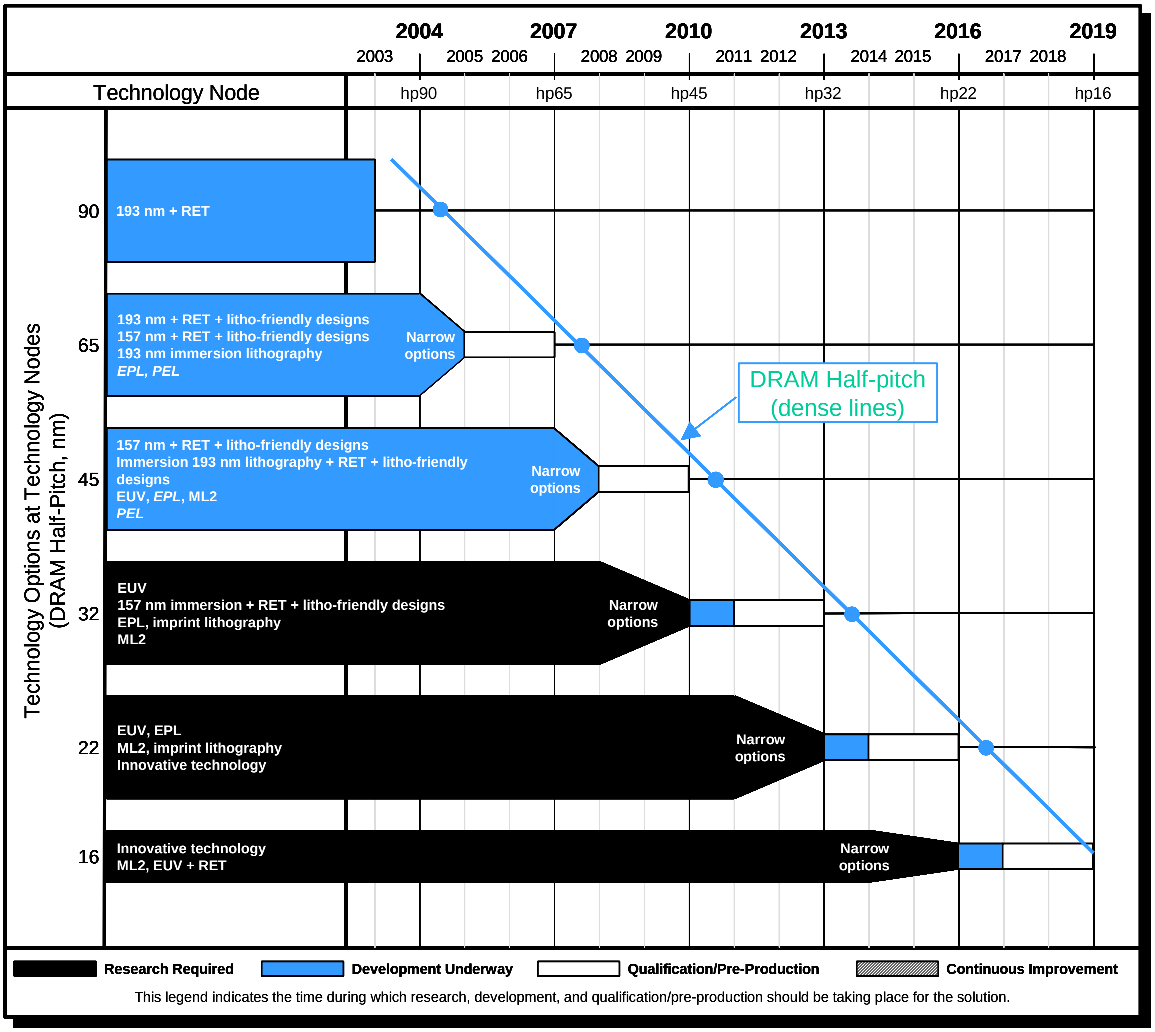
Notes: EPL is a potential solution at the 65, 45 and 32-nm nodes for one geographical region, and PEL is a potential solution at the 32-nm node for one geographical region. RET will be used with all optical lithography solutions, including with immersion; therefore, it is not explicitly noted.

RET — resolution enhancement technology EUV — extreme ultraviolet EPL — electron projection lithography

ML2—maskless lithography PEL—proximity electron lithography LFD—Lithography friendly design rules

Figure 53 2004 Lithography Exposure Tool Potential Solutions ***UPDATED****

*To compare to previous version of this figure see the following page.



Technologies shown in italics have only single region support.
RET—resolution enhancement technology EUV—extreme ultraviolet EPL—electron projection lithography
ML2—maskless lithography PEL—proximity electron lithography

Figure 53 2003 Lithography Exposure Tool Potential Solutions **WAS**