ASSEMBLY AND PACKAGING

Table 74 Assembly and Packaging Difficult Challenges [Update]

	Difficult Challenges ≥ 65 nm / Through 2007	*Summary of Issues*
Was	Improved organic substrates	– Tg compatible with Pb free solder processing – Increased wireability at low cost – Improved impedance control and lower dielectric loss to support higher frequency applications – Improved planarity and low warpage at higher process temperatures – Low-moisture absorption – Low-cost embedded passives
Is	Improved organic substrates	– Tg compatible with Pb free solder processing – Increased wireability at low cost – Improved impedance control and lower dielectric loss to support higher frequency applications – Improved planarity and low warpage at higher process temperatures – Low-moisture absorption – Low-cost embedded passives **–Substrate cost is barrier to flip chip adoption today**
Was	Improved underfills for flip chip on organic substrates	– Improve flow, fast dispense/cure, better interface adhesion, lower moisture absorption – Higher operating range for automotive in liquid dispense underfills – Improved adhesion, small filler size, and improved flow for mold based underfills
Is	Improved underfills for flip chip on organic substrates	– Improve flow, fast dispense/cure, better interface adhesion, lower moisture absorption – Higher operating range for automotive **and Pb free soldering** in liquid dispense underfills – Improved adhesion, small filler size, and improved flow for mold based underfills **–Issues are manufacturability for chip-size packages, compatibility with Harsh environments (automotive) and improved reliability for soldering processes**
Was	Coordinated design tools and simulators to address chip, package, and substrate co-design	– Mix signal co-design and simulation environment – Faster analysis tools for transient thermal analysis and integrated thermal mechanical analysis – Electrical (power disturbs, EMI†, signal integrity associated with higher frequency/current and lower voltage switching) – Commercial EDA‡ supplier support
Is	Coordinated design tools and simulators to address chip, package, and substrate co-design	– Mix signal co-design and simulation environment – Faster analysis tools for transient thermal analysis and integrated thermal mechanical analysis – Electrical (power disturbs, EMI†, signal integrity associated with higher frequency/current and lower voltage switching) – Commercial EDA‡ supplier support **–System level co-design is needed now. EDA support for "native" area array is required to meet the Roadmap projections.** **- Educational programs required to train engineers in these technologies/requirements.**
Was	Impact of Cu/low κ on packaging	– Direct wirebond and bump to Cu – Bump and underfill technology to assure low κ dielectric integrity – Improved Mechanical strength of dielectrics – Interfacial adhesion
Is	Impact of Cu/low κ on packaging	– Direct wirebond and bump to Cu – Bump and underfill technology to assure low κ dielectric integrity – Improved Mechanical strength of dielectrics – Interfacial adhesion **–Mechanisms to measure the critical properties need to be developed.**
	Pb, Sb, and Br free packaging materials	– Lower cost materials and processes to meet new requirements, including higher reflow temperatures. – Reliability under thermal cycling (stress and moisture)

Table 74 Assembly and Packaging Difficult Challenges [Update] (continued)

	Difficult Challenges < 65 nm / Beyond 2007	*Summary of Issues*
	Package cost that may greatly exceed die cost	– Research investments required for packaging cost reduction are decreasing
	Small, high pad count	– Array I/O pitches below 80 microns
Was	High Frequency die	– Substrate wiring density to support >20 lines/mm – Lower loss dielectrics – Skin effect above 10GHz
Is	High Frequency die	– Substrate wiring density to support >20 lines/mm – Lower loss dielectrics – Skin effect above 10GHz **–"Hot spot" thermal management needs to be addressed before 2007. There is a "brick wall at 5 micron lines and spaces. Design TWG would like to have an upper bound on thermal management capability of future packages.**
Was	Close gaps between substrate technology and the chip	– Interconnect density scaled to silicon (silicon I/O density increasing faster than the printed circuit
Is	Close gaps between substrate technology and the chip	– Interconnect density scaled to silicon (silicon I/O density increasing faster than the printed circuit **–Production techniques will require silicon-like production and process technologies after 2005.**
Was	System level design capability to integrated chips, passives and substrates	– Partitioning of system designs and manufacturing across numerous companies will make required optimization for performance, reliability, and cost of complex systems very difficult. Complex standards for information types and management of information quality along with a structure for moving this information will be required.
Is	System level design capability to integrate chips, passives and substrates	– Partitioning of system designs and manufacturing across numerous companies will make required optimization for performance, reliability, and cost of complex systems very difficult. Complex standards for information types and management of information quality along with a structure for moving this information will be required. **–The thermal/mechanical issues must be included with the electrical issues described in the 2001 Roadmap. This is also an issue before 2007.Embedded passives may be integrated into the "bumps" as well as the substrates.**
Add	**Electromigration is not addressed and will become a more limiting factor through this period. It must be addressed together with a thermal/mechanical reliability modeling.**	**–Electromigration may become a limiting factor as the current per unit area increases**

SIP as addressed but the Roadmap does not deal with the critical issues of "systems" packaging. System designers and design tools need to contemplate these alternatives.
Bumpless area array technologies will be needed during this period. Face-to-face packages is one example. Higher frequency, lower power and lower profile are driving forces.

** CTE - Coefficient of thermal expansion*

*** UBM - Under bump metallurgy*

†-EMI-Electromagnetic interference

‡ EDA-Electronic design automation

Table 75a Single-chip Packaging Technology Requirements—Near-term

	Year of Production	*2001*	*2002*	*2003*	*2004*	*2005*	*2006*	*2007*
	DRAM ½ Pitch (nm)	*130*	*115*	*100*	*90*	*80*	*70*	*65*
	MPU / ASIC ½ Pitch (nm)	*150*	*130*	*107*	*90*	*80*	*70*	*65*
	MPU Printed Gate Length (nm)	*90*	*75*	*65*	*53*	*45*	*40*	*35*
	MPU Physical Gate Length (nm)	*65*	*53*	*45*	*37*	*32*	*28*	*25*
	Cost (Cents/Pin) [1][2]							
Was	Low Cost	**0.30–0.75**	**0.28–0.68**	**0.26–0.62**	**0.25–0.56**	**0.24–0.51**	**0.23–0.46**	**0.22–0.41**
Is	Low Cost, Hand held and Memory **The color applies to the low end only and are due only to cost. The high end numbers are OK**	**0.30–0.75**	**0.30–0.62**	**0.30–0.56**	**Scale @ 5% per year**			
Was	Hand-held	**0.45–0.90**	**0.42–0.81**	**0.40–0.73**	**0.38–0.65**	**0.36–0.60**	**0.34–0.56**	**0.32–0.52**
Is	Hand-held **Delete these categories**	**0.45–0.90**	**0.30–0.62**	**0.30–0.56**	**Scale @ 5% per year**			
Was	Cost-performance	**0.80–1.60**	**0.75–1.44**	**0.70–1.30**	**0.66–1.17**	**0.61–1.06**	**0.56–1.03**	**0.53–1.00**
Is	Cost-performance	**0.80–1.60**	**0.75–1.30**	**Scale @ 5% per year high end keep low end due to added complexity (power, pad pitch, increased bumps per die, etc)**				
	High-performance	**2.2**	**2.09**	**1.98**	**1.88**	**1.78**	**1.69**	**1.61**
Was	Harsh	**0.45–4.00**	**0.40–3.60**	**0.36–3.20**	**0.32–2.88**	**0.29–2.59**	**0.26–2.33**	**0.23–2.11**
Is	Harsh **Pb free will cause consolidation with other categories**	**0.45–4.00**	**0.40–3.60**	**0.36–3.20**	**0.32–2.88**	**0.29–2.59**	**0.26–2.33**	**0.23–2.11**
Was	Memory	**0.36–1.54**	**0.34–1.39**	**0.32–1.26**	**0.30–1.14**	**0.28–1.03**	**0.27–0.93**	**0.27–0.84**
Is	Memory **Delete these categories**	**0.36–1.54**	**0.34–1.39**	**0.32–1.26**	**0.30–1.14**	**0.28–1.03**	**0.27–0.93**	**0.27–0.84**
	Chip Size (mm^2) [3]							
	Low Cost	**57**	**59**	**61**	**63**	**65**	**65**	**65**
	Hand-held	**57**	**59**	**61**	**63**	**65**	**65**	**65**
	Cost-performance	**170**	**178**	**186**	**195**	**204**	**204**	**204**
	High-performance	**310**	**310**	**310**	**310**	**310**	**310**	**310**
	Harsh	**60**	**80**	**100**	**100**	**100**	**100**	**100**
	Memory	**127**	**141**	**157**	**175**	**175**	**175**	**175**
	Power: Single Chip Package (Watts) [4]							
	Low Cost	**n/a**	**n/a**	**n/a**	**n/a**	**n/a**	**n/a**	**n/a**
	Hand-held	**2.4**	**2.6**	**2.8**	**3.2**	**3.2**	**3.5**	**3.5**
Was	Cost-performance	**61**	**75**	**81**	**85**	**92**	**98**	**104**
Is	Cost-performance	**61**	**75**	**81**	**85**	**92**	**98**	**104**
Was	High-performance	**130**	**140**	**150**	**160**	**170**	**180**	**190**
Is	High-performance	**130**	**140**	**150**	**160**	**170**	**180**	**190**
	Harsh	**14**	**14**	**14**	**16**	**16**	**18**	**18**
	Memory	**1.2**	**1.4**	**1.6**	**1.8**	**2**	**2**	**2**

Table 75a Single-chip Packaging Technology Requirements—Near-term (continued)

	Year of Production	2001	2002	2003	2004	2005	2006	2007
	DRAM ½ Pitch (nm)	130	115	100	90	80	70	65
	MPU / ASIC ½ Pitch (nm)	150	130	107	90	80	70	65
	MPU Printed Gate Length (nm)	90	75	65	53	45	40	35
	MPU Physical Gate Length (nm)	65	53	45	37	32	28	25
	Core Voltage (Volts)							
Was	Low Cost	1.8	1.2	1.2	1.2	1.2	0.9	0.9
Is	Low Cost	1.8	1.2	1.2	1.2	1	0.9	0.9
Was	Hand-held	1.2	1.2	1.1–1.2	1.1–1.2	1.1–1.2	1.0–1.2	0.9–1.1
Is	Hand-held	1.2	1.2	1.1–1.2	1.1–1.2	1	1.0–1.2	0.9–1.1
Was	Cost-performance	1.8	1.5	1.5	1.2	1.2	0.9	0.9
Is	Cost-performance	1.8	1.5	1.2	1.2	1	0.9	0.9
	High-performance	1.1	1	1	1	0.9	0.9	0.7
	Harsh	3.3	2.5	2.5	2.5	1.2	1.2	1.2
Was	Memory	1.8	1.5	1.5	1.2	1.2	1.2	0.9
Is	Memory	1.8	1.5	1.2	1.2	1	1.2	0.9
	Package Pincount maximum [5][6]							
	Low Cost	90–338	100–371	112–408	122–448	134–494	144–534	160–598
	Hand-held	100–420	112–464	122–508	134–560	144–616	160–680	176–748
	Cost-performance	480–1200	480–1320	500–1452	500–1600	550–1760	550–1936	600–2140
Was	High-performance	1700	1870	2057	2263	2489	2738	3012
Is	High-performance	1700	1870	2057	2263	2489	2738	3012
	Harsh	280	308	338	372	408	448	494
	Memory	44–128	44–144	44–144	48–160	48–160	48–160	48–160
	Minimum Overall Package Profile (mm)							
	Low Cost	1	1	1	1	0.5	0.5	0.5
	Hand-held	0.5	0.5	0.5	0.5	0.5	0.5	0.5
Was	Cost-performance	1.0–1.2	1.0–1.2	1.0–1.2	0.8–1.2	0.8–1.2	0.8–1.2	0.8–1.2
Is	Cost-performance	1.0–1.2	1	1	0.8	0.8	0.8	0.8
	High-performance	n/a	n/a	n/a	n/a	n/a	n/a	N/a
	Harsh	1	1	1	1	1	1	1
	Memory	1	1	1	0.8	0.5	0.5	0.5

White–Manufacturable Solutions Exist, and Are Being Optimized
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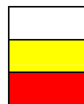

Table 75a Single-chip Packaging Technology Requirements—Near-term (continued)

	Year of Production	*2001*	*2002*	*2003*	*2004*	*2005*	*2006*	*2007*
	DRAM ½ Pitch (nm)	*130*	*115*	*100*	*90*	*80*	*70*	*65*
	MPU / ASIC ½ Pitch (nm)	*150*	*130*	*107*	*90*	*80*	*70*	*65*
	MPU Printed Gate Length (nm)	*90*	*75*	*65*	*53*	*45*	*40*	*35*
	MPU Physical Gate Length (nm)	*65*	*53*	*45*	*37*	*32*	*28*	*25*
	Performance: On-Chip (MHz)[7].							
	Low Cost	415/2400	460/2640	502/3194	552/3514	607/3865	668/4251	735/4676
	Hand-held	415/2400	460/2640	502/3194	552/3514	607/3865	668/4251	735/4676
	Cost-performance	1700	2320`	3090	3990	5170	5630	6740
	High-performance	1700	2320	3090	3990	5170	5630	6740
	Harsh	60	66	72	80	88	96	106
	Memory	166/400	200/440	200/495	200/550	200/612	300/673	300/740
	Performance: Chip-to-Board for Peripheral Buses (MHz) [7]							
	Low Cost	100	100	100	100	100	100	100
	Hand-held	100	100	100	100	100	100	100
	Cost-performance	166/600	200/660	200/726	200/798	300/878	300/966/1062	300/1063
	High-performance	1700	1870	2057	2262	2488	2737	3011
	Harsh	60	66	72	80	88	96	106
	Memory (D/SRAM/RDRAM)	166/400	200/445	200/495	200/550	300/612	300/673	300/714
	Junction Temperature Maximum (°C).							
	Low Cost	125	125	125	125	125	125	125
	Hand-held	100	100	100	100	100	100	100
Was	Cost-performance	105	85	85	85	85	85	85
Is	Cost-performance	105	90	90	90	85	85	85
Was	High-performance	90	85	85	85	85	85	85
Is	High-performance	90	90	90	90	90	85	85
Was	Harsh - Complex IC's	150	150	150	150	150	150	150
Is	Harsh - Complex IC's							
	Memory	125	125	125	125	125	125	125
	Operating Temperature Extreme: Ambient (°C) ***Driven by automotive industry for harsh(Japan, US, Germany).***							
	Low Cost	55	55	55	55	55	55	55
	Hand-held	55	55	55	55	55	55	55
	Cost-performance	45	45	45	45	45	45	45
	High-performance	45	45	45	45	45	45	45
	Harsh Complex IC's	-40 to 125	-40 to 125	-40 to 125	-40 to 125	-40 to 125	-40 to 125	-40 to 125
	Harsh-Power/Linear	-40 to 150	-40 to 150	-40 to 180	-40 to 180	-40 to 200	-40 to 200	-40 to 200
Add	Memory	TBD	TBD	TBD	TBD	TBD	TBD	TBD

Table 75b Single-chip Packaging Technology Requirements—Long-term

Note—same comments in red in Table 75a apply

	Year of Production	*2010*	*2013*	*2016*
	DRAM ½ Pitch (nm)	*45*	*32*	*22*
	MPU / ASIC ½ Pitch (nm)	*50*	*35*	*25*
	MPU Printed Gate Length (nm)	*25*	*18*	*13*
	MPU Physical Gate Length (nm)	*18*	*13*	*9*
	Cost (Cents/Pin)[1] [2]			
Was	Low Cost	0.22–0.49	0.19–0.42	0.19–0.39
Is	Low Cost	0.22–0.49	0.19–0.42	0.19–0.39
Was	Hand-held	0.27–0.70	0.23–0.67	0.20–0.56
Is	Hand-held	0.27–0.70	0.23–0.67	0.20–0.56
Was	Cost-performance	0.49–0.98	0.42–0.93	0.36–0.79
Is	Cost-performance	0.49–0.98	0.42–0.93	0.36–0.79
	High-performance	1.68	1.44	1.22
	Harsh	0.27–1.54	0.23–1.12	0.20–.9
Was	Memory	0.22–0.54	0.19–0.39	0.19–0.33
Is	Memory	0.22–0.54	0.19–0.39	0.19–0.33
	Chip Size (mm^2)[3]			
	Low Cost	81	90	90
	Hand-held	81	90	90
	Cost-performance	268	307	307
	High-performance	310	310	310
	Harsh	150	150	150
	Memory	191	250	250
	Power: Single Chip Package (Watts)[4]			
	Low Cost	N/A	N/A	N/A
	Hand-held	3	3	3
Was	Cost-performance	119.6	137.6	158.2
Is	Cost-performance	119.6	137.6	158.2
Was	High-performance	218	250.7	288.3
Is	High-performance	218	250.7	288.3
	Harsh	20.7	23.8	27.4
	Memory	2.3	2.65	3.05

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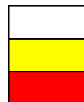

Table 75b Single-chip Packaging Technology Requirements—Long-term (continued)

Note—same comments in red in Table 75a apply

	Year of Production	*2010*	*2013*	*2016*
	DRAM ½ Pitch (nm)	*45*	*32*	*22*
	MPU / ASIC ½ Pitch (nm)	*50*	*35*	*25*
	MPU Printed Gate Length (nm)	*25*	*18*	*13*
	MPU Physical Gate Length (nm)	*18*	*13*	*9*
	Core Voltage (Volts)			
	Low Cost	**0.6**	**0.5–0.6**	**0.3**
	Hand-held	**0.5**	**0.4**	**0.4**
	Cost-performance	**0.6**	**0.6**	**0.5**
	High-performance	**0.6**	**0.5**	**0.4**
	Harsh	**1.2**	**0.9**	**0.9**
	Memory	**0.6**	**0.6**	**0.3**
	Package Pincount [5] [6]			
	Low Cost	**208–777**	**270–1011**	**351–1314**
	Hand-held	**229–972**	**298–1264**	**387–1643**
Was	Cost-performance	**780–2782**	**1014–3616**	**1318–4702**
Is	Cost-performance	**780–2782**	**1014–3616**	**1318–4702**
Was	High-performance	**4009**	**5335**	**7100**
Is	High-performance	**4009**	**5335**	**7100**
	Harsh	**642**	**835**	**1086**
	Memory	**62–208**	**81–270**	**105–351**
	Overall Package Profile (mm)			
Was	Low Cost	**0.8**	**0.5**	**0.5**
Is	Low Cost	**0.5**	**0.5**	**0.5**
Was	Hand-held	**0.65**	**0.5**	**0.5**
Is	Hand-held	**0.5**	**0.5**	**0.5**
Was	Cost-performance	**0.65-0.8**	**0.50–0.65**	**0.5–0.65**
Is	Cost-performance	**0.5**	**0.5**	**0.5**
	High-performance	**n/a**	**n/a**	**n/a**
	Harsh	**1**	**1**	**0.8**
Was	Memory	**0.65**	**0.5**	**0.5**
Is	Memory	**0.5**	**0.5**	**0.5**

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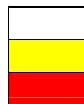

Table 75b Single-chip Packaging Technology Requirements—Long-term (continued)

Note—same comments in red in Table 75a apply

	Year of Production	*2010*	*2013*	*2016*
	DRAM ½ Pitch (nm)	*45*	*32*	*22*
	MPU / ASIC ½ Pitch (nm)	*50*	*35*	*25*
	MPU Printed Gate Length (nm)	*25*	*18*	*13*
	MPU Physical Gate Length (nm)	*18*	*13*	*9*
	Performance: On-Chip (MHz) [7]			
	Low Cost	**956–6079**	**1243–7903**	**1616–10274**
	Hand-held	**956–6079**	**1243–7903**	**1616–10274**
	Cost-performance	**12000**	**19000**	**29000**
	High-performance	**12000**	**19000**	**29000**
	Harsh	**138**	**179**	**234**
	Memory	**450/984**	**600/1280**	**750/1665**
	Performance: Chip-to-Board for Peripheral Buses (MHz)[7]			
	Low Cost	**125**	**125**	**150**
	Hand-held	**125**	**125**	**150**
	Cost-performance	**300/1415**	**300/1883**	**300/2506**
	High-performance	**4009**	**5339**	**7100**
	Harsh	**125**	**125**	**150**
	Memory (S/SRAM)	**250/761**	**250/963**	**250/1175**
	Junction Temperature Maximum (°C) for Cost- performance			
	Low Cost	**125**	**125**	**125**
	Hand-held	**100**	**100**	**100**
Was	Cost-performance	**85**	**85**	**85**
Is	Cost-performance	**85**	**85**	**85**
Was	High-performance	**85**	**85**	**85**
Is	High-performance	**85**	**85**	**85**
	Harsh	**150**	**150**	**150**
	Harsh-Complex IC's	**190**	**190**	**190**
	Memory	**100**	**100**	**100**
	Operating Temperature Extreme: Ambient (°C)			
	Low Cost	**55**	**55**	**55**
	Hand-held	**55**	**55**	**55**
	Cost-performance	**45**	**45**	**45**
	High-performance	**45**	**45**	**45**
	Harsh	**-40 to 125**	**-40 to 125**	**-40 to 125**
	Harsh-Complex IC's	**-40 to 150**	**-40 to 150**	**-40 to 150**
	Memory	**55**	**55**	**55**

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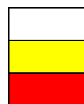


Table 76 Comparison between Bare Chip Mounting and WLP Technology

Item	Bare Chip Mounting	Wafer Level Packaging
Package Type	—	*– Real chip size package (FBGA)*
Device Body Size	*– Same as chip size*	*– Same as chip size*
Terminal Design of Device	*– All terminal pads shall be located in adaptable pitch on chip*	*– All terminal pads shall be located in adaptable pitch on chip*
Quality Assurance of Device	*– Difficult (especially burn in test)*	*– Easy*
Interconnection of Board	*– Wire bonding (WB)* *– Flip chip bonding (FCB)*	*– Solder ball terminal*
Interconnecting Wire Length	*– FCB can achieve the shortest connection length*	*– May be slightly longer than FCB for re-wire die and ball*
Mounting Area on Board	*– Slight larger than chip area (fan-out for WB)* *– (Under fill print area for FCB)*	*– Same area as chip size*
Reliability after Board Mounting	*– Encapsulation and under-fill material required*	*– Near equal to conventional packages*
Mountability on Board	*– Facility for bare chip assembly required* *– Difficult to repair*	*– Multiple parts reflow available* *– Easy to be repaired by standard SMT assembly process*

Table 77 Chip to Next Level Potential Solutions

	Year of Production	*2001*	*2002*	*2003*	*2004*	*2005*	*2006*	*2007*	*2010*	*2013*	*2016*
	DRAM ½ Pitch (nm)	*130*	*115*	*100*	*90*	*80*	*70*	*65*	*45*	*32*	*22*
	MPU / ASIC ½ Pitch (nm)	*150*	*130*	*107*	*90*	*80*	*70*	*65*	*50*	*35*	*25*
	MPU Printed Gate Length (nm)	*90*	*75*	*65*	*53*	*45*	*40*	*35*	*25*	*18*	*13*
	MPU Physical Gate Length (nm)	*65*	*53*	*45*	*37*	*32*	*28*	*25*	*18*	*13*	*9*
	Chip Interconnect Pitch (µm)										
Was	Wire bond—ball	**45**	**35**	**30**	**25**	**20**	**20**	**20**	**20**	**20**	***20***
Is	Wire bond—ball	**45**	**40**	**35**	**30**	**25**	**20**	**20**	**20**	**20**	**20**
Was	Wire bond—wedge	**40**	**35**	**30**	**25**	**20**	**20**	**20**	**20**	**20**	**20**
Is	Wire bond—wedge	**50**	**50**	**40**	**40**	**35**	**35**	**30**	**20**	**20**	**20**
Was	TAB*.	**40**	**40**	**40**	**40**	**30**	**30**	**30**	**30**	**30**	**30**
Is	TAB* **Japan TWG has the lead for Tab technologies**	**45**	**40**	**35**	**35**	**30**	**30**	**25**	**20**	**20**	**15**
Was	Flip chip (area array for cost-performance and high-performance)	**160**	**160**	**150**	**150**	**130**	**130**	**120**	**90**	**80**	**70**
Is	**Flip chip area array**	**200**	**180**	**150**	**150**	**100**	**100**	**80**	**70**	**70**	**50**
Was	Peripheral flip chip for hand-held, low-cost, and harsh	**150**	**130**	**120**	**110**	**100**	**90**	**80**	**60**	**45**	**30**
Is	**Peripheral flip chip**	**80**	**80**	**60**	**60**	**40**	**40**	**30**	**20**	**20**	**15**

Table 78 Ball Grid Array Packages Potential Solutions

	Year of Production	*2001*	*2002*	*2003*	*2004*	*2005*	*2006*	*2007*	*2010*	*2013*	*2016*
	DRAM ½ Pitch (nm)	*130*	*115*	*100*	*90*	*80*	*70*	*65*	*45*	*32*	*22*
	MPU / ASIC ½ Pitch (nm)	*150*	*130*	*107*	*90*	*80*	*70*	*65*	*50*	*35*	*25*
	MPU Printed Gate Length (nm)	*90*	*75*	*65*	*53*	*45*	*40*	*35*	*25*	*18*	*13*
	MPU Physical Gate Length (nm)	*65*	*53*	*45*	*37*	*32*	*28*	*25*	*18*	*13*	*9*
	BGA Solder Ball Pitch (mm)										
Was	Low cost	**1**	**1**	**0.8**	**0.8**	**0.65**	**0.65**	**0.65**	**0.5**	**0.5**	**0.5**
Is	Low cost	**1**	**0.8**	**0.8**	**0.8**	**0.5**	**0.5**	**0.5**	**0.5**	**0.5**	**0.5**
Was	Hand-Held	**1**	**1**	**0.8**	**0.8**	**0.65**	**0.65**	**0.65**	**0.5**	**0.5**	**0.5**
Is	Hand-Held	**1**	**0.8**	**0.8**	**0.8**	**0.5**	**0.5**	**0.5**	**0.5**	**0.5**	**0.5**
Was	Cost-performance	**1**	**1**	**0.8**	**0.8**	**0.65**	**0.65**	**0.65**	**0.5**	**0.5**	**0.5**
Is	Cost-performance	**1**	**1**	**1**	**0.8**	**0.8**	**0.8**	**0.5**	**0.5**	**0.5**	**0.5**
Was	High-Performance	**0.8**	**0.8**	**0.8**	**0.8**	**0.65**	**0.65**	**0.65**	**0.5**	**0.5**	**0.5**
Is	High-Performance	**0.8**	**1**	**1**	**1**	**1**	**0.8**	**0.8**	**0.8**	**0.8**	**0.8**
Was	Harsh	**1.27**	**1.27**	**1**	**1**	**1**	**0.8**	**0.65**	**0.5**	**0.5**	**0.5**
Is	Harsh	**1.27**	**1.27**	**1**	**1**	**1**	**0.8**	**0.8**	**0.5**	**0.5**	**0.5**

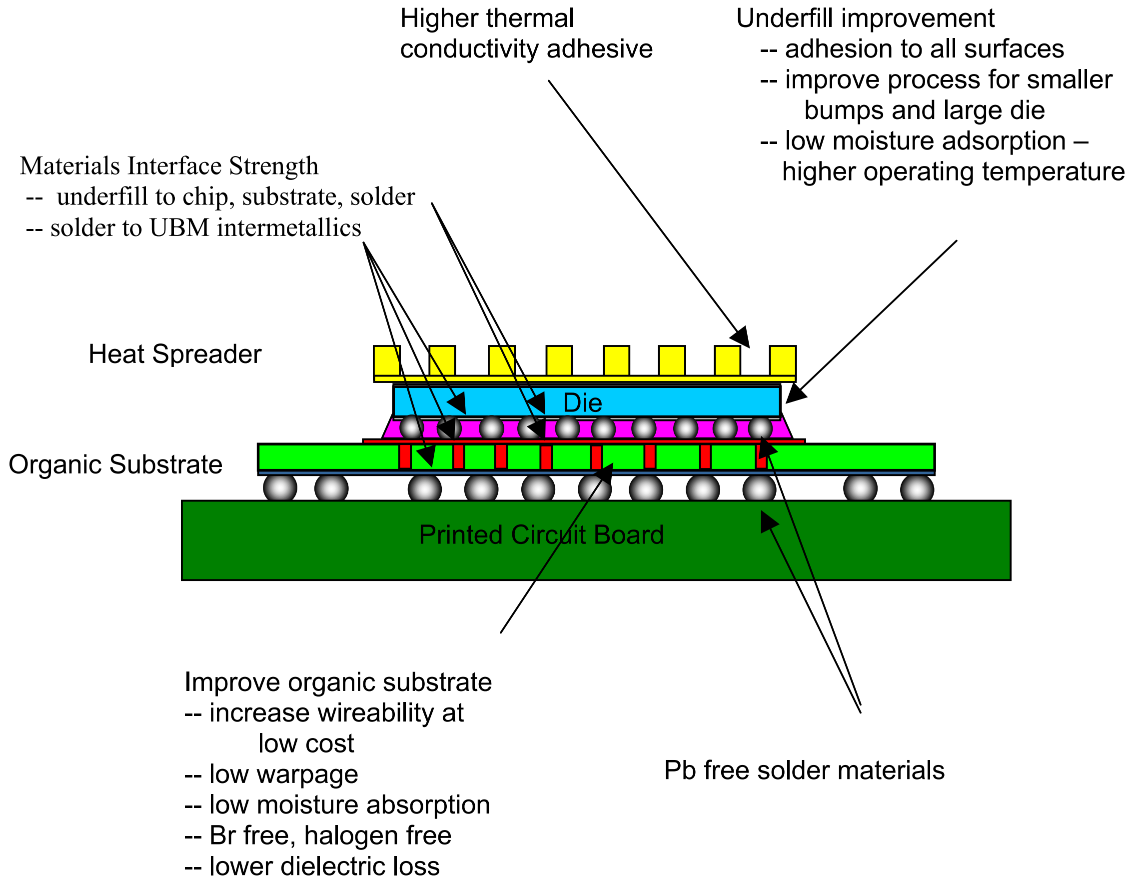
Table 79 Single Chip Packages Potential Solutions

	Year of Production	*2001*	*2002*	*2003*	*2004*	*2005*	*2006*	*2007*	*2010*	*2013*	*2016*
	DRAM ½ Pitch (nm)	*130*	*115*	*100*	*90*	*80*	*70*	*65*	*45*	*32*	*22*
	MPU / ASIC ½ Pitch (nm)	*150*	*130*	*107*	*90*	*80*	*70*	*65*	*50*	*35*	*25*
	MPU Printed Gate Length (nm)	*90*	*75*	*65*	*53*	*45*	*40*	*35*	*25*	*18*	*13*
	MPU Physical Gate Length (nm)	*65*	*53*	*45*	*37*	*32*	*28*	*25*	*18*	*13*	*9*
Was	FBGA/CSP area array pitch (mm)	**0.4**	**0.4**	**0.4**	**0.4**	**0.3**	**0.3**	**0.3**	**0.3**	**0.3**	**0.3**
Is	FBGA/CSP area array pitch (mm)	**0.5**	**0.5**	**0.4**	**0.4**	**0.3**	**0.3**	**0.2**	**0.15**	**0.15**	**0.1**
Was	FBGA/CSP size (mm/side)	**10**	**10**	**10**	**10**	**10**	**10**	**10**	**10**	**10**	**10**
Is	FBGA/CSP size (mm/side)	**4–21**	**4–21**	**4–21**	**4–21**	**4–21**	**4–21**	**4–21**	**4–21**	**4–21**	**4–21**

Table 80 BGA and FBGA/CSP Package Substrate Potential Solutions

	Year of Production	*2001*	*2002*	*2003*	*2004*	*2005*	*2006*	*2007*	*2010*	*2013*	*2016*
	DRAM ½ Pitch (nm)	*130*	*115*	*100*	*90*	*80*	*70*	*65*	*45*	*32*	*22*
	MPU / ASIC ½ Pitch (nm)	*150*	*130*	*107*	*90*	*80*	*70*	*65*	*50*	*35*	*25*
	MPU Printed Gate Length (nm)	*90*	*75*	*65*	*53*	*45*	*40*	*35*	*25*	*18*	*13*
	MPU Physical Gate Length (nm)	*65*	*53*	*45*	*37*	*32*	*28*	*25*	*18*	*13*	*9*
Was	FBGA/CSP solder ball pad pitch (mm)	**0.4**	**0.4**	**0.4**	**0.4**	**0.3**	**0.3**	**0.3**	**0.3**	**0.3**	**0.25**
Is	FBGA/CSP solder ball pad pitch (mm)	**0.5**	**0.5**	**0.4**	**0.4**	**0.3**	**0.3**	**0.2**	**0.15**	**0.15**	**0.1**
Was	Pad size (µm)	**160**	**160**	**160**	**160**	**120**	**120**	**120**	**120**	**120**	**100**
Is	Pad size (µm)	**200**	**200**	**160**	**160**	**120**	**120**	**120**	**120**	**120**	**100**
Was	Line width (µm)	**48**	**48**	**48**	**48**	**36**	**36**	**36**	**36**	**36**	**30**
Is	Line width (µm)	**60**	**60**	**48**	**48**	**36**	**36**	**24**	**18**	**18**	**12**
Was	Line spacing (µm)	**48**	**48**	**48**	**48**	**36**	**36**	**36**	**36**	**36**	**30**
Is	Line spacing (µm)	**60**	**60**	**48**	**48**	**36**	**36**	**24**	**18**	**18**	**12**
	# Rows accessed	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**

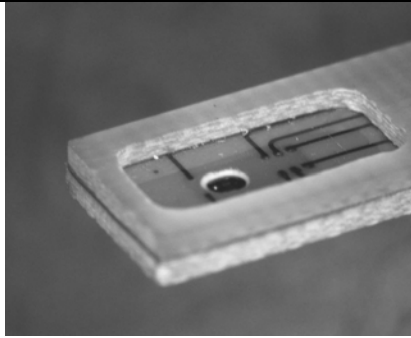
Summary of New Materials Requirements

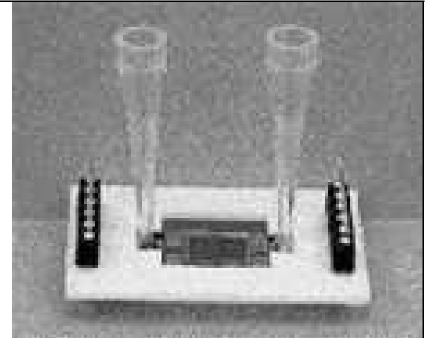


Materials and Interface Characterization Research Needs

- **-- materials properties**
- **-- materials interface properties**
- **-- data base for integrated chip to package model**

New Emerging Packaging Challenges for Emerging Technology



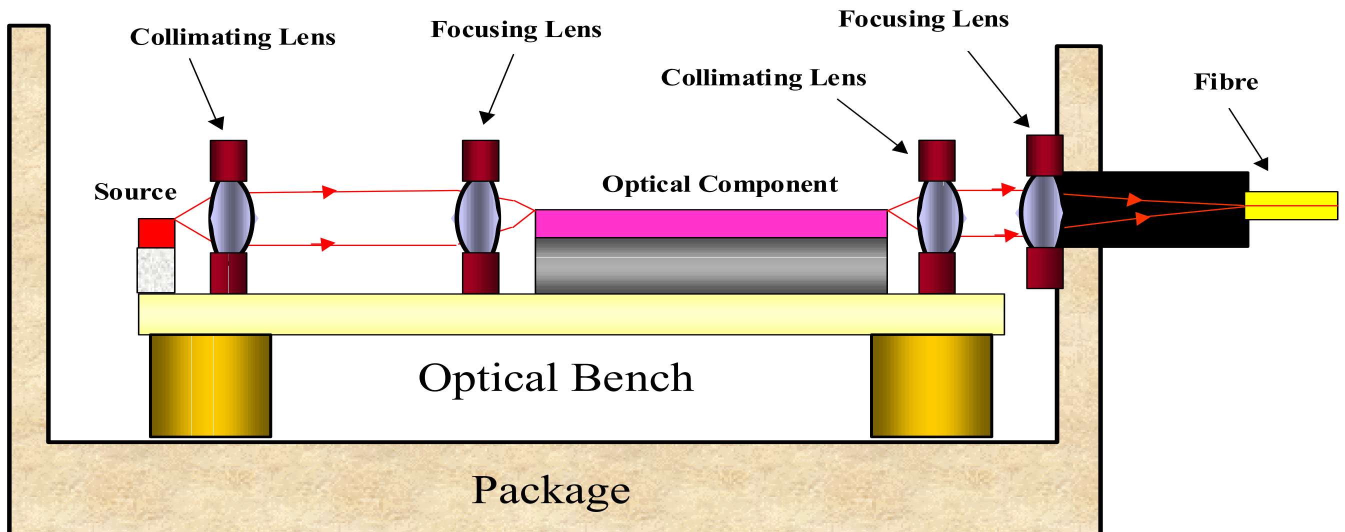


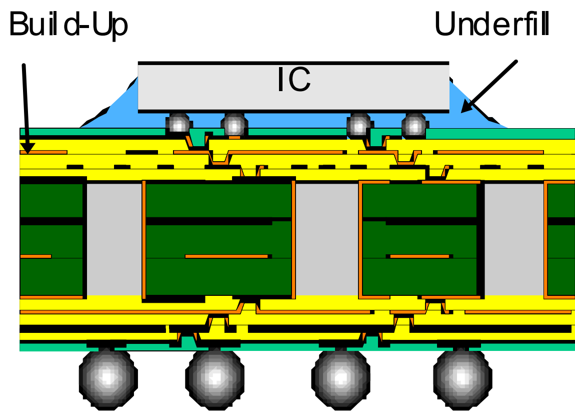
Vacuum package for uncooled IR bolometer

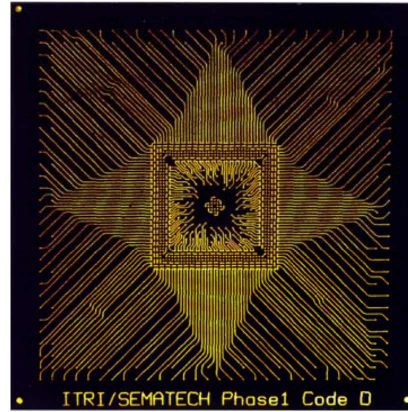
Package with exposed chip for ISFET

Fluidic interconnection for micro-PCR

Major Components for Optical Packaging







Thin film build-up using 75 µm vias

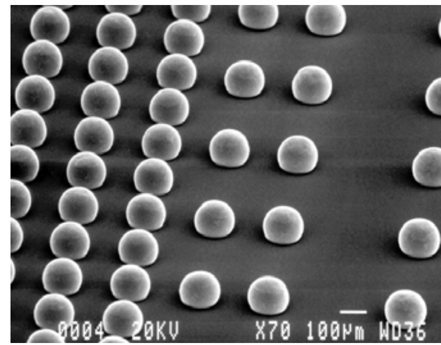


Figure 6. Flip chip interconnect and improved I/O pad arrangement